Two-pulse sub-ns switching of a perpendicular spin-orbit torque MRAM cell without external magnetic field

A. Makarov, V. Sverdlov, and S. Selberherr
Institute for Microelectronics, TU Wien, Vienna, Austria

The breathtaking increase in performance and speed of modern integrated circuits is steadily supported by continuous miniaturization of complementary metal-oxide semiconductor (CMOS) devices. However, a rapid growth of the standby power due to transistor leakage is becoming a pressing issue. The microelectronics industry is facing major challenges related to power dissipation and energy consumption, and microprocessor scaling will hit a power wall soon. A promising way to mitigate this trend is to introduce nonvolatility into integrated circuits. The development of electrically addressable nonvolatile memory combining high speed and high endurance is essential to achieve these goals by replacing static random access memory (SRAM), particularly in the caches of hierarchical multi-level processor memory structures [1]. The spin-orbit torque magnetic random access memory (SOT-MRAM) with perpendicular magnetization combines non-volatility, high speed and high endurance and is thus suitable for applications in caches [2]. However, its development is still hindered by the need of an external magnetic field to guarantee deterministic switching [3].

We discuss the two-pulse scheme previously proposed for switching of an in-plane structure [4]. The SOT due to the first 100 ps pulse tilts the magnetization of the free layer in-plane perpendicular to the direction of the write pulse 1. The SOT of the second consecutive pulse results in an additional precession of the magnetization in the part of the free layer under it, which is transferred to the remaining part of the free layer through the exchange interaction. Depending on the spin of this precession, the magnetization of the remaining part tilts up or down with respect to in-plane orientation. The part under the wire of write pulse 2 follows the precession after the current is turned off, thus completing the switching. Calculations of the switching times for several pulse durations as a function of the width of the second pulse wire is shown below. We conclude that the fastest, sub-300 ps switching is achieved at around 30% overlap of the second pulse wire with the free layer.

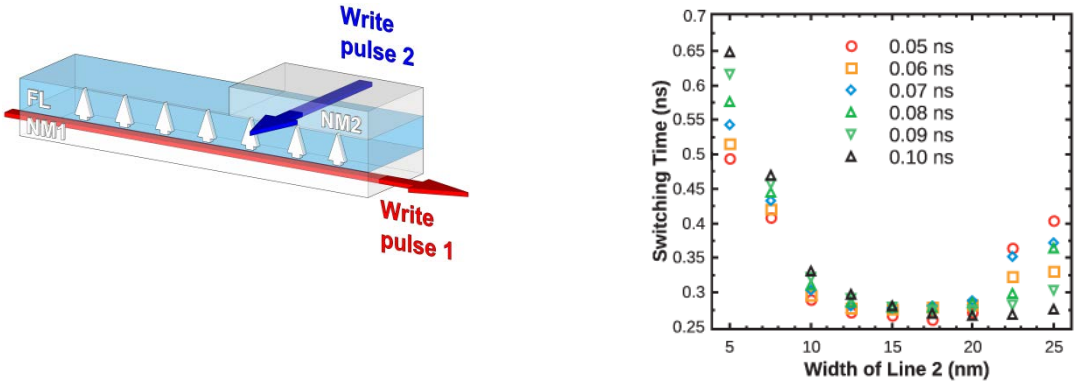

Fig. 1. (a) Perpendicular SOT-MRAM memory cell with a 52.5x12.5x2 nm free layer; (b) Switching time *vs.* line 2 width, for several durations of the pulse 2, $I_1 = I_2 = 100$ μA.

1. T. Hanyu *et al.*, *Proc. IEEE* **104**, 1844 (2016).
2. S.-W. Lee and K.-J. Lee, *Proc. IEEE* **104**, 1831 (2016).
3 S. Fukami *et al.*, *Nature Nanotechnol.* **11**, 621 (2016).
4. A. Makarov *et al.*, *Semicond. Sci. Technol.* **31**, 113006 (2016).