GaN-based vertical nanowire transistor for logic application

Dong-Hyeok Son, Jun-Hyeok Lee, Jeong-Gil Kim, Ki-Sik Im, and Jung-Hee Lee
School of Electronics Engineering, Kyungpook National University, Daegu 702-201, Korea

Although GaN has superior material properties, such as wide band-gap energy, high electron saturation velocity and high thermal stability, research into GaN-based devices for logic applications has been hindered by the high saturation voltage and high subthreshold swing compared to Si logic transistors. On the other hand, GaN FinFET devices have shown extremely low off-state leakage current, low subthreshold swing, smaller saturation voltage, and normally-off operation, indicating that GaN has the potential to replace Si-based logic devices. Moreover, GaN has higher effective mass and smaller permittivity compared to Si, Ge, and other III-V materials, which can effectively suppress the source-drain tunneling current and short channel effects in logic transistors.

Some years ago, we introduced GaN-based vertical nanowire transistors with a positive threshold voltage and low off-state leakage. However, the output current did not saturate, because the channel near the drain was not covered by the gate and hence high access resistance impeded current saturation.

In this work, we present GaN-based vertical nanowire transistors in which the channel is fully covered by the gate. As a result, these devices are not affected by access resistance and hence exhibit improved performance. Our device also exhibits a low saturation voltage of ~0.5 V, smaller than the overdrive voltage. The reason for this low saturation voltage is that the undoped nanowire channel with diameter of 120 nm, length of 300 nm, and relatively low background doping density of 2.0×10^{16} cm^{-3} can be easily pinched off even at small drain voltage without influence of access resistance, something that is difficult to achieve in conventional GaN-based transistors.

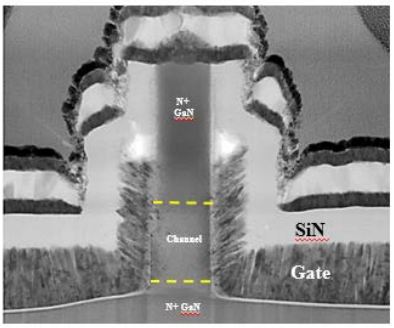

FIG. 1. Cross-sectional SEM image of the GaN-based vertical nanowire transistor.

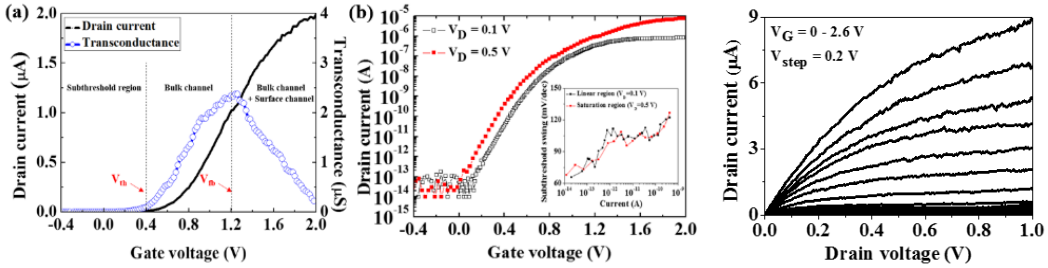

Fig. 2. Transfer (left) and output (right) characteristics of device.