Future of logic device technology in the short and long term

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Although Si MOSFETs have dominated the integrated circuit applications over the past four decades, it is anticipated that the development of CMOS would reach MOSFET downsizing limits sometime after the next decade. However, there are no really promising alternative candidates to replace Si MOSFETs for ultra-high-density CMOS integration with better performance and low cost. Thus, maybe, we have to stick to CMOS devices until the end of scaling. In order to pursue the downsizing of CMOS for another decade, the development of new technologies is becoming extremely important. Not all the companies can necessarily develop the most advanced technology in a timely fashion and the competition between the leading semiconductor manufacturing companies has become very severe, threatening their very survival.

The current status of the frontend of the technologies is as follows. Because of challenges in lithography and also in maintaining the I_{ON}/I_{OFF} ratio, the rate of the shrinkage for the line pitch and gate length has become significantly less aggressive, so that we will face the downsizing limit later than previously predicted. New device structures, such as multi-gate (Fin-FET, tri-gate, and Si-nanowire MOSFETs) and FD-SOI MOSFETs are already replacing the conventional planar MOSFETs. Continuous improvement of the high-κ/metal gate technology has enabled EOT scaling down to 0.9–0.8 nm in production, but introduction of new materials is desirable for further EOT scaling. In order to decrease the MOSFET gate length L_G down to deep sub-10 nm regime, we have to solve very difficult problems: significant increase in subthreshold current; significant decrease in conduction for ultra-narrow fins or ultra-thin Si SOI channels; significant increase of gate leakage current and reliability degradation for small EOT MOSFETs; and through-put decrease for very fine sub-10 nm lithography. At this moment, we do not know the solutions for those problems, although there are many interesting prospects in emerging technologies. Thus, probably, the Si Fin-FET with $L_G < 10$ nm would be the last generation of the logic CMOS scaling.

What would be next for the logic devices after they reach the downsizing limit? To answer the question, it is helpful to think about the "need" or application side, rather than the "supply" side. Currently, we are entering the "wearable" device era, but what comes next? I believe that "wearing" will somehow become annoying and people will want to be free from it, by turning to devices embedded in the surrounding environment, rather than carried by humans. Over the next few decades, logic devices will evolve to accommodate an environment-embedded network of sensors, with wireless communication and wireless power supply. And after that? The future several decades from now is a kind of a dream story. If pressed, I would bet on the introduction of biologically-inspired systems, with brain-mimicking algorithms for logic applications, DNA-based self-assembly of the logic devices, or even the use of insect parts for sensors, *etc*.