A lesson from archeology: The buried gates

A. Litty, Y. Solaro, H. El Dirani, S. Ortolland, P. Fonteneau, L. Onestas,
C. Fenouillet-Béranger, C. Le Royer, M. Bawedin, A. Zaslavsky, P. Ferrari, and S. Cristoloveanu
STMicroelectronics, Crolles, and *IMEP-LAHC, Grenoble Institute of Technology, Minatec, Grenoble,*
and *CEA, LETI, Minatec Campus, Grenoble, France;* and *Brown University, Providence RI, USA*

In FD–SOI technology, there is plenty of room at the bottom … underneath the buried insulator. Ground planes (GPs) can be added and used as secondary gates in order to make SOI circuits think more rapidly and spend less energy.

Since two are better than one, *n*-type and *p*-type GPs are offered as regular design options. They are of particular interest for devices where the body is partitioned into regions with independent functions.

We demonstrate the advantages conferred by GPs for two device prototypes. First is the ultrathin LDMOS transistor fabricated at the 14 nm node. The GP located below the gate region serves to tune the threshold voltage: high V_T in OFF-mode for reduced leakage and low V_T in ON-mode for enhanced drive current. The second GP, designed below the drift region of the LDMOS, enables independent control of the series resistance and breakdown voltage.

A second example is the band-modulation transistor, named Z^3-FET, where the two GPs act as control buried gates and the top surface is free. The advantage is to eliminate the gate dielectric with its reliability issues and to use the free surface for detecting ions, light, ESD events, *etc*.

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