Challenges to ultra-low-power operation

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We are facing dramatic challenges in static and dynamic power consumption of ICs, which could be overcome using disruptive devices, technologies and materials. Promising solutions includes 2D layers, transition-metal dichalcogenides (TMDs), heterostructures using strained Si, Ge and III-V thin films, multi-gates, nanowires, CNTs, tunnel FETs and NEMS.

In the field of MOSFETs, several very interesting advances have been recently shown. 3DFETs can improve sub-20 nm CMOS node performance and substantially reduce supply voltage and short channel effects. However, the traditional Si channel could be replaced by high-mobility materials in future VLSI applications. Heterogeneous 2D atomic crystals, especially TMDs, have atomically smooth surfaces without dangling bounds, no thickness fluctuations, and good mobility in CVD-deposited films. A first CMOS-compatible TMD 3D transistor technology using novel hybrid Si/MoS_2 channel Fin-FET and NWFET with improved I_{ON} has been demonstrated. It has also been shown that bilayer MoS_2 channel FETs can meet high-performance (HP) requirements down to 6.6 nm node, while low-standby-power (LSTP) requirements present significant challenges for sub-10 nm nodes. On the other hand, the high mobility and the low effective mass of WSe_2 enable 2D FETs for both HP and LSTP applications down to the 5 nm node. SOI topology can only sustain good electrostatics for single-layer TMDs, while double-gate topology can do so for up to three layers.

A comparative analysis of ring oscillators based on different channel materials, different spacer materials, and different transistor architectures suggests that the largest benefits of speed gain and reduction in power consumption for MOSFET architectures is achieved by switching from 7 nm Si baseline Fin-FET process to 5 nm vertical Si NWs.

In the domain of small slope switches, the TFETs seem very promising. However, so far, no one has demonstrated experimentally a TFET that has simultaneously both an I_{ON} comparable to CMOS and a subthreshold swing of less than 60 mV/decade over several decades. The highest current for which a subthreshold swing of 60 mV/decade is observed is approximately 1 nA/μm. A new class of electron-hole bi-layer (EHB) TFETs was proposed with parallel tunneling direction and gate electric field, which allows I_{ON} to be proportional to the gate length. Semi-classical simulations for Ge EHB-TFETs showed impressive results that later on needed to be corrected by the consideration of quantum mechanical effects and parasitic lateral tunneling, with undesirable implications for the device performance. Simulated TFETs with 2D layers using MoS_2-WTe_2 vertical tunneling also showed very good subthreshold swing.

Finally, heterostructure TFETs realized with III-V materials have been compared by quantum simulations, showing results significantly better than reference MOSFETs [1–9].

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