Getting rid of the DRAM capacitor

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Since the early days of the DRAM memory cells, it has been clear that their integration in the standard CMOS process would be increasingly difficult [1]. However, DRAM has survived for more than 30 years, overcoming the scaling issues faced at each technology node. Nowadays, with 20 nm-class DRAM in production, the scalability of this technology is more questioned than ever. Integration of sufficient capacitor area, charge transfer from the storage node into the bit line, and leakage current are major issues pushing towards a paradigm shift [2].

The suppression of the external storage element, which simplifies the cell architecture while maintaining fast charge transfer within a single transistor, is a topic attracting great interest. Several single-transistor DRAM variants (1T-DRAMs) have been proposed during the last ten years as candidates for DRAM replacement [3, 4]. Some of them have outperformed the standard DRAM in terms of real estate or operation speed, but none of them has become a serious alternative demonstrating simultaneously low variability, immunity to cell disturbance issues and scalability [5].

We will review the recent developments in the 1T-DRAM arena, which are pointing to the architectural modification of standard MOS transistors for better control of the charge stored in the body of the device. Dedicated body, different doping polarities, underlapped gate regions or the introduction of SiGe layers are examples of various paths taken by 1T-DRAM research in recent years. We will discuss the merits, issues, and solutions for further optimization of these horizontal or vertical multi-body transistors that will eventually replace the DRAM.

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