The future of Si nanoelectronics

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Recently, CMOS downsizing has been accelerated very aggressively in both production and research, and beautiful transistor operation of several-nm gate length CMOS devices has been reported in conferences. However, many serious problems are expected for implementing small-geometry MOSFETs into large-scale integrated (LSI) circuits. It is still questionable whether we can successfully introduce deep sub-10 nm CMOS LSIs into market, because the problems expected at this moment – such as inadequate I_{ON}/I_{OFF} ratio and current drive, variation in the electrical characteristics, and concerns about the yield, reliability and manufacturing cost. Considering the above situation, we have conducted nano-CMOS studies to assess possible solutions to anticipated challenges. A major conclusion obtained is that aggressive introduction of new materials, processes, structures, and operating concepts is required to solve the problems of the nano-CMOS era. Especially, the thinning of the gate oxide is the bottleneck of the future downscaling, and thus, new materials and process technologies which enable a decrease in the equivalent oxide thickness value less than 0.5 nm are very important. Also, changing the material of source/drain from semiconductor to metal is necessary to suppress of the diffusion of the dopants and thus, ensure an effective channel length of less than several nm. Multi-gate structures such as fin, tri-gate, or nanowire are inevitable to suppress short-channel effects.

Unfortunately, there are no candidates among the so-called "beyond CMOS" new devices that can believably replace CMOS transistors of highly integrated circuits within 20 years. Thus, our opinion is that we need to still continue to develop CMOS-based transistors following the "more Moore" approach while investigating the "more than Moore" alternatives. The good news is that Si nanowire FETs have been found to have very promising characteristics with high I_{ON}/I_{OFF} ratio and current drive. Also, La-silicate high-κ gate insulator and Ni-silicide source/drain have been proven to be very promising candidates. This talk will present the future nano-CMOS technologies that will enable downsizing for next several generations.

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