Physics and design of nanoscale field effect diodes (FEDs) for memory and electrostatic discharge (ESD) applications

Dimitris E. Ioannou, Zakariae Chbili, Qiliang Li, Yang Yang, and Akram A. Salman
George Mason University and *Texas Instruments Inc., USA*

This research project combines the strengths of the thin capacitively coupled thyristor (TCCT) [1] with the strengths of the nanoscale field effect diode (FED) to design, fabricate and test new memory cells. The research is in response to the widely recognized urgent need for progress in memory technology, as abundantly demonstrated, for example, by the large number of dedicated technical sessions in recent IEEE-IEDM meetings. Field effect diodes involve demanding device physics and nanofabrication technology, and we explore their design space in order to establish the most appropriate structures and operation conditions for new types of SRAM, DRAM and NVM memory cells [2]. In addition, FED structures have shown promise and are further explored in this research project for ESD protection applications [3]. These two applications are characterized by different demands on the device properties: for memory applications, leakage control and small cell size drive the device design, whereas for ESD protection large forward breakdown voltage must be achieved.

The FED structure resembles a SOI *pin* diode to which two closely spaced narrow gates have been added. Its many advantages derive from the fact that by suitably biasing these (independent) gates, the FED can be operated as a *pin* diode or as a thyristor. We will discuss the relevant nanoscale FED device physics, which allows us to design a variety of FED memory cells and ESD protection devices, including multigate-SOI MOSFET and Fin-FET FEDs. These new cells are characterized by better gate control, faster operation and lower leakage power dissipation at reduced cell area. This better gate control of the FED also leads to higher current and higher breakdown voltage in ESD applications.

Our research is expected to have substantial broader impact in the quest for new devices for the "post CMOS" semiconductor industry era, as it introduces device structures with operational principles different from classical CMOS, while at the same time benefiting from the vast experience with silicon technology. These devices will make urgently needed contributions to semiconductor industry in two very important areas, namely memory cell technology and electrostatic discharge protection.

Support by NSF Grant ECCS-901236 is gratefully acknowledged.

1. F. Nemati and J. D. Plummer, *Tech. Dig. IEDM* (1999), p. 283; see also *www.t-ram.com*
2. Y. Yang, A. Gangopadhyay, Q. Li, and D. E. Ioannou, *Proc. ISDRS* (2009), art. 5378045; Z. Chbili, Y. Yang, Q. Li, and D. E. Ioannou, *Proc. ISDRS* (2011), art. 6135246.
3. A. A. Salman, S. G. Beebe, M. Eman, M. M. Pelella, and D. E. Ioannou, *Tech. Dig. IEDM* (2006), art. 4154406; Y. Yang, A. A. Salman, D. E. Ioannou, and S. G. Beebe, *Solid-State Electronics* **52**, 1482 (2008); and S. Cao, S. G. Beebe, A. A. Salman, M. M. Pelella, J.-H. Chun, and R. W. Dutton, *Proc. IEEE Intern. Rel. Physics Symp.* (2009), p. 594.