# A sharp-switching fully-depleted SOI device with high current drive 

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The downscaling of the MOSFET has been proceeding for several decades, enabling higher integration density, higher operation speed, and lower power consumption. However, the subthreshold swing (SS) of MOSFET is limited by the thermal diffusion to $S S \geq 60 \mathrm{mV} / \mathrm{dec}$ at room temperature. This imposes an eventual limit on the downscaling of supply voltage $V_{\mathrm{DD}}$.

Thus, sharp-switching devices, such as impact ionization MOS (I-MOS) and tunneling FET (TFET), are of great interests to achieve lower SS. Since the I-MOS operates with impact ionization, the required supply voltage $V_{\mathrm{DD}}$ must be several times the bandgap, which is not fully compatible with modern CMOS [1]. The TFET operates with band-to-band tunneling and while the fabrication and $V_{\mathrm{DD}}$ are typically CMOS-compatible, the on-state current $I_{\mathrm{ON}}$ has been disappointing lower than MOSFET values [2]. Other types of sharp switching devices are based on feedback between carrier flows and their injection barriers, such as feedback FET (FB-FET) [3] and field-effect diode (FED) [4]. The FB-FET achieves SS $\sim 0.35 \mathrm{mV} / \mathrm{dec}$ and $I_{\mathrm{ON}}>10 \mu \mathrm{~A} / \mu \mathrm{m}$ under reasonable $V_{\mathrm{DD}}$, but operates with surface charge storage $Q_{\mathrm{S}}$, which is difficult to control precisely. The FED needs no $Q_{\mathrm{s}}$, but requires the fabrication of two adjacent front gates, which is challenging.

In this work, we demonstrate a new sharp-switching device combining the asymmetrical TFET structure [3] with the feedback operation principle. The device has an undoped channel partially covered by a single front gate, with the injection barriers created by the front and back gates, see Fig. 1(a). Figure 1(b) compares the transfer characteristics to I-MOS [2], TFET [3], and FB-FET [4]. Our device exhibits sharp switching with large $I_{\mathrm{ON}}>500 \mu \mathrm{~A} / \mu \mathrm{m}$, and is well-suited for compact one-transistor memories.


Fig. 1. (a) Schematic view of the new device structure; (b) comparison with IMOS [2], TFET [3] and FBFET [4].

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