Top-down nanowires versus bottom-up for nanoelectronic applications

Thierry Baron
Laboratoire des Technologies de la Microélectronique–CNRS, Grenoble, France

Scaling down of semiconductor devices is the driving force for the development of new applications (mobile phone, memory cards, sensors …). The natural evolution of the fin-FET technology announced recently by Intel could employ nanowires (NWs) as channels in MOSFET technology. Nanowires could also find applications in other devices and particularly to add new functionalities in the integrated circuits (3D integration).

We will review and compare the different methods for nanowires fabrication, namely the top-down and the bottom-up approaches from the perspective of microelectronic integration. The advantages and remaining hurdles to achieve device integration containing nanowires will be discussed. The targeted devices include transistors, capacitors and sensors.

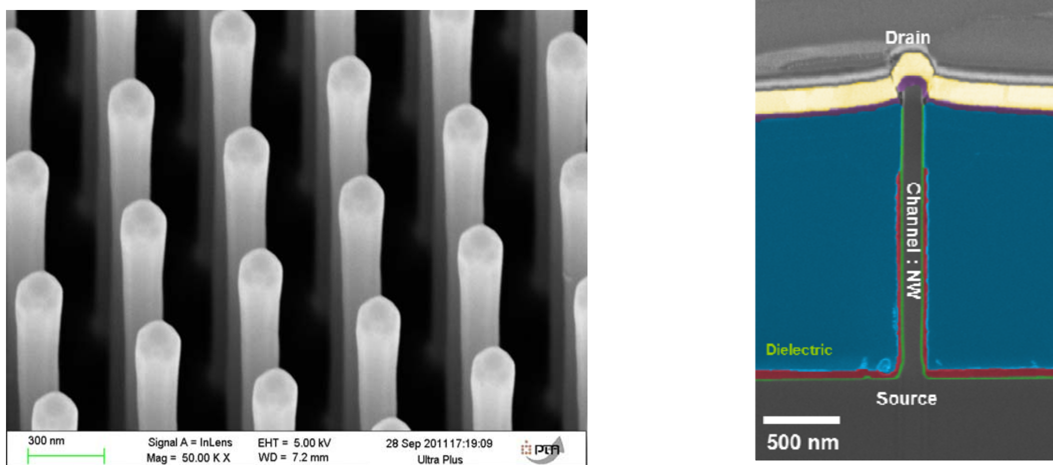

Fig. 1. Scanning electron micrograph of vertical NW array obtained by top-down approach (left, courtesy of Martin *et al.*) and an example of vertical integration of NWs for gate-all-around devices (right, from [1]).

Work done in collaboration with B. Salem, F. Bassani, L. Latu-Romain, M. Kogelschatz, C. Ternon, M. Martin (LTM), P. Gentile, N. Pauc (SiNAPS), T. Ernst (CEA-LETI), and PhD students A. Potié, G. Rosaz, P. Periwal, M. Ollivier, and Ph. Morel.

1. G. Rosaz, B. Salem, N. Pauc, A. Potié, P. Gentile, and T. Baron, *Appl. Phys. Lett*. **99**, 193107 (2011).