Simulation of self-heating effects in different SOI MOS architectures

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Self-heating effects (SHEs) are expected to become an increasing problem for future technological nodes, due to the use of new architectures such as silicon-on-insulator (SOI). Thin silicon layers have a much lower thermal conductivity than bulk silicon [1]; moreover, in SOI devices the channel is thermally insulated from the underlying substrate by a SiO_2 buried-oxide layer. All these aspects cause severe SHE, that detrimentally impacts the carrier mobility and therefore the saturation drain current I_{DS}.

We discuss SHE in different SOI architectures: *n*-channel planar single-gate (SG), double-gate (DG), and FinFET transistors, designed to have the same electrical isothermal characteristics, *e.g.* same threshold voltage, transconductance, and a good immunity from short-channel-effects (SCEs).

The DG and FinFET transistors feature the same silicon thickness ($t_{Si} = W_{fin} = 10$ nm) and gate length ($L_G = 50$ nm); as the SG device is strongly affected by SCE, we considered two different scenarios: $t_{Si} = 10$ nm and $L_G = 64$ nm, or $t_{Si} = 5$nm and $L_G = 50$ nm.

Our analysis used a commercial 3D electro-thermal simulator, with a temperature- and film thickness-dependent model for the silicon thermal conductivity adopted from [2]. As the standard drift-diffusion approach is unable to account for nonequilibrium phenomena in ultrashort devices, and therefore underestimates I_{DS}, the mobility parameters have been modified to match Monte Carlo-calculated I_{DS}-V_{DS} curves [3]. Different solutions for the thermal boundary conditions have been studied.

The simulations pointed out that the SHE detrimentally impacts the device performance, and it is dependent on the device structure. In particular, the thermal resistance due to the source/ drain access regions, as well as the ratio between the surface available for the heat dissipation through the buried oxide and the volume of the active region, change from a structure to another.

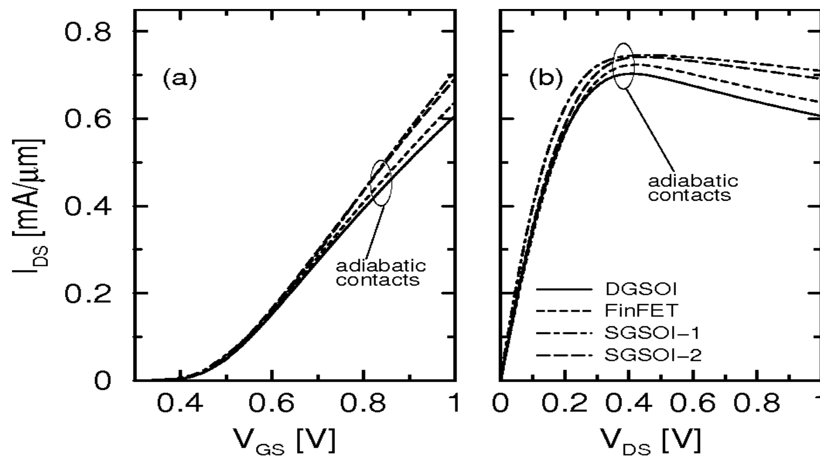

FIG. 1. Transfer characteristics at $V_D = 1.0$ V (a) and output characteristics at $V_G = 1.0$ V (b) calculated by 3D electro-thermal simulations; the gate and S/D contacts are treated as adiabatic.

1. E. Pop *et al.*, *Proc. IEEE* **94**, 1587 (2006).
2. W. Liu *et al.*, *IEEE Trans. Electron Dev*. **81**, 1868 (2006).
3. J. D. Bude, *Proc. SISPAD* (2000), pp. 23-26.