Nanoscale energetics: the looming power crisis and how to avoid it

James Burr
Sun Microsystems, USA

Molecules currently under consideration for doing digital work range in size from about 12 Å for a single RTD structure to 60x60 Å for a simple logic gate. While impressively small, it is conceivable that CMOS transistors could be built at this scale – 60 Å devices have already been reported. Just as it is unfair to assume there will never be a three-terminal molecular switch, it is also unfair to assume that silicon is somehow excluded from the nanocosm.

Now, suppose we did have 20 Å transistors and 20 Å wires. What would their properties be? It is possible to estimate performance and power dissipation at this scale using techniques proven for mesoscopic CMOS, and to apply these same techniques to proposed molecular electronic devices. The results are surprising . What emerges is that wires dissipate a *lot* of power. This is interesting since it is technology agnostic – the problem is probably worse for molecular electronics than for CMOS since the level of 3D integration is potentially much higher. This talk will show how to predict performance and power dissipation in CMOS technology, apply the technique to some proposed molecular logic circuits, and compare the results. The conclusions: 1) power and performance are dominated overwhelmingly by wire capacitance; 2) although shortening wires improves performance and reduces energy per function, it increases power density; and 3) molecular logic elements proposed to date are 10^3–10^6 times slower than nanoscale CMOS simply because they do not supply enough current to drive the wires required to connect them into real circuits. This has far-reaching implications for future directions in digital systems architectures, because switching speed will have to be greatly compromised to take advantage of a huge potential increase in functional density.