Collector-Controlled States and the Formation of Hot Electron Domains in Real-Space Transfer Transistors

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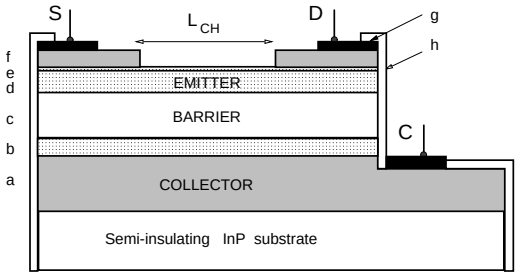
Introduction

The concept of real-space transfer[1] (RST) describes the process in which electrons in a narrow semiconductor layer, accelerated by an electric field parallel to the layer, acquire high average energy (become "hot") and then spill over an energy barrier into the adjacent layer. This principle underlies the operation of a three-terminal heterojunction device, called the charge injection transistor or CHINT.[2,3] Figure 1 shows the structure of this device, implemented in the InGaAs/InAlAs heterosystem, lattice-matched to InP. The emitter layer (*d*) has two contacts, *S* and *D*, and plays the role of a hot-electron cathode. The collector layer (*a*) is separated from the emitter by a potential barrier (*c*). Transistor action consists in the control of the injection current I_C by the voltage V_D, applied between *S* and *D*.

The structure shown in Fig. 1 and its variations have been employed in a series of experimental studies.[4,5] Typically, the onset of charge injection leads to highly non-linear effects, including a strong negative differential resistance (NDR) in the $I_D(V_D)$ dependence with sharp steps indicative of an internal switching and the formation of high-field domains. These instabilities arise due to a positive feedback between the RST and the heating electric field in the emitter channel. Significant progress in the understanding of these processes has been achieved[6] with the help of continuation modeling and transient device simulation.



a: 5000 Å InGaAs n^+ (Si:10^{19})
b: 500 Å InGaAs n^- (Si:10^{17})
c: 2000 Å InAlAs u
d 500 Å InGaAs n (Si:10^{16})
e: 25 Å InAlAs n^+ (Si:10^{19})
f: 200 Å InGaAs n^+ (Sn:10^{20})
g: 500 Å Ti / 1000 Å Au
h: Si_3N_4

Fig. 1. Cross-section of a real-space-transfer transistor implemented[4] in the $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ heterostructure lattice-matched to InP.
The epitaxially-grown heavily-doped cap layer *f*, forming the *S* and *D* contacts, is patterned lithographically with the help of the etch-stop layer *e*.

A number of functional applications have been contemplated based on the unique characteristics of three-terminal RST devices. Recently, the scope of such applications was expanded by our invention[7] of a new multiterminal device structure, called the NORAND. Its principle embodies the basic symmetry inherent in the charge injection by RST: the direction of the collector current is the same irrespective of the polarity of the heating voltage. The NORAND has three symmetric logic inputs and performs both the NOR and the AND logic functions − interchangeably in the course of the circuit operation. This operation has been demonstrated experimentally.[3] The invention of NORAND has focused our attention on the symmetry properties of RST transistors.

The basic CHINT structure is symmetric with respect to reflections in the midplane normal to channel. Hence states of the device at an external bias $[V_D, V_C]$ are related to those at $[-V_D, (V_C - V_D)]$. In particular, states at $V_D = 0$ must either be symmetric or possess broken-symmetry partners. An unexpected recent discovery[6] is the existence of a number of such states, some of which are not only stationary but also *stable* with respect to small perturbations. In these "anomalous" states,[8] the electron heating is due to the fringing field from the collector electrode. Our study shows that the formation of hot-electron domains at $V_D > 0$ represents a transition to a collector-controlled state that is continuously related to one of the anomalous states at $V_D = 0$. Understanding of these processes may stimulate the invention of novel RST devices with an enhanced functionality.

The study of hot-electron domains in RST transistors is also important for understanding the device limitations. Switching of the electron-heating control to the collector restricts the range where CHINT can be used as a linear amplifier. The frequency performance of CHINT in its usual mode is believed to be limited only by the time of flight of hot electrons over high-field regions of the device, i.e., over distances of order the barrier-layer thickness. For the device in Fig. 1, the transit time can be estimated to be of order 2-3 ps, which sets the upper limit for unity-gain cutoff frequencies at around 50 GHz. The cutoff frequencies, extrapolated from the microwave measurements of scattering parameters in this structure,[5] were 40 Ghz for both the current and the power gain. The ultimate speed performance can be achieved with an inverted CHINT structure in which the collector is the top layer.[9] This allows the reduction of the parasitic drain-collector capacitance and therefore the use of narrower barriers. With sufficiently narrow barriers, the CHINT can be expected to outperform a field-effect transistor of similar geometry (the RST collector corresponding to the FET gate, etc.) because the small-signal performance of CHINT is not limited by the time of flight between the source and the drain.[10] However, the domain formation itself seems to be a longer, FET-like, process.

Results of our numerical simulation of the hot-electron transport in a three-terminal RST structure are reviewed below. Details of the program and computational methods are described elsewhere[11, 12] and further discussed in the accompanying paper.[13]

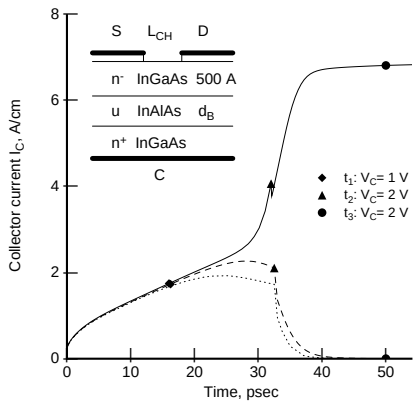
Symmetry breaking and the formation of hot-electron domains

The presented results correspond to a specific choice of an InGaAs/InAlAs heterostructure, lattice-matched to InP, as in Fig. 1. The height of $In_{.52}Al_{.48}As$ barrier, separating the $In_{.53}Ga_{.47}As$ channel and collector layers, is taken equal 0.5 eV. Models for the local hot-electron mobility $\mu(T_e)$ and the energy relaxation time $\tau_E(T_e)$ are chosen so that in a uniform electric field, F, one obtains a given velocity-field $v(F)$ and temperature-field $T_e(F)$ characteristics. The current density is assumed to consist of a drift ($en\mu\vec{\nabla}V$) and a thermodiffusion ($\mu\vec{\nabla}[nkT_e]$) components, where n is the electron concentration and V the electrostatic potential. The quasi-Fermi level and T_e are assumed continuous at all heterostructure interfaces; this implies that the RST current density is thermionic and included self-consistently in the continuity equations. In order to disentangle our results from NDR effects arising from the momentum-space transfer, we have chosen the $v(F)$ dependence in a simple form $v = \mu_0 F\,[1+(\mu_0 F/v_{sat})^2]^{-1/2}$, parameterized by the low-field room-temperature mobility μ_0 and the saturation velocity v_{sat}. Our results remain qualitatively similar for a more realistic $v(F)$ model, appropriate for InGaAs. To further simplify the discussion, we have excluded the phenomena of impact ionization and tunneling. We have performed a number of simulations, varying the geometry (channel length L_{CH} and barrier thickness d_B), the transport parameter v_{sat}, and the external bias conditions.

Fig. 2 illustrates a time-dependent simulation of a device with $L_{CH} = 5\,\mu m$ and $d_B = 0.2\,\mu m$. Both S and D electrodes are kept grounded, while V_C is linearly ramped from 0 to $V_C = 2\,V$. Depending on the ramping time τ the device settles in one of two states: for $\tau > \tau_{cr}$ it is the normal[12] state, whereas for $\tau < \tau_{cr}$ the steady state carries a large RST current (Fig. 2a). The

critical ramping speed is determined by the rate at which the increasing fringing field (Fig. 2b) is screened by channel electrons. The value of $\tau_{cr} \simeq 32.3\,\text{ps}$ roughly corresponds to the time of electron travel from S and D contacts to the middle of the channel.

The anomalous state at $V_D = 0$ exists only for a sufficiently high V_C, and the value of V_C^{cr}, below which this state disappears, depends on the device geometry and v_{sat}. The value of V_C^{cr} is sharply defined, and for the ramp end voltage V above V_C^{cr}, one has $\tau_{cr} \propto V$ to a good approximation, cf. Fig. 3a. This indicates that the relevant critical parameter is the displacement current ($\propto dV/dt$), which should be compared to a transient current ($\propto v_{sat}$)



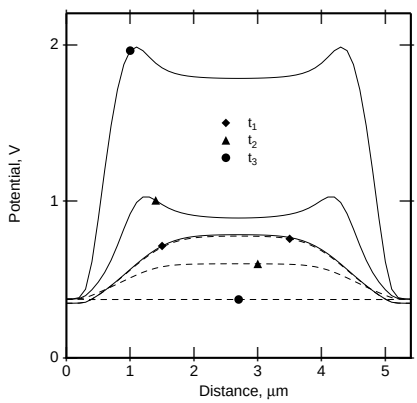
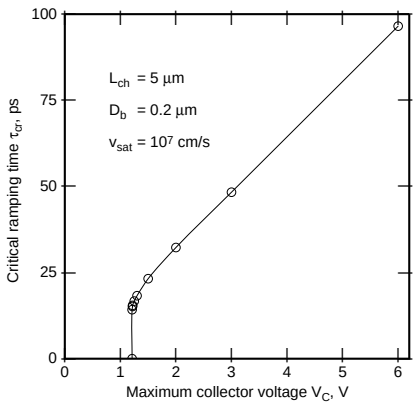


Fig. 2. Time-dependent simulation of a real-space transfer transistor with $L_{CH} = 5\,\mu\text{m}$, $d_B = 0.2\,\mu\text{m}$, and $v_{sat} = 10^7\,\text{cm/s}$. The collector voltage is ramped linearly from $V_C = 0$ at $t = 0$ to $V = 2\,\text{V}$ at $t = \tau$. The results are plotted for two situations: $\tau = 32.0\,\text{ps} < \tau_{cr}$ (solid lines) and $\tau = 32.5\,\text{ps} > \tau_{cr}$ (dashed lines).
(a), *top figure*: Collector current $I_C(t)$; inset shows cross-section of the device structure. Dotted curve corresponds to the absence of a RST (pure displacement current); it is obtained by artificially increasing the barrier height.
(b), *bottom figure*: Potential distribution $V(x)$ along the channel at selected times.



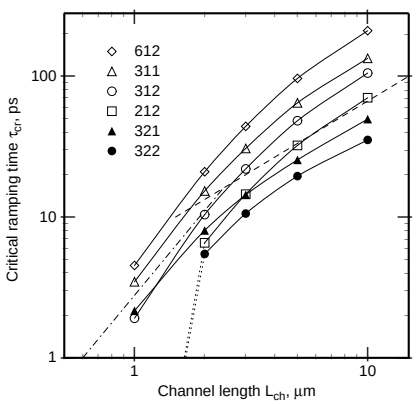


Fig. 3. Critical ramping speed for the formation of a stable anomalous stable state at $V_D = 0$. The collector bias is ramped linearly $V_C = 0 \to V$ in the time interval τ. For $\tau > \tau_{cr}$ the device settles in the normal state, for $\tau < \tau_{cr}$ in the anomalous state **d** (cf. Fig. 4).
(a), *top figure*: The dependence of τ_{cr} on the endramp voltage for a $5\,\mu\text{m}$ device. The value of V_C^{cr} for this device is 1.211 V.
(b), *bottom figure*: The curve labels *VSD* indicate the endramp voltage (V) in volts, the saturated velocity (S) in $10^7\,\text{cm/s}$ and the barrier thickness (D) in 1000 Å. The dashed and stipple lines indicate linear and quadratic dependences, respectively.

associated with electron screening processes in the emitter. The values of τ_{cr}, determined to within 0.1 ps, are plotted in Fig. 3b against the emitter channel length L_{CH} for different assumed values of v_{sat}, barrier thicknesses, and ramp end voltages V. For short L_{CH} the dependence $\tau_{cr}(L_{CH})$ is approximately quadratic, and for long L_{CH} the dependence is linear.

Starting from the two stationary states at $V_D = 0$, we were able to determine the characteristics $I_D(V_D)$ and $I_C(V_D)$ at a fixed collector voltage $V_C = 2\,V$ relative to the S electrode. Using a predictor-corrector continuation method[11], we can trace arbitrarily shaped, connected components of the characteristic, starting from any established state within each component. The curves in Fig. 4 correspond to the locus of points in the (V_D, I_D) plane for which the device has a steady state at a given V_C. To our knowledge, the displayed $I_D(V_D)$ dependence represents the first example of a multiply connected current-voltage characteristic. Any transition between disconnected components of the graph requires a global redistribution of the state fields corresponding to the formation or repositioning of high-field, high-temperature domains in the structure. Such a redistribution, reminiscent of a phase transition, is forced as V_D increases beyond the rightmost point (**k**) of the bounded graph component.

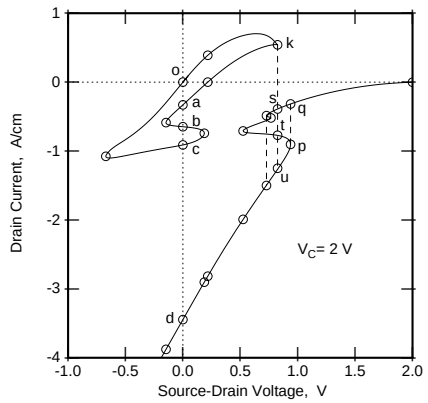


Fig. 4. Current-voltage characteristics obtained by the continuation method.

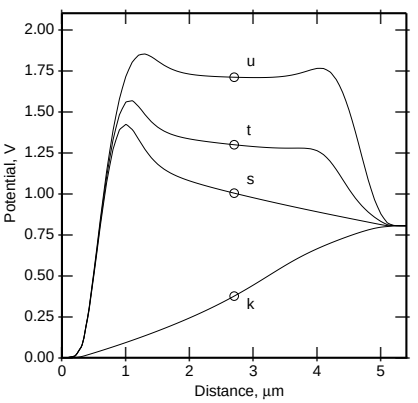


Fig. 5. The channel potential profile $V(x)$ in different CHINT states at the same external bias ($V_C = 2\,V$, $V_D = 0.8246\,V$).

The potential profiles $V(x)$ along the channel − before and after the transition − are shown in Fig. 5. Of the three collector-controlled states, **s**, **t**, and **u**, corresponding to the same ($V_D \simeq 0.82\,V$) external bias as the state **k**, two (**s** and **u**) are stable. The actual transition occurs into the state **u** which has the highest value of the collector current. This has been ascertained by a time-dependent simulation in which the initial state **k** was perturbed by a small step $V_D(\mathbf{k}) \to V_D(\mathbf{k}) + \delta V_D$. The hot-electron domains in the state **u** are characterized by a strong field concentration, accompanied by a dramatic rise in T_e. The electron concentration in the domain is depleted so that the collector field remains unscreened and the local potential goes below that of the drain, resulting in a negative I_D. All states on the **p** − **u** − **d** branch of the collector-controlled component are similar to **u** and perfectly stable. This indicates that state **d** (which we had first found in rapid ramping of V_C at $V_D = 0$, cf. Fig. 2) is experimentally accessible by a quasi-static variation of V_D at fixed V_C. The existence of a stable anomalous state **d** is obviously a necessary (though insufficient) condition for the multiply-connected topology of the $I_D(V_D)$ characteristic. As discussed above, it results when the competition between RST and screening of the fringing collector field is resolved in favor of RST. Precisely when this happens depends on the transport parameters assumed and the device geometry.

In addition to the normal state **o** and the anomalous state **d**, Fig. 4 reveals three other anomalous states (**a**, **b**, and **c**) at $V_D = 0$. The profiles $V(x)$ along the channel in these states are shown in Fig. 6. It is clear that because of the non-linear nature of the problem, the actual

stationary states may not transform according to irreducible representations of the symmetry group of the equations governing the device behavior at $V_D = 0$. The distribution of internal fields in the anomalous states is either fully symmetric or these states form a set of partners and transform into one another under the symmetry operations. Thus, states **a** and **c** under reflection transform into each other, even though the group has only one-dimensional linear representations. On the other hand, states **o**, **b**, and **d** are symmetric. Biasing the *D* electrode with respect to *S* breaks the reflection symmetry and allows a continuous transformation between states of different symmetry on the loop. This type of analysis is likely to prove very potent with devices of more complicated symmetry, such as the NORAND, whose symmetry group is C_{3v}.

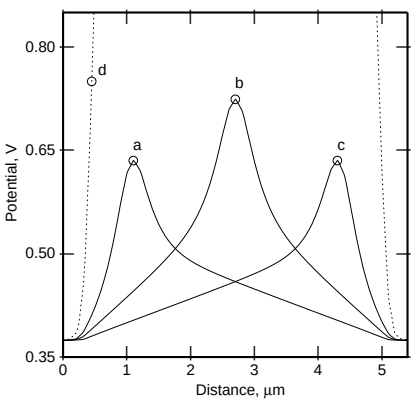
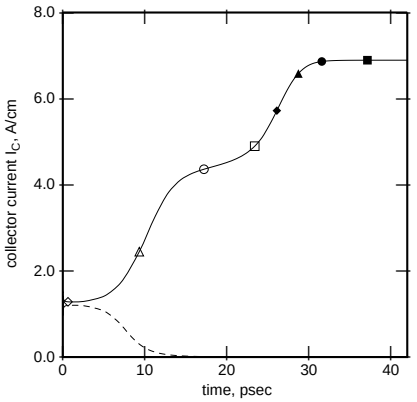


Fig. 6 (above). The channel potential in the four anomalous states at $V_D = 0$.



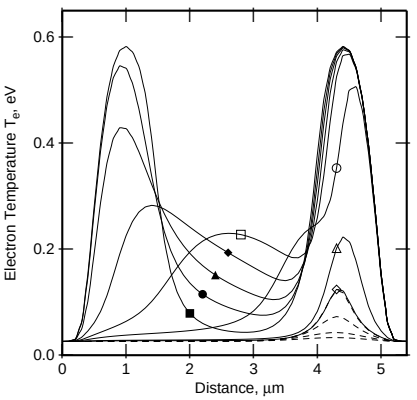


Fig. 7 (right). Evolution of the non-stationary states $\mathbf{c}_+$ (solid lines) and $\mathbf{c}_-$ (dashed lines) at $V_D = 0$. Time dependence of the injection current is shown in *the top figure*; symbols mark the selected times in the evolution, at which the electron temperature profiles are plotted in *the bottom figure*. The "plateau" in the $I_C(t)$ dependence near $t = 20$ ps evidently corresponds to the situation when a fully-developed hot-electron domain exists already near *D* but not yet near the *S* electrode.

Of the five states at $V_D = 0$ and $V_C = 2$ V, only two (**o** and **d**) are stable with respect to small perturbations. This has been ascertained by following the evolution of states in the vicinity of the steady states at $V_D = 0$. In these simulations, Fig. 7, the initial states $\mathbf{a}_\pm$, $\mathbf{b}_\pm$, and $\mathbf{c}_\pm$ have been assumed to coincide with a state on the loop displaced from **a**, **b**, and **c**, respectively, by an infinitesimal voltage $\delta V_D = \pm 10$ mV. Even though these states are virtually indistinguishable from the corresponding stationary ones, we found that $\mathbf{a}_+$, $\mathbf{b}_-$, and $\mathbf{c}_-$ evolved into **o**, while $\mathbf{a}_-$, $\mathbf{b}_+$, and $\mathbf{c}_+$ into **d**. The instability of states **a** and **c** is associated with a NDR in the $I_C(V_C)$ dependence, $\partial I_C/\partial V_C < 0$, and that of **b** with both $\partial I_C/\partial V_C < 0$ and $\partial I_D/\partial V_D < 0$. All these instabilities develop on a rapid time scale, corresponding to the electron travel over the distances of the order of the domain size. They result in either the formation (repositioning) of a hot-electron domain, or its complete quench due to the screening by channel electrons.

Conclusion

We have found that RST transistors possess complicated − often multiply-connected − *IV* characteristics. Application of a sufficiently high V_D forces a switching transition, accompanied by the formation of a hot electron domain. Physically, the domains form when the finite supply rate of electrons to a "hot spot" is exceeded by the RST flux from that spot. The depleted domains unscreen the fringing field ("normally"[8] screened by channel electrons) and the RST becomes collector controlled.

Potential applications of RST transistors are likely to be based on their peculiar symmetry with respect to the heating field polarity. The same symmetry shows up in the analysis of the hot-electron domain formation. States of a multiterminal RST device under general bias are "adiabatically" connected to the anomalous states of the symmetric configuration at $V_D = 0$. We believe the phenomena that occur at $V_D = 0$ capture the essential physics associated with the RST domains in general.

All steady-state results discussed above correspond to a fixed bias $V_C = 2\,\mathrm{V}$. Slicing the $I_D(V_D, V_C)$ surface at different V_C, we find $I_D(V_D)$ curves of different topologies.[13] The internal fields evolve smoothly along a connected $I_D(V_D)$ trajectory and do not signal the approach of a switching transition. Phase-space mappings successfully give the global type of information. Moreover, they usually give an unerring guess as to the *stability* of a given state.

References

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