Charge injection logic

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The charge injection transistor is a semiconductor device based on transfer of hot electrons between separately contacted conducting layers. The nature of hot-electron injection by the real-space transfer allows the implementation of novel circuit elements. In particular, we propose a multiterminal single-device structure that works as a functional element with three logic inputs X_j ($j = 1,2,3$) and one output equal to $(X_1 \cap X_2 \cap X_3) \cup (\overline{X}_1 \cap \overline{X}_2 \cap \overline{X}_3)$. This device, called the NORAND, can perform both as a NOR(X_1,X_2) and as an AND(X_1,X_2) element, reprogrammable electrically by changing the X_3 input. The operation of NORAND with logic gain is demonstrated experimentally by an equivalent circuit connection of discrete charge injection transistors implemented within InGaAs/InAlAs on InP technology.

The charge injection transistor or CHINT[1] is a three-terminal semiconductor device based on the effect of real-space transfer (RST) of hot electrons between conducting layers, separated by a potential barrier and contacted independently. One of these layers, referred to as the channel, has two surface contacts, source (S) and drain (D). Application of a source-to-drain bias leads to a heating of channel electrons and charge injection into the second conducting layer. The channel acts as a hot-electron emitter and the second conducting layer as a collector (C). The device shows a strong negative differential resistance (NDR) in the source-drain characteristic and an efficient control of the injection current by the drain voltage. Three-terminal RST devices have been extensively investigated, both experimentally[2-11] and theoretically,[12-14] and a number of their logic applications have been contemplated.[1-4,12]

In this letter, a new multiterminal RST device structure is proposed, and its generic use in logic circuits is demonstrated experimentally. The idea is based on the symmetric nature of charge injection[1] with respect to the polarity of the source-drain voltage V_{SD}. Consider the typical injection characteristics of a charge injection transistor, Fig. 1. The device structure used in this work for illustrative purposes is similar to that presented in our earlier report,[10] with some modifications resulting in an improved device performance.[15] Figure 1(a) shows the dependences I_C vs V_{SD} at several collector voltages V_C. Curves of this type were originally reported[1] for cryogenic temperatures and used to determine the effective electron temperature T_e in the emitting channel. The slight asymmetry of the injection curves is due to the variation in the gating action of the collector at $V_{SD} < 0$. The fact that the injected collector current I_C does not depend on which of the two surface terminals, S or D, is chosen to be the source, allows the implementation of devices in which the role of a particular terminal in the circuit is not defined by the layout.

The room-temperature CHINT characteristics I_C vs V_C at several heating voltages V_{SD} are shown in Fig. 1(b) along with a load curve corresponding to a resistor R in the collector circuit. Consider the circuit illustrated in Fig. 1(b) not as a transistor but as a logic element with inputs S and D corresponding to the biases on the S and D electrodes, respectively. The point to note is that the logic function OUT(S,D) represents an exclusive NOR, since OUT is high when I_C is low (no RST) and OUT is low when the injection current is flowing. The latter situation results only when the voltages S and D are sufficiently different.

Figure 2 illustrates a schematic diagram of the proposed logic element NORAND which has three logic input X_j ($j = 1,2,3$) and one output OUT, connected as in Fig. 1(b). Which of the X_j will serve as a source and which as a drain is determined only at the time when a particular logic operation is performed. The value of OUT is high (logic 1) is only when all three X_j's have the same value (high or low). All the other six possible logic input configurations lead to the same high injection current resulting from hot-electron emitters formed in two of the three channels, X_{3-1}, X_{1-2}, and X_{2-3}. Three of these configurations correspond to the presence of two sources and one drain, the other three to one source and two drains. It is easy to see that the logic function OUT ($\{X_j\}$) is given by

$$\text{OUT}(X_1,X_2,X_3) = (X_1 \cap X_2 \cap X_3) \cup (\overline{X}_1 \cap \overline{X}_2 \cap \overline{X}_3) \,,$$

where the symbols $\cap$, $\cup$, and $\overline{A}$ stand for logic functions AND, OR, and NOTA, respectively. The truth table of the NORAND is as follows:

	I		II		III		IV	
X_1:	0	0	1	1	0	0	1	1
X_2:	0	1	0	1	0	1	0	1
X_3:	0	0	0	0	1	1	1	1
OUT:	1	0	0	0	0	0	0	1
	$\overline{X_1 \cup X_2}$		(NOR)		$X_1 \cap X_2$		(AND)	

We see that the NORAND operates as a NOR (X_1,X_2) when the input to X_3 is *low*, and as an AND (X_1,X_2) when X_3 is *high*. It is clear that the threefold symmetry of the device ensures that the injection current has the same value in all the six states corresponding to logic OUT $= 0$. One can achieve a similar effect without an exact threefold symmetry, e.g., with a "cylindrically" symmetric arrangement of the $\{X_j\}$ electrodes, cf. the bottom part of Fig. 2.

To illustrate the operation of NORAND, we have assembled a circuit consisting of three discrete CHINT devices
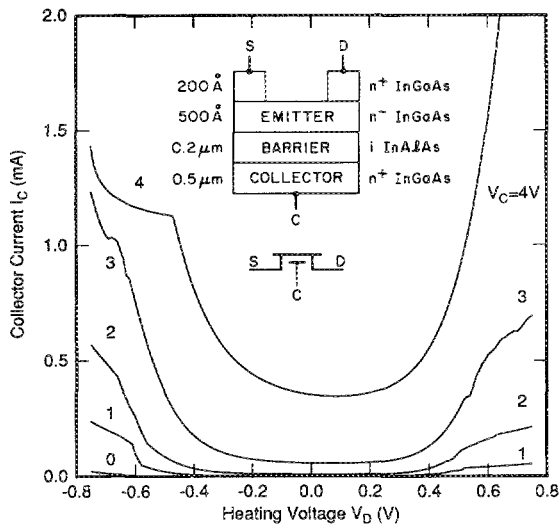
(a)
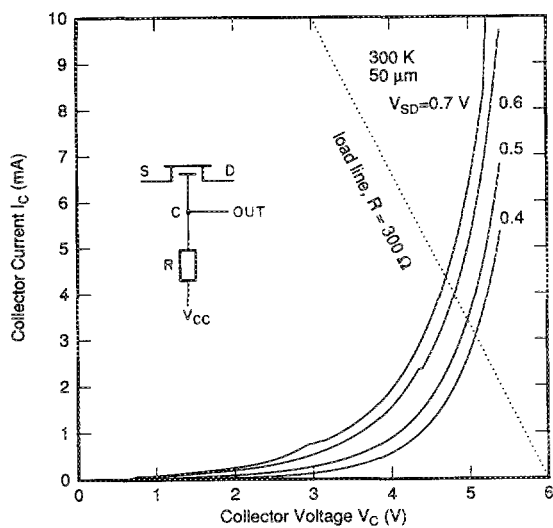
(b)

FIG. 1. (a) Charge injection curves at room temperature. Inset shows schematic cross section of the CHINT device structure and its circuit symbol used in this work. (b) Loading diagram of a charge injection transistor. For the resistor $R = 300\ \Omega$, the gain in the transitions along the load line is $\Delta\text{OUT}/\Delta V_{\text{SD}} \approx 1.5$.

with similar characteristics. In order to have a meaningful demonstration it is imperative that the device should operate with a logic gain. In switching a single device, like in Fig. 1(b), the gain equals $\overline{g}_m R$, where R is the load resistance and $\overline{g}_m$ the average transconductance in the logic transition. The transconductance g_m in CHINT is defined as the slope of the I_C vs V_{SD} characteristic $g_m \equiv \partial I_C/\partial V_D$ at constant V_C. At sufficiently high collector biases, g_m can reach very high values in a narrow range of V_D near the peak of the drain current.[15] However, because of the unavoidable slight differences between the devices it was inconvenient to operate within the narrow range of high g_m. Another difficulty was associated with the fact that each emitting channel, X_{i-j}, $i, j = 1,2,3$, should, ideally, be stable against oscillations in the input circuit, i.e., the logic state corresponding to a *high* value of $|X_i - X_j|$ should be out-
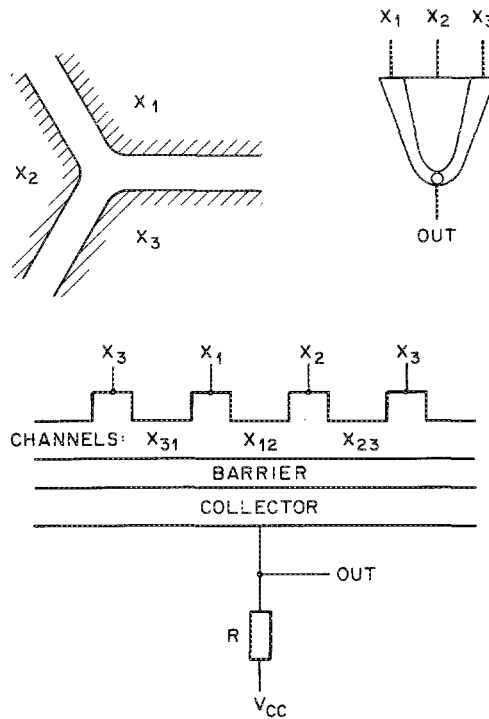

FIG. 2. Schematic layout of input electrodes in a NORAND logic element. Figure in the top left corner shows a symmetric arrangement of three identical channels, X_{3-1}, X_{1-2}, and X_{2-3}. By symmetry, one has the same hot-electron injection for any of the six states of binary input in which at least one of the three X_j's is different from the other two. The bottom figure shows the schematic cross section of an asymmetric layout. One of the electrodes is physically (but not logically) split, resulting in a "periodic" boundary condition, equivalent to the threefold rotational symmetry of the top left figure. Figure on the top right shows a proposed circuit symbol for the NORAND.

side the NDR region of the $I_D(V_D)$ characteristic. Experimentally, at high V_C the NDR region typically spans about 1.5 to 3 V. This feature is undesirable because it implies that in order to obtain a voltage gain, one would have to use a high load resistance. However, the wide extent of the unstable region appears to be related to the interaction between the active device and the reactive impedances of an external circuit. The NDR region becomes narrower for devices with smaller channel widths.

For the purpose of illustration, we can ensure the circuit stability by operating the switch in a range of relatively low $\overline{g}_m$ and employing a high-impedance load, as illustrated by the dotted line in Fig. 3 (a). This load line was obtained with the help of a transistor used as a nearly constant current source; see the inset to Fig. 3(a). The resultant functional characteristics of the NORAND are illustrated by four oscilloscope traces in Fig. 3(b). The two traces on the left correspond to $X_3 = 0$ and illustrate the operation of NOR(X_1,X_2); the traces on the right correspond to $X_3 = 4$ V and the operation of AND(X_1,X_2). The order of traces agrees with that in the NORAND truth table, e.g., the bottom trace on the right illustrates the last two columns of the table.

In order that a logic device could be used in integrated circuits, it is necessary that its input and output voltages be
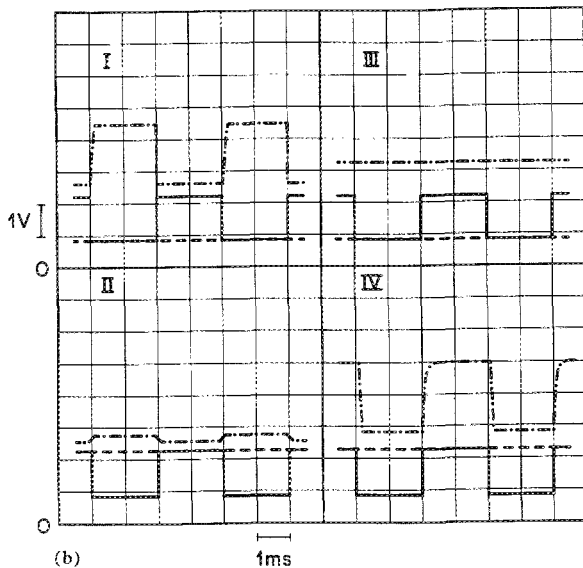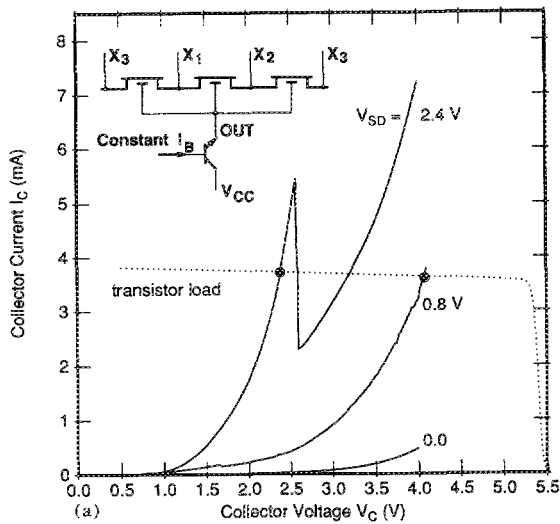
FIG. 3. Experimental illustration of the room-temperature operation of a NORAND element assembled from three discrete CHINT devices with similar characteristics. (a) Characteristics of one of the devices employed in the range of switching operation. Dotted line indicates the constant-current load ($I_C \approx 3.7$ mA) used in the demonstration. The circuit connection is shown schematically in the inset. (b) Oscilloscope traces of the NORAND response function at $V_{CC} = 5.5$ V. Dashed lines correspond to X_1, solid lines to X_2, and stippled lines to OUT. Traces I and II were obtained with $X_3 = 0$; traces III and IV correspond to $X_3 = 4$ V. Each quadrant in the figure illustrates two columns of the NORAND truth table with the roman numerals corresponding to those in the table. All traces refer to a common origin in each of the four quadrants.

consistent. As Fig. 3(b) suggests, in the case of NORAND this may require an additional level-shifting circuitry. In principle, this would not be a necessary requirement if only the NOR part of the NORAND truth table were to be employed. In the NOR configuration, the device has a well-defined ground level, and a consistent range of input-output characteristics can be found, as we have ascertained experimentally. On the other hand, in the AND configuration the low-OUT voltage must be higher than the lowest of the input voltages. In an optimized device, this difference can be made small, but since it would still accumulate after several stages, the level shifting will be mandatory. Further discussion of this interesting point will be made elsewhere

in the context of a specific application. Of course, it is well known that all logic functions can be implemented on the basis of a NOR element alone.

The functional element proposed in this work departs radically from all previously contemplated uses for multi-terminal RST devices.[16] At the same time, it represents a natural embodiment of the essence of hot-electron injection by the RST. Compared to all existing logic families, the NORAND offers a considerable economy in the layout of basic functional elements. Moreover, it promises faster operation of these elements, since the entire function is implemented within one gate delay of a high-speed transistor. The speed of charge injection transistors is discussed in Ref. 16, Sec. 7.4.5. The present generation of InGaAs/InAlAs-on-InP devices show a promising microwave performance.[17]

The demonstrated fact that the NORAND element can perform both AND and NOR functions, and is reprogrammable in the course of computation, represents an important and natural property of charge injection logic.

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[15] Thus, the peak-to-valley ratio of NDR in the I_D characteristic now routinely exceeds 1000 at room temperature, and the transconductance exceeds 20 S per millimeter of channel width. Molecular beam epitaxial growth sequence and subsequent processing of this device structure has been described separately in a study of its static current-voltage characteristics, see P. M. Mensz, P. A. Garbinski, A. Y. Cho, D. L. Sivco, and S. Luryi, Appl. Phys. Lett. 57 (to be published, 1990).

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[17] As evidenced by the small-signal current gain h_{21} and the maximum available gain (MAG), calculated from the measured S parameters [P. M. Mensz, H. Schumacher, P. A. Garbinski, A. Y. Cho, D. L. Sivco, and S. Luryi (1990 IEDM Technical Digest)]. The unity-gain frequency for both h_{21} and MAG was observed to exceed 25 GHz in a wide range of bias conditions.

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