This paper will discuss the mechanisms, the data relating to each effect and the implications for several different types of devices.

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VA-1 An Indium Phosphide MISFET Integrated Circuit Technology—D. K. Kinell, Lockheed Microelectronics Center, Sunnyvale, CA.

This paper reports on progress made towards achieving an InP based MIS integrated circuit technology. With the advent of DC stable, high transconductance InP MIS enhancement and depletion transistors,[1] it is possible to consider implementing this technology into high performance integrated circuit designs.[2] The high saturation velocity of electrons in InP as compared to silicon and gallium arsenide is the reason for the interest in this technology and is thus attractive as a candidate for high speed digital integrated circuits.

We have designed a test mask set for evaluation of InP MIS integrated circuits. The design includes test devices of 1.5 micron gate lengths for enhancement and depletion mode InP transistors. Logic inverters with different geometric ratios are also included in the design. Finally, 15 stage ring oscillators for evaluating speed performance are incorporated in the test circuit.

The process starts with iron-doped semi-insulating InP substrates. Enhancement devices are fabricated without a channel implant whereas depletion devices require a light silicon implantation. Source and drain regions are also implanted with silicon to a $5 \times 10^3/cm^2$ level. Annealing of the implantations are performed with a capping technique at 715°C using a phosphorus doped S_iO_2 cap. The S_iO_2 gate insulator is deposited at 240°C after Au-Ge/Pt ohmic metallization. Gate metal and circuit interconnection is achieved with an aluminum lift-off process.

This presentation also includes current fabrication process limited constraints. Lack of a suitable self-alignment structure places geometric as well as speed limitations on the InP MISFET technology. Also to be discussed are other potential problem areas such as surface inversion or electron accumulation between devices leading to leakage current problems. Potential solutions will be outlined.

Finally, results of fabricated devices will be presented. Enhancement devices exhibit maximum transconductances in the range of 60 ms/mm and depletion devices were fabricated with higher transconductances in the range of 70 ms/mm. Functional InP logic inverters and 15 stage ring oscillators have been fabricated. Propagation delays as low as 170 ps were obtained.

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[2]L. Messick, "A High Speed Monolithic InP MISFET Integrated Logic Inverter," *IEEE Transaction on Electron Devices*, vol. ED-28, No. 2, Feb. 1981.

VA-2 Charge Injection Over Barriers in Unipolar Semiconductor Structures—S. Luryi and R. F. Kazarinov, Bell Laboratories, Murray Hill, NJ 07974.

Our purpose is to discuss the phenomenon of charge injection (CI) in unipolar semiconductor structures. By CI we mean the thermionic emission of electrons over a potential barrier whose height is *efficiently* controlled by external voltage. CI is known to occur in forward-biased Schottky diodes (SD) where electrons are injected into a metal. However, because of the large concentration of electrons in the latter, the injected charge produces no tangible effect on the conductivity near the boundary. No CI into the semiconductor occurs in a reverse-biased SD (neglecting a small effect of image-force lowering) and current is limited by thermionic emission over a barrier of fixed height. Similarly, in all-

semiconductor analogs of the SD such as camel diodes[1] and n-n heterojunctions,[2] injection takes place only in the forward-bias regime.

A triangular barrier (TB) structure with finite slopes on both sides possesses a fundamentally new feature: CI in both directions. Diodes based on such barriers have been recently fabricated by MBE using either variable-gap[3] or modulation-doped[4] semiconductors. The IV characteristics of TBs show exponential growth in both directions and for a sufficiently asymmetrical TB rectification was observed. We report here a theory of the CI over TBs giving an exact analytic expression for the IV characteristics which agrees with experiment. The ideality factor for the exponential dependence is calculated as a function of the TB geometry and doping profile. At high current densities the theory predicts saturation of the exponential growth and transition to a linear IV characteristic. This behavior is due to i) slowing down of the effective diffusion velocity on the uphill slope of the TB, and ii) screening of the applied field by the mobile charge on the downhill slope. Which of these two effects is more important depends on the TB geometry and the material. The first effect is expected to be of importance in diodes based on GaAs, whereas in silicon, because of its larger Richardson constant, the second effect should dominate the saturation behavior. For diodes of similar geometry and doping profile the charge injection regime extends to higher currents in Si than in GaAs. Analogy with subthreshold characteristics of FET as well as device applications of TB structures will be discussed.

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[2]A. Chandra and L. F. Eastman, *Electron. Lett.*, vol. 15, 91, 1979.

[3]C. L. Allyn, A. C. Gossard, and W. Wiegmann, *Appl. Phys. Lett.*, vol. 36, 373, 1980.

[4]R. J. Malik, K. Board, C. E. C. Wood, L. F. Eastman, T. R. AuCoin, and R. L. Ross, *Electron Lett.*, vol. 16, 836, 1980.

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VA-3 Novel MIcrowave Medium Power GaAs MESFET With Schottky Drain—D. Meignant, Laboratoires d'Electronique et de Physique Appliquée 3, avenue Descartes, 94450 Limeil-Brévannes, France.

This paper describes a new microwave GaAs MESFET having a Schottky drain and a submicron recessed gate.

It is now clear that in order to obtain the highest output power performance, high source to drain and drain to gate breakdown voltages are required.

It is well known that the use of a recessed gate increases the source drain breakdown voltage and moreover increases the gain of the device, but does not affect the drain to gate breakdown voltage.

In order to increase this voltage, we propose to use a Schottky drain.[1]

This Schottky drain should lead to improvements in drain to gate breakdown voltage because a Schottky diode prevents the minority carrier injection in the active layer and also the current in the drain region should be more uniform compared to that of a standard ohmic contact.

The recessed gate is realised by self-alignment from drain to source. In order to fabricate a submicron gate without a mask of the same or even smaller dimensions that the gate length, we have used a novel technique involving the use of one sided under-etch of the drain metallisation.

Using this technique, medium power microwave FETs have been fabricated with gate lengths as small as .5 μm.

The drain metallisation was WTi, the source was AuGe/Ni alloyed at 470°C and the gate was Ti/Pt/Au.

Typical results for GaAs FETs (.8 μm gate length, and 600 μm gate width) were $I_{DSS} = 160$ mA, $g_m = 70$ mA/V and the breakdown voltage between gate and drain was in excess of 25 Volts.