subject: **Anomalous Temperature Dependence of Current-Voltage Characteristics in AlGaAs/W/GaAs Diode Structures with Floating Metal Layers**
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TECHNICAL MEMORANDUM

Diode current-voltage characteristics normally result from a classic case of thermionic emission over a barrier.[1,2] The exponential rise of current with temperature has been one of the classic phenomena taught in schools and is used thermometrically. In this paper we report observations on simple structures which exhibit clear diode characteristics at room temperature but which have a monotonic *increase* of current passed at a given voltage as temperature is *reduced.* In some structures over four thousand times as much current will flow at 30K than at 300K. We attribute this phenomenon to an internal transistor action in the devices.

The structures which exhibit this unusual effect are GaAs/W/GaAs and AlGaAs/W/GaAs structures with thin $\lesssim$ 10 nm porous metal layers embedded in single crystal III-V material. The layers were fabricated by an *in situ* Molecular Beam Epitaxy process which has been described previously.[3,4] Three samples showing this effect were made, all grown on n^+ GaAs substrates. Sample 1 has a 1 μm GaAs buffer, a nominal 10 nm W layer, and a 1 μm GaAs upper layer all doped with Si at $5\times10^{16}/cm^3$

concentration. Sample 2 has a 1 μm buffer layer Si-doped at $5\times10^{16}/cm^3$, a nominal 10 nm thick W metal layer, followed by a 10 period superlattice of 5 nm GaAs and 5 nm $Al_{.3}Ga_{.7}As$ and 0.5 μm of GaAs, all doped at $5\times10^{16}/cm^3$ with Si. Sample 3 has the same structure as 1 but with a nominal 8 nm W layer and a doping level of $2\times10^{16}/cm^3$ of Si. After growth the samples were patterned with 100 μm diameter dots of Au/Sn/Au contact metallization and alloyed at 400˚C for 20 sec. Some of the samples were then etched in 4:1:1 H_2SO_4:H_2O_2:H_2O to expose the metal base layers, while others were left unetched.

Electrical measurements on these samples were performed in a home-built probe station capable of making multi-point probe measurements at temperatures from room temperature down to 20K. Current-voltage measurements were made using a Keithley model 230 programmable voltage source and a Keithley 619 electrometer. The current was measured as voltage across a 100 Ω load resistance in series with the diode. Faster though less accurate measurements were made using a ramp source from a Hewlett Packard 8116A signal source and detected on a Tektronix 7854 oscilloscope with a 7A22 vertical amplifier. The digitized data from the oscilloscope and the electrometer were passed to a Digital Equipment MICRO PDP-11 computer via an IEEE-488 bus. Transistor characteristics for those devices with contacted base layers have been reported previously.[4] However, the significant processing problems encountered in exposing the base and maintaining base conductivity led us to do a more extended series of measurements on the diode characteristics of structures with floating metal layers.

The striking characteristic feature of these current-voltage measurements is shown in Figure 1(a,b). At room temperature (290K) the current clearly resembles that of a diode. The asymmetry of the current has been discussed before.[4] It appears to be due to the greater density of defects in the overgrown GaAs material which lead to greater leakage and earlier breakdown of the diode characteristic in that direction. The polarity of these plots always corresponds to positive voltage for the upper contact. As the temperature is lowered, the characteristic changes. The same diode at 22K shows a resistor-like current-voltage relation which appears to saturate and returns to the diode form for higher voltages. Figure 1b shows low-bias I(V) curves in sample 2 for a range of temperatures. The characteristic can be roughly modeled as a diode shunted by a saturable, temperature-dependent resistor. As temperature

drops by a factor of 10, from 290K to 30K, the equivalent resistance, i.e. the inverse of the slope of the I(V) curve at low bias voltage, drops by a factor of nearly 300 in sample 1 and by over 4,000 in sample 2. Typical current ratios of I at 290K and 30K are shown in Figures 2a and 2b. Ratios of this sort are commonly seen only in very pure metals.[5] Further, this resistance roughly follows an exponential law $R \sim R_o\exp(\alpha T^2)$ with $R_o \approx 2{,}900\Omega$ and $\alpha \approx 6.1\times10^{-5}/K^2$ from 290K down to 22K in sample 2. There is a slight difference in R_o on the positive and negative sides of zero bias, amounting to about 1% in both samples 1 and 2. No strong asymmetry associated with the superlattice upper layer of sample 2 has been seen. Sample 3 is a much leakier structure with a very weak diode characteristic at room temperature. It exhibits only about a factor of three drop in resistance at 30K.

The resistance as a function of temperature is remarkable in several ways. Its behavior is opposite to that expected in a junction barrier device and the lack of power law behavior argues strongly against scattering being the cause.[6] In fact it behaves very much like a barrier device with a temperature controlled barrier. This is what we believe to be the case.

The model which provides the best physical explanation of this behavior takes into account the fact that the device is not merely a simple barrier structure but one with internal modulation. The measured current in these devices can pass through the base region by several paths. As shown in Figure 3a, there are four basic conduction mechanisms operating in the barrier region. The dominant emitter-collector current under most circumstances is that labeled (1) in Figure 3a. This is the current through the perforations in the metal layer. Since the barrier in these perforations ϕ_P is less than the Schottky barrier ϕ_{SB} to the metal itself and since the quantum mechanical reflection coefficient[7] is not important to this current path because the electrons remain in GaAs, it dominates over other emitter-collector current paths even when the perforations account for only a small fraction of the area of the base. The current path labeled (2) in Figure 3a represents thermionic emission over the emitter-base Schottky barrier ϕ_{SB}. It tends to add charge to the base. The current paths labeled (3) and (4) tend to remove charge from the base. Path (3) represents thermionic emission over the base-collector Schottky barrier. This current is substantially less than current (2) because the effective barrier height is less for the forward-biased Schottky barrier. Both current paths (2) and (3) are exponentially enhanced by temperature. Current

path (4) represents a base leakage current due defect-related tunneling. We have previously discussed this current as a dominant cause of poor amplification in these structures.[4] This current is relatively temperature independent. When a bias voltage is applied to the emitter and collector the metal of the base is charged by current (2) and discharged by currents (3) and (4). At room temperature current (2) is substantially greater than (3) and (4) and the metal of the base acquires a charge Q. As shown in Figure 3b, this charge raises the potential of the metal base and of the material in the perforations. Current flow by path (1) is blocked as the potential barrier rises. This is the metal gate transistor action first proposed by Lindmayer.[8] With current flow blocked the emitter-collector I(V) characteristic resembles that of a triangular barrier diode.[9,10] At low temperatures the base charging current (2) is reduced while current (4) is essentially unchanged so the base charge is continually reduced as temperature drops. The current saturation observed in Figure 1a occurs at levels of 1-5% of the saturation current for the device area in question. This is consistent with previous transmission electron microscopy studies of the W layers showing approximately that much area to be perforated.[3,4] The improvement of the current ratios in the superlattice sample 2 we attribute to reduced leakage rather than wide-gap emitter effects, since no pronounced asymmetry of the I(V) curves exists when compared with the pure GaAs overlayer sample 1. The peak in the current ratios of Figure 2 is explained by the saturation of current path(1). The absence of a peak in the reverse bias direction is due to the higher leakage in the overgrown material. The current ratio must be unity at zero bias.

The pronounced effect shown in unetched structures is in contrast with the much weaker effect shown in structures in which the base has been exposed and contacted. The act of exposing the W base seems to greatly increase the leakage current (4) and reduce the possibility for base charging. The implication for practical transistor applications of these structures is that processing problems, not inherent structural problems have reduced the available current gain in the previous study.[4] The strength of the anomalous temperature effect shown in the current work suggests that metal gate transistors may have substantially higher gain than previously reported. Similar anomalous temperature dependence of diode characteristics should also be expected in other structures where charge trapping and internal gain occur. Examples are two-terminal measurements of some permeable-base[11] and hot electron

transistors.[12,13]

In conclusion, we have observed a striking anomalous temperature dependence of floating metal base diodes in which the resistance at low bias *falls* exponentially with reduced temperature rather than rises. We ascribe this effect to base charging by thermionic currents coupled with the internal modulation characteristics of the devices. We wish to thank L. Peterson for assistance in growing the samples and M. Gurvitch and F. Capasso for helpful conversations during the course of this work.

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Atts.
References 1-13
Figure Captions
Figures 1- 4

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FIGURE CAPTIONS

Figure 1a. Current-voltage characteristics for sample 1 with GaAs/W/GaAs structure at temperatures of 290K and 22K. The change from diode behavior at high temperatures to resistor-like behavior a low temperatures with saturation of the resistor characteristic is evident.

1b. Low bias current-voltage characteristics for sample 2 with GaAs-AlGaAs Superlattice /W/GaAs structure at five indicated temperatures. The monotonic nature of the resistance-temperature relationship is evident.

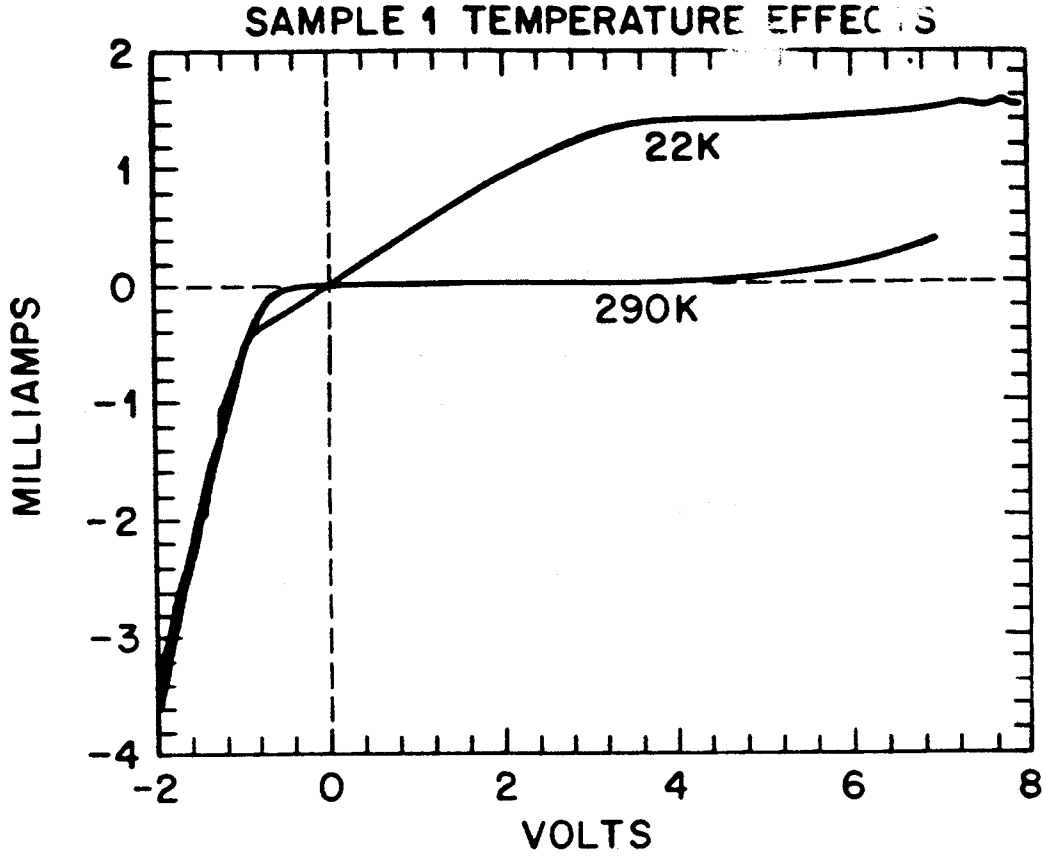
Figure 2a. Ratio of current at 30K to current at 290K as a function of voltage for sample 1.

2b. Ratio of current at 30K to current at 290K as a function of voltage for sample 2.

Figure 3a. Structure of the device with important current paths indicated. The Schottky barrier height to the metal base is indicated by ϕ_{SB}. The barrier height in the perforations is indicated by ϕ_P. The Fermi levels in the emitter and collector are indicated by E_{Fe} and E_{Fc} respectively. The potential barrier to the metal is indicated by a solid line and that to the perforation by a dash. The paths of currents in the device are designated as follows: (1) The thermionic current from emitter to collector through the perforations, (2) the thermionic current from the emitter into the base metal, (3) the thermionic current from the base metal to the collector, (4) the tunneling current, mediated by defects (x), from the base into the collector. The "hot electron" component, important to the usual metal base transistor, is negligible.[13]

3b. Effects of charge-up of the base. The solid and dotted lines indicate the potential barrier to the metal respectively with and without charge. The dashed and dot-dashed lines indicate the potential barrier to the perforations respectively with and without charge.

a)


SAMPLE 1 TEMPERATURE EFFECTS
22K
290K
MILLIAMPS
VOLTS
2
1
0
-1
-2
-3
-4
-2
0
2
4
6
8

b)

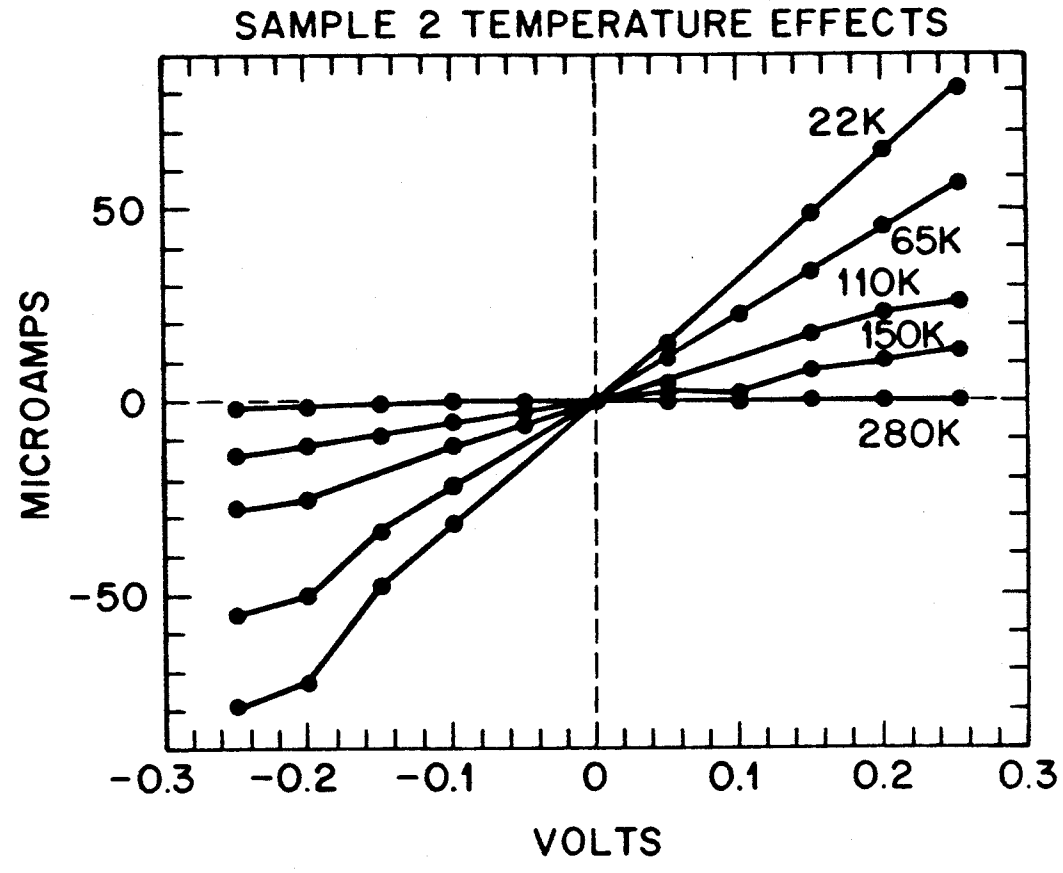
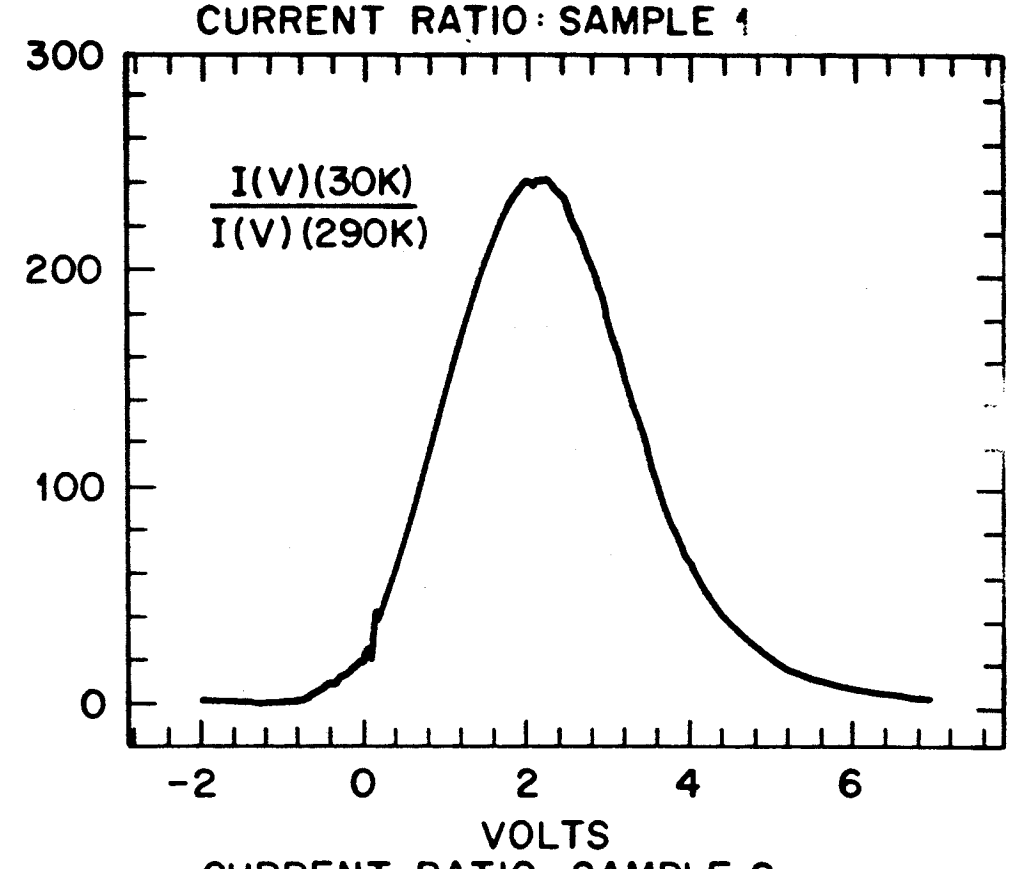

SAMPLE 2 TEMPERATURE EFFECTS
22K
65K
110K
150K
280K
MICROAMPS
VOLTS
50
0
-50
-0.3
-0.2
-0.1
0
0.1
0.2
0.3

Fig. 1

a)


CURRENT RATIO: SAMPLE 1
300
200
100
0
I(V)(30K)
I(V)(290K)
-2
0
2
4
6
VOLTS

b)

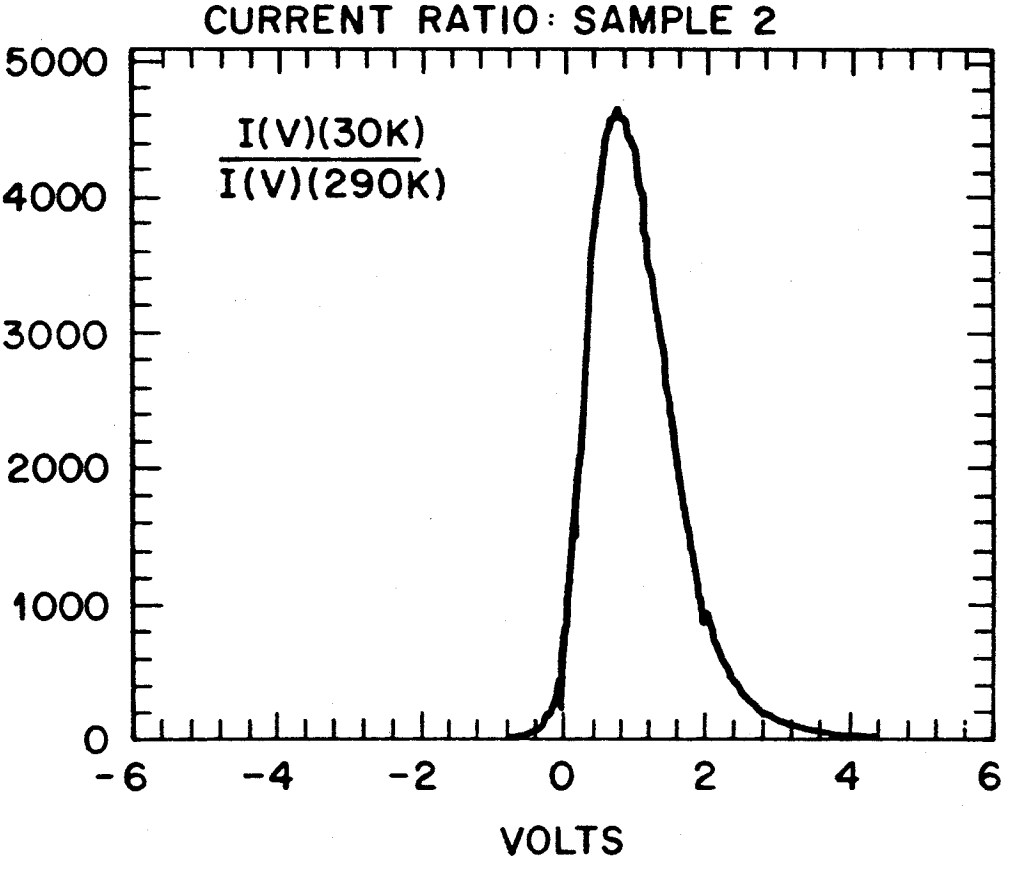

CURRENT RATIO: SAMPLE 2
5000
4000
3000
2000
1000
0
I(V)(30K)
I(V)(290K)
-6
-4
-2
0
2
4
6
VOLTS

Fig. 2

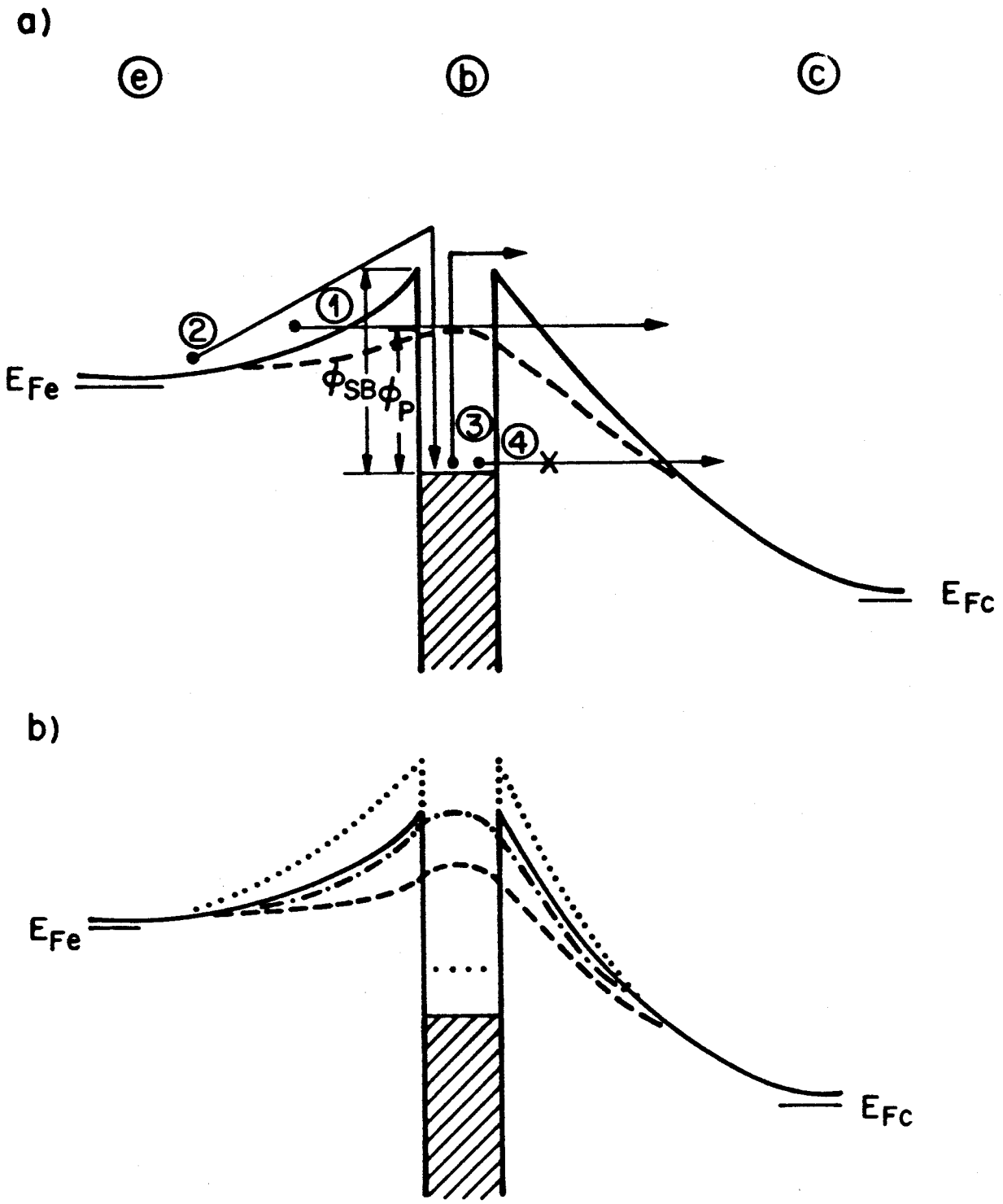


Fig. 3