and planar p-n junctions," *IEEE Trans. Electron Devices*, vol. ED-23, pp. 950-955, 1976.

[8] D. L. Scharfetter and H. K. Gummel, "Large-signal analysis of a silicon Read diode oscillator," *IEEE Trans. Electron Devices*, vol. ED-16, pp. 64-77, 1969.

[9] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1969.

[10] R. Van Overstraeten and H. De Man, "Measurement of the ionization rates in diffused silicon p-n junctions," *Solid-State Electron.*, vol. 13, pp. 583-608, 1970.

[11] V. C. Alwin, "Time-dependent carrier flow in a power transistor structure under nonisothermal conditions," Ph.D. dissertation, University of Massachusetts, Amherst, MA, 1976; also V. C. Alwin, D. H. Navon, and L. J. Turgeon, "Time dependent carrier flow in a transistor structure under nonisothermal conditions," *IEEE Trans. Electron Devices*, vol. ED-24, pp. 1297-1304, 1977.

[12] S. Yasuda and M. Kurata, "Two-dimensional field distribution analysis of reverse biased p-n junction devices," *Solid-State Electron.*, vol. 23, pp. 1077-1084, 1980.

[13] C. A. Lee, R. A. Logan, R. L. Latdorf, J. J. Kleimack, and W. W. Wiegmann, "Ionization rates of holes and electrons in silicon," *Phys. Rev.*, vol. 134A, pp. 761-773, 1964.

[14] V.A.K. Temple and M. S. Adler, "Calculation of the diffusion related avalanche breakdown in high-voltage planar p-n junctions," *IEEE Trans. Electron Devices*, vol. ED-22, pp. 910-916, 1975.

[15] D. R. Decker and C. N. Dunn, "Temperature dependence of carrier ionization rates and saturated velocities in silicon," *J. Electron. Mater.*, vol. 4, pp. 527-547, 1975.

New Infrared Detector on a Silicon Chip

SERGE LURYI, MEMBER, IEEE, ALEXANDER KASTALSKY, AND JOHN C. BEAN, MEMBER, IEEE

***Abstract*—We report a single-crystal Si-Ge structure which works as an efficient photodetector in the wavelength region of up to 1.5 μm. The multilevel structure is grown by molecular-beam epitaxy on an n-type 3-in silicon substrate and consists of the following layers: n^+ silicon (1000 Å), $n^+Ge_xSi_{1-x}$ alloy (1800 Å, graded in ten steps from $x = 0$ to $x = 1$), n^+ germanium (1.25 μm), undoped germanium (2.0 μm), and p^+ germanium (2500 Å). Top three layers form a germanium p-i-n diode, which is removed from the Ge-Si interface by a buffer layer of high conductivity. An advantage of this structure is that its performance is insensitive to material defects in the buffer layers. Moreover, transmission electron microscopy shows that the density of dislocations introduced by lattice mismatch at the Ge-Si interface falls off with the separation from the interface. Our first experimental structures do exhibit the characteristics of a germanium p-i-n diode. The spectral response curves agree with those given in the literature for germanium, both at room and liquid nitrogen temperatures. For the incident light wavelength of 1.45 μm we have measured a quantum efficiency of 41 percent at $T = 300$ K. We believe that our approach opens an attractive possibility of fabricating complete infrared optoelectronic systems on a silicon chip.**

I. INTRODUCTION

AS IS WELL KNOWN, the celebrated silicon technology has not been able to produce an on-chip infrared photodetector for long-wavelength fiber-optics communications. The obvious difficulty lies in the fact that silicon band gap E_G is wider than the photon energy in the range of fiber transparency (1.3-1.5 μm). Attempts have been made to overcome this difficulty by using Schottky-barrier structures with photoexcitation of carriers from metal (or silicide) into silicon [1]. The threshold for such a photoeffect is determined by the Schottky-barrier height and can easily match the required infrared range; however, the quantum efficiency of absorption in such structures is usually low. So far, the only practical way of employing silicon technology for fiber-optics communications has been to combine silicon integrated circuits with germanium or InGaAsP detectors on a separate chip.

In this paper we propose another approach to this problem which employs germanium p-i-n diode grown on conducting silicon substrate by molecular-beam epitaxy (MBE). It is well known that germanium does grow on silicon as a single crystal [2]. However, the large lattice mismatch (4 percent) between the two materials usually results in a high density of dislocations at the interface, which adversely affects the p-n junction properties (causing leakage, carrier trapping, etc.). To minimize the effect of dislocations, we have moved the active detector structure away from the interface by inserting a highly doped germanium buffer layer of the same conductivity type as that in the underlying silicon substrate. In order to avoid possible series resistance and trapping due to heterojunction spikes at the interface, the transition between silicon and germanium is made graded rather than abrupt. The resulting structure can be expected to possess the electrical and optical characteristics of an ordinary germaniun p-i-n diode. In order to satisfy the requirements of both speed and efficiency, we must use direct optical transitions in germanium ($h\nu \gtrsim 0.8$ eV). For these transitions the absorption coefficient is of the order of 10^4 cm^{-1}, which corresponds to an effective absorption length of ≈ 1 μm and an intrinsic delay of about 10 ps.

II. EXPERIMENTAL

The multilayer Ge-Si structure used in our experiments and its band diagram are shown schematically in Fig. 1. We have grown two structures 1) and 2), which were identical in every

Manuscript received September 23, 1983; revised March 16, 1984.
The authors are with AT&T Bell Laboratories, Murray Hill, NJ 07974.

0018-9383/84/0900-1135$01.00

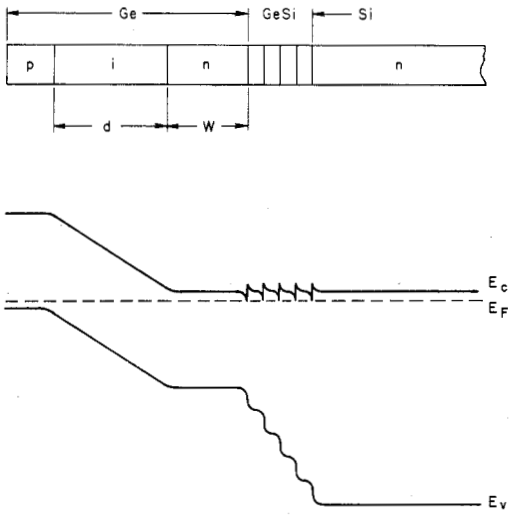


Fig. 1. The multilayer Ge–Si structure and its schematic band diagram.

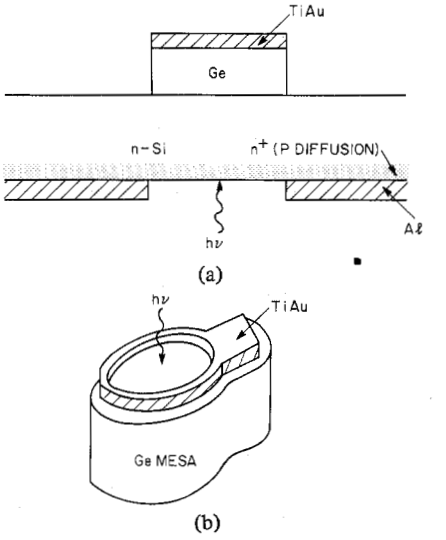


Fig. 2. Detector configurations. (a) Diodes processed for backside illumination. Circular holes in aluminum are aligned with the mesa dots; diameter D = 50, 100, 150, and 200 μm, respectively. (b) Diodes processed for frontside illumination.

respect except for the thickness W of the germanium buffer layer: W_1 = 1.25 μm, and W_2 = 0.3 μm, and a third structure complementary to 2), i.e., germanium n-i-p diode on a p-Si substrate.

The band diagram shown in Fig. 1 was drawn on the assumption of a discontinuity in the valence band of 0.17 eV [3], based on the results of photoemission measurements. This implies a conduction band discontinuity of ≈ 0.023 eV at each step in the Ge_xSi_{1-x} graded layer. On the other hand, if we used the electron affinity data [4] for the heterojunction lineup, the total conduction band discontinuity between Si and Ge would be only 0.05 eV. In either case, for the doping level $N_D \sim 10^{18}$ cm^{-3} we can expect no series resistance associated with spikes in the conduction band. Electron-hole pairs generated by light in the active i-(undoped) layer of germanium, are separated by the built-in electric field so that electrons are collected in silicon. In the structure of complementary polarity, holes were the carriers collected in silicon.

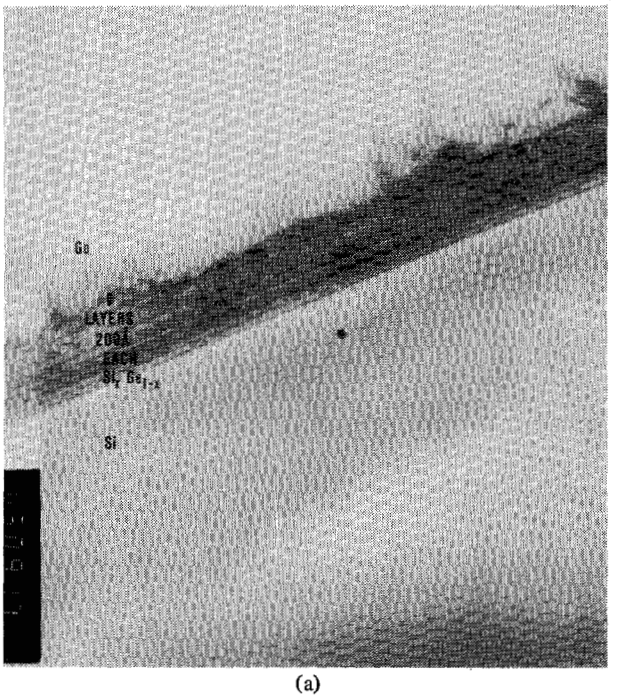
These structures were grown by MBE on Wacker (100) n-type 3-in wafers of 0.5–3.0 Ω · cm resistivity (phosphorus). Prior to MBE processing the wafer front side was protected by a grown oxide, the backside polished and phosphorus diffused. Immediately before MBE growth the oxide was stripped and the wafer chemically cleaned. Details of the MBE apparatus and processing are published elsewhere [2], [5]. Briefly, wafers are cleaned *in situ* by argon ion sputtering followed by an 800°–1000°C anneal. Silicon and germanium are then evaporated from separate e-beam deposition sources onto the wafer at vacuum pressures $\leq 5 \times 10^{-8}$ torr. The e-beam sources were charged with pieces of polycrystalline Wacker silicon and Varian germanium. The Si and Ge poly resistivities were specified as >1000 Ω · cm and >50 Ω · cm, respectively. The initial silicon layer was grown at 750°C and all other layers were grown at 550°C. Heavily doped layers were grown at a rate of 2 Å/s, and the other layers at a rate of 5 Å/s. Dopants were introduced during growth by simultaneous low-energy ion implantation of As_2^+ or BF_2^+. Following MBE growth, wafers were fabricated into diodes by means of conventional UV lithography and wet chemical etching.

The Ge-Si diodes were processed in two ways: a) for back side illumination, and b) for front side illumination. In both cases the backside contact (to silicon) was made by phosphorus diffusion and aluminum metallization. We used silicon wafers polished on both sides. In case a) the optical windows at the back were aligned with metal dots on the top of the mesas (Fig. 2(a)) by using an infrared microscope. In case b) the contact to p-germanium was made in a "pop top" configuration (Fig. 2(b)), which leaves a large area of the diode exposed to illumination.

Transmission electron micrograph (TEM) of the structure[1], shown in Fig. 3(a), clearly resolves the nine 200-Å-thick layers of graded Ge-Si. Dark spots in germanium (above the graded layers) represent the fields of strain and dislocations. Analysis of the TEM data shows that the density of dislocations rapidly decays with separation from the interface. However, as seen from Fig. 3(b), an appreciable number of threading dislocations persist even at distances of order 1 μm into germanium. Alternate Ge–Si grading schemes are being investigated.

Fig. 4 shows the typical diode I–V characteristics, taken at room temperature (Fig. 4(a)) and 77 K (Fig. 4(b)). These characteristics were uniform over the wafer, and scaled with the diode area. Characteristics of diodes processed for backside and frontside illumination were nearly identical. At room temperature, we observe a substantial reverse-bias leakage (Fig. 4(a)) which is linear in voltage. For reverse biases up to several volts, we found a specific resistance $(dV/dI) \times$ area ≈ 5 Ω · cm^2. The fact that the reverse current scales with the area indicates that it is not controlled by a surface leakage. We found no change in the I–V curves for structures 1) and 2) with different thicknesses of the n^+-Ge buffer layer, viz., 0.3 and 1.25 μm. As the temperature is lowered, the reverse leakage drops dramatically, Fig. 4(b). However, even at 77 K, the leakage is substantial at reverse biases above 3 V. When the

[1]The TEM data were taken for us by T. T. Sheng.



(a)

(b)

Fig. 3. Transmission electron micrograph of the structure cross section. (a) Magnification 150 000. (b) Magnification 60 000.

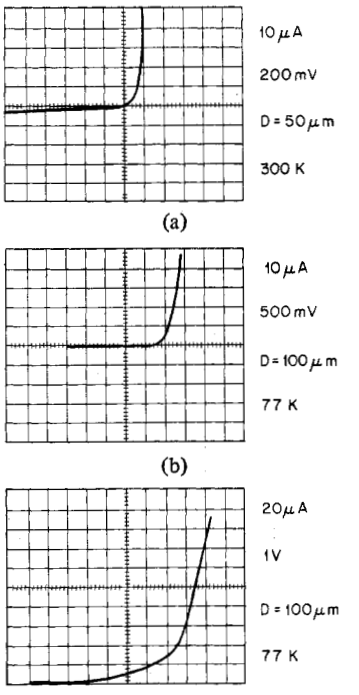


Fig. 4. Current–voltage characteristics. (a) $T = 300$ K. (b) $T = 77$ K. (c) $T = 77$ K, reverse bias only; note that the curve-tracer picture is inverted compared to (b) and the origin shifted by 1 V and 100 μA.

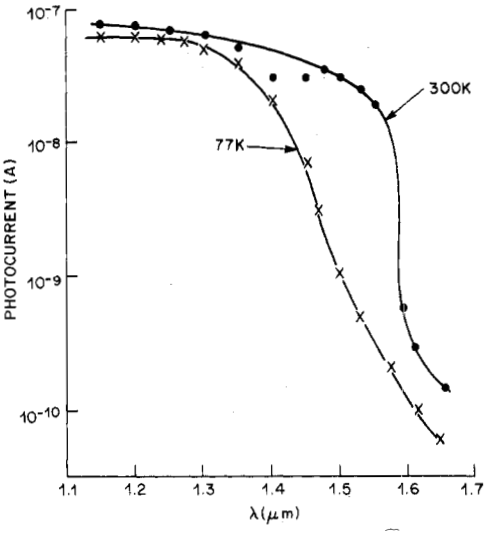


Fig. 5. Photoresponse spectra at 300 and 77 K.

applied voltage exceeds 7 V, the current is controlled by a series resistance due to the silicon substrate, Fig. 4(c). Detailed analysis of the voltage and temperature dependences of the reverse current characteristics, as well as capacitance–voltage characteristics, is presented in Section III.

Optical measurements have demonstrated that photocurrents in our detector result from absorption in germanium p-i-n junction. Fig. 5 shows the photoresponse versus the wavelength λ of incident light, measured at 300 and 77 K, respectively. The photocurrent threshold, as well as its shift with the temperature, agree with the well-known absorption data for germanium (see, for example, [6]). One can see the transition from indirect to direct absorption which occurs with increasing photon energy at $\lambda = 1.45$ μm (77 K) and $\lambda = 1.59$ μm (300 K). The data shown in Fig. 5 were not corrected for the spectral variation of incident optical power (tungsten source). However, we compared the response of our detector with that of a commercially available germanium detector (Judson Infrared Inc., model J-16-8) at $\lambda = 1.3$ μm for $T = 77$ K and $\lambda = 1.45$ μm for $T = 300$ K. The measured quantum efficiency η was found to be approximately 40 percent at both temperatures, which was nearly identical to that of the precalibrated detector (neither detector had an antireflection coating). This high value of η was obtained in the photovoltaic mode, i.e., with no

external bias applied. Similar results were obtained with a complementary structure (n-i-p germanium diode grown on p-type silicon substrate); however, this structure had an order of magnitude higher reverse leakage at room temperature. When we used sample 2 (narrow buffer layer), we obtained very close results with both front and backside illumination. In this sample, using 100-μm dot backside illuminated with incident power of 1.5×10^{-3} W/cm^2 at $\lambda = 1.288$ μm, we measured a photocurrent $I = 5 \times 10^{-8}$ A. On the other hand, when we used sample 1, only front-side illuminated diodes were light-sensitive. In the backside illumination arrangement most of the incident infrared radiation was, evidently, filtered away by the 1.25-μm-thick buffer layer.

III. Electrical Characterization of the Junction

In order to further characterize electric properties of our p-i-n junction and ascertain the orgin of the high observed reverse-bias leakage, we carried out a number of capacitance- and current-voltage measurements at different temperatures. Because of the high leakage at room temperature, C-V characteristics were taken at 77 K only. At zero applied bias, the measured value of the capacitance was $C = 5.8$ pF for a diode of area $A = 3.14 \times 10^{-4}$ cm^2. This corresponds to a depletion layer thickness of about 0.8 μm. Fig. 6 presents a plot of $(A/C)^2$ as function of the applied voltage. The slope of this curve determines fixed charge concentration near the depleted layer boundary. In contrast to the case of a p-n junction uniformly doped on each side, the intercept with the voltage axis does not determine the built-in potential V_{bi}. For an ideal p-i-n diode one has

$$\left(\frac{A}{C}\right)^2 = \frac{2}{qN\epsilon}(V + V_{bi}) + \frac{d^2}{\epsilon^2}$$

where N is the density of fixed charge at one of the boundaries of the depletion layer, d the i-layer thickness, and ϵ the dielectric permittivity. As seen from Fig. 6, the space-charge concentration in the nominally "intrinsic" region of our p-i-n diode is spatially nonuniform and varies from $\sim 4 \times 10^{15}$ cm^{-3} at zero bias to $\sim 9 \times 10^{15}$ cm^{-3} at high reverse biases. If we assume these values for the dopant concentration and calculate the depleted layer thickness and the junction capacitance at zero bias, we find values close to the above quoted measured results. The extent of the active region in our diode is thus determined not by the thickness of the undoped "i" layer (≈ 2 μm), but rather by the depletion length corresponding to the impurity concentration in that layer. The type (p or n) of this unintentional dopant is uncertain.

Fig. 7 shows the reverse-bias characteristics at 77 K. It exhibits a strong (nearly exponential) voltage dependence. This is in contrast to the room temperature leakage (Fig. 4(a)) which has ohmic behavior in a wide range of applied reverse voltage. If we plot $\log I$ versus $(V + V_{bi})^{1/4}$, where V_{bi} is taken equal 0.73 V, which is the bandgap of Ge at 77 K, we obtain a straight line over four orders of magnitude, c.f., Fig. 7. Such a dependence suggests that we are dealing with hopping conduction over deep-level traps in the p-n junction region of Ge, activated by the electric field E. This mechanism of conduction, known as Poole-Frenkel effect, gives [7] $\log I \propto E^{1/2}$. It can explain the curve in Fig. 7(b), since in a p-n junction one has $E \propto (V + V_{bi})^{1/2}$.

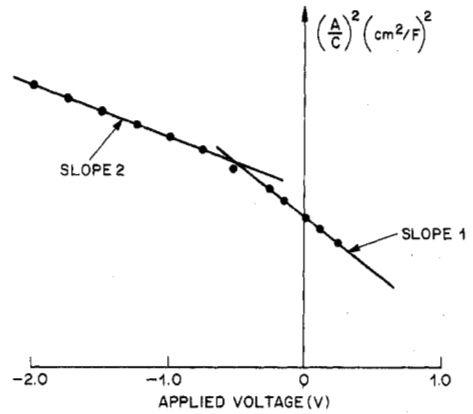


Fig. 6. Capacitance-voltage characteristics at 77 K. Device area $A = 3.14 \times 10^{-4}$ cm^2. We plot $(A/C)^2$ versus V. Slope 1 corresponds to $N = 4.2 \times 10^{15}$ cm^{-3}; Slope 2 gives $N = 9.3 \times 10^{15}$ cm^{-3}. At zero bias $C/A = 1.8 \times 10^4$ pF/cm^2.

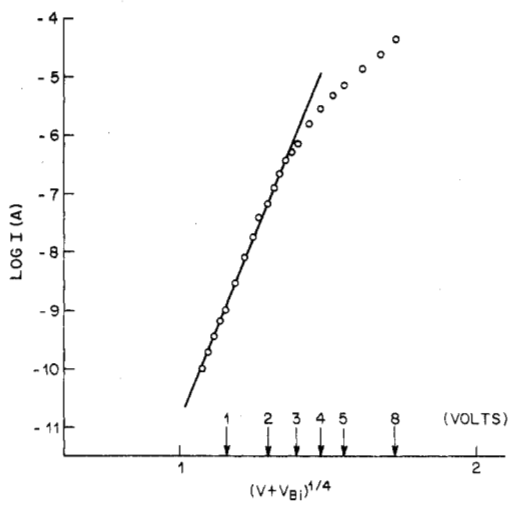


Fig. 7. Reverse-bias characteristics at 77 K. Device area $A = 7.85 \times 10^{-5}$ cm^2. We plot $\log I$ versus $(V + V_{bi})^{1/4}$ with eV_{bi} taken equal 0.73 eV (Ge bandgap at 77 K).

Temperature variation of the reverse current (Fig. 8) has a strong dependence on the applied bias V. for $V \lesssim 0.1$ V the $\log I$ versus $1/kT$ curves show one activation energy, 0.31 eV. On the other hand, curves corresponding to higher V seem to possess two different slopes: one equal 0.31 eV at high temperatures and another, voltage-dependent slope at $T \lesssim 200$ K. This suggests the existence of two distinct mechanisms of conduction. In our view, the mechanism operating at low temperatures is the above mentioned Poole-Frenkel process. In this case the measured slope corresponds to the trap ionization energy lowered by the electric field. The high-temperature behavior may be also explained by hopping conduction over traps in the field region; in this case the 0.31-eV slope would correspond to the energy necessary for carrier activation into traps at one of the boundaries of the field region. Another possible explanation involves threading dislocations, which at high temperatures provide carriers for band conduction with the activation energy of ≈ 0.3 eV [8]. We are unable to dis-

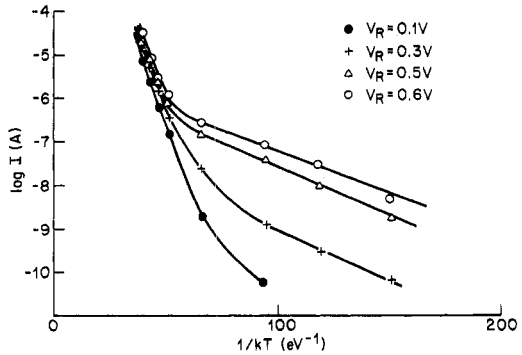


Fig. 8. Temperature dependence of the reverse current at different applied voltages.

tinguish between these two mechanisms, nor suggest any other explanation compatible with the ohmic behavior of the reverse leakage observed at room temperature.

IV. Conclusion

We have demonstrated the feasibility of fabricating infrared photodetectors for long-wavelength fiber-optics communications on a silicon chip. Our approach, based on growing single-crystal germanium p-i-n junction on silicon substrate, is entirely compatible with the silicon integrated-circuit technology. We have fabricated diodes with a quantum efficiency $\eta \approx 40$ percent, measured in a short-circuit configuration. Further improvement can be expected in reducing the reverse-bias leakage, which in our samples appears to be related to the quality of germanium.

Note Added in Proof: Two-hour, 650°-700°C annealing of the present structure has reduced parasitic leakage currents by about a factor of 4. Recent experiments employing alternate grading schemes produced a further improvement, bringing leakage down to ~ 1/20 of the levels reported in this paper. These results will be reported in full in a subsequent publication.

Acknowledgment

The authors are grateful to D. Kahng, R. F. Kazarinov, and S. M. Sze for fruitful discussions, to A. R. Tretola for device processing, to R. T. Lynch and T. T. Sheng for help in the experiments, and to M. P. Lepselter for encouragement and support of this work.

References

[1] T. R. Harrison, A. M. Johnson, P. K. Tien, and A. H. Dayem, "$NiSi_2$-Si infrared Schottky photodetectors grown by molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 41, pp. 734–736, 1982.
[2] J. C. Bean, T. T. Sheng, L. C. Feldman, A. T. Fiory, and R. T. Lynch, "Pseudomorphic growth of Ge_xSi_{1-x} alloys on silicon by molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 44, pp. 102–104, 1984.
[3] G. Margaritondo, "Microscopic investigations of semiconductor interfaces," *Solid-State Electron.*, vol. 26, pp. 499–513, 1983.
[4] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981, p. 850.
[5] J. C. Bean and E. A. Sadowski, "Silicon MBE apparatus for uniform high-rate deposition on standard format wafers," *J. Vac. Sci. Technol.*, vol. 20, no. 2, pp. 137–142, 1982.
[6] K. Seeger, *Semiconductor Physics*. Berlin: Springer, 1973, p. 336.
[7] N. F. Mott and E. A. Davis, *Electronic Processes in Non-Crystalline Materials*, 2nd ed. Oxford, England: Clarendon Press, 1979.
[8] W. Barth and G. Langohr, "Spectral dependence of the stationary photoconductivity and the relaxation process in plastically deformed germanium," *Phys. Status Solid. (a)*, vol. 3, pp. K289–292, 1970.

Design of GaAs 1k Bit Static RAM

MASAYUKI INO, MINORU TOGASHI, MASAHIRO HIRAYAMA, KATSUHIKO KURUMADA, MEMBER, IEEE, AND MASAMICHI OHMORI, MEMBER, IEEE

Abstract—**A 1k bit GaAs static RAM with E/D DCFL was designed and successfully fabricated by SAINT. A bit line pull-up was introduced to the design to make higher operation speed by 25 percent and reduce cell array power consumption by 50 percent. The RAM circuit was optimized in the points of a speed, a power, and an operating margin. A minimum address access time of 1.5 ns was measured for a total power dissipation of 369 mW. This performance is the best achieved so far, for practical application in cache or buffer memories.**

Manuscript received October 19, 1983; revised February 10, 1984.
The authors are with Atsugi Electrical Communication Laboratory, Nippon Telegraph and Telephone Public Corporation, Kanagawa, 243-01, Japan.

I. Introduction

FOR A LONG TIME high-speed and low power IC memories have been expected to be applied for cache or buffer memories in high-speed computers and high bit rate digital communication systems. The GaAs direct-coupled FET logic (DCFL) has the essential requirements of low power consumption, high-speed, and high packing density, for LSI's. The first GaAs 16-bit RAM adopting an E/D DCFL has already been reported [1]. Another approach using LPFL has resulted in a high-speed 8-bit RAM which, however, has quite high power

0018-9383/84/0900-1139$01.00