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# Microwave Generation in NERFET

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*Abstract*—**Microwave generation in a NEgative Resistance Field-Effect Transistor (NERFET) is reported for the first time. This device is based on a GaAs/AlGaAs heterostructure which exhibits negative differential resistance due to a transfer of hot-electrons out of a source-drain channel and into a conducting substrate. In an untuned microwave circuit at 77 K, the NERFET was found to generate wide-band noise at frequencies up to 2.3 GHz. In a tunable resonant circuit, stable microwave oscillations were observed at frequencies as high as 1.45 GHz. While further experiments are needed to determine the performance limits of the NERFET, the preliminary results presented here demonstrate the potential of this new device as a high-frequency element.**

THE FIELD-EFFECT TRANSISTOR with a negative differential resistance (NDR) in its drain circuit (NERFET) was first proposed in [1]. The NDR effect arises owing to hot-electron charge transfer from the FET channel into a subsidiary conducting layer (substrate) over a built-in potential barrier. The NERFET structure was experimentally realized [2] using an MBE grown GaAs/AlGaAs heterostructure shown in Fig. 1. This structure and processing are described in detail in [2] and [3], where it is demonstrated that the structure exhibits NDR in accordance with the hot-electron transfer proposed in [1]. Estimates show [3] that the fundamental limit on the generation frequency in the NERFET lies in the range of 100 GHz and higher.

Static characteristics of the NERFET obtained in [2] showed a pronounced NDR effect strongly influenced by the gate $V_G$ and substrate $V_B$ voltages. This effect has been observed both at $T = 77$ K and $T = 300$ K. A typical I-V characteristic in the drain circuit ($I_D$ versus $V_{SD}$) is presented in Fig. 2 for a device 250 $\mu$m in width. The curve corresponds to the biased-substrate device configuration [2]. As can be seen there is a well pronounced drop in drain current at $V_D = 1.0$ V, indicating the onset NDR. The NDR branch of curve-tracer characteristics appears to be the result of averaging over oscillations.

In this letter we present experimental results which demonstrate microwave power generation in the NERFET. The microwave circuitry for these experiments is shown in Fig. 3.

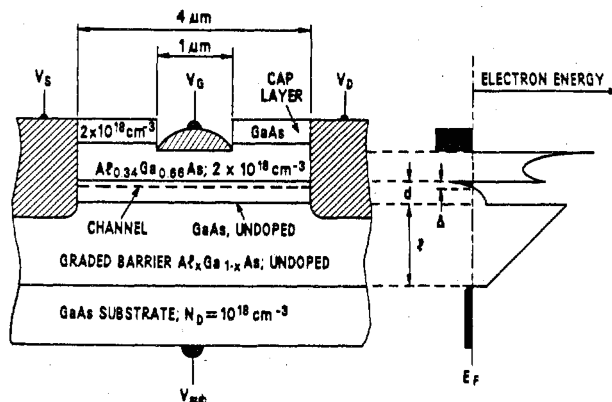


Fig. 1. GaAs/AlGaAs NERFET structure.

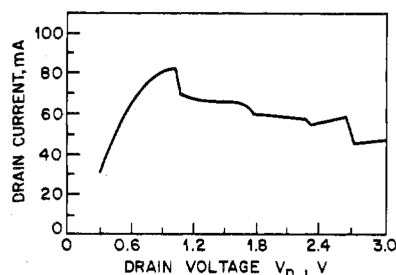


Fig. 2. Drain current $I_D$ versus source-drain voltage $V_D$ at 77 K for $V_G = 0$ and $V_B = 4.0$ V.

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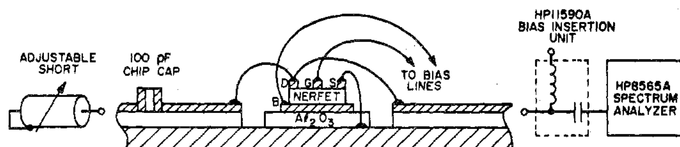


Fig. 3. Diagram of NERFET and microstrip circuit.

The NERFET die was soldered to an alumina standoff insulator which was mounted on the ground plane of a 50-Ω microstrip circuit. The standoff permitted electrical contact to be made to the NERFET substrate $B$ while isolating this contact from the microwave ground. The source contact $S$ was bonded to the ground plane of the circuit while the drain contact $D$ was bonded to two 50-Ω microstrip lines. One of these lines was capacitively coupled to a coaxial adjustable short to provide a resonator in the source–drain circuit which could be turned over the half-wave frequency range of 0.7–3.5 GHz. The other 50-Ω line supplied dc bias to the drain and was used as the output port of the circuit. Bias to the substrate $B$ and gate $G$ was made with separate microstrip lines. In the following, dc bias voltages are referenced to the source. The microwave output was monitored on an HP8565 spectrum analyzer.

The room temperature dc characteristics of the NERFET were considerably degraded with respect to NDR peak-to-valley ratio in this circuit due to heating arising from the poor thermal contact achieved in the present mounting scheme. Thus microwave measurements were only carried out at 77 K. Cooling was obtained by immersion of the circuit in a liquid nitrogen bath.

Before investigating the NERFET's behavior in a resonant circuit, the general microwave activity of the device was examined by monitoring the microwave spectrum with the coaxial resonator removed. As the drain bias voltage $V_D$ was increased, with other bias voltages fixed, broad-band noise was observed beginning at the point of the first drain-current drop seen in Fig. 1, approximately 1.0 V. The noise level as well as the cutoff frequency (highest frequency of the generated noise that could be measured in our system) were dependent on drain and substrate bias, and to a lesser extent on the gate bias. The maximum noise cutoff frequency observed was 2.3 GHz and occurred for $V_D = 1.5$ V, $V_B = 3.7$ V, and $V_G = 0$, where $D$, $B$, and $G$ refer to the drain, substrate, and gate, respectively. At this bias, $I_D$ and $I_B$ were 35 A and 100 mA, respectively.

When the resonator was added to the circuit, the microwave noise disappeared and instead a clean stable microwave output was seen (Fig. 4) at a single frequency $f$ (plus harmonics) which could be tuned by varying the short position. The highest frequency achieved was 1.45 GHz and occurred for $V_D = 2.7$, $V_B = 4.0$, and $V_G = 0$ with $I_D = 55$ mA and $I_B = 90$ mA. The generation efficiency $\eta$ is defined as the ratio of the mw output power to the supplied dc power (which is our case dissipates both in the drain and the substrate circuits). The substrate current is partly due to a parasitic source leakage [3]. In the present experiments, because of device overheating, this parasitic component was dominant. In some measurements, however, we were able to reduce it significantly, thus enhancing $\eta$. The highest efficiency so achieved was $\eta \approx 5$ percent at 0.8 GHz with the microwave power being 2 mW.

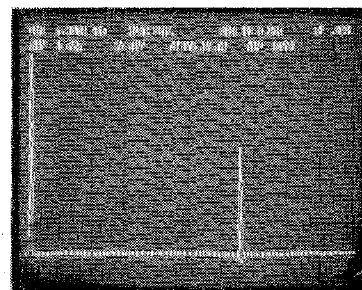

Fig. 4. Typical single frequency output ($f$ = 1.18 GHz) on spectrum analyzer; $T$ = 77 K.

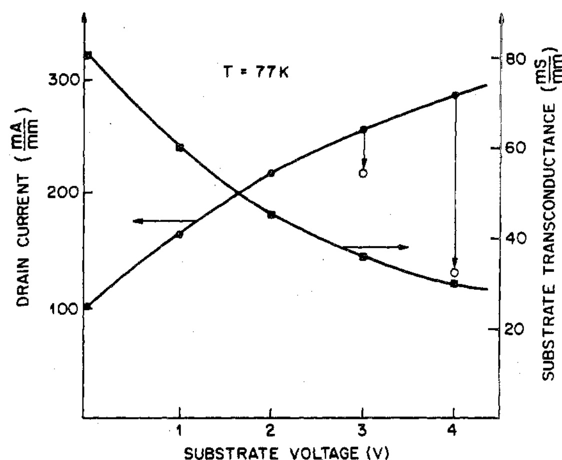


Fig. 5. Drain current and substrate transconductance versus substrate voltage $V_B$ for a typical NERFET at $V_D = 0.95$ V. The circles indicate the current drop seen at $V_D = 1.0$ V. Values per millimeter of gate width are shown.

As previously described, the drain current in the NERFET is controlled by the gate action of both the metallic gate and the substrate. Thus microwave oscillation can occur in this structure not only due to the negative resistance of the drain current, but also by conventional transistor action involving feedback from the drain circuit to either the gate or substrate circuits. The possibility that the observed oscillations were due to a transistor action involving the gate is eliminated by the fact that similar oscillations were also observed for a modified NERFET having a gate notch, but no gate metallization. Furthermore, the fact that the current instability occurs for a range of substrate bias where the substrate transconductance is relatively low, as seen in Fig. 5, supports the argument that the oscillations do not originate from a transistor action involving the substrate. Thus we believe the microwave oscillations originate from the NDR mechanism described in [1] and [2]. At this stage it is very encouraging that the device appears to be free of the parasitic electron trapping and reemission processes, which at 77 K would have limited its speed well below the observed gigahertz frequencies.

We believe that the frequency cutoff in these experiments is due to the limitations of our high-frequency setup rather than to the intrinsic device limit. For the present geometry the device frequency limit was estimated [3] to be about 30 GHz—resulting mainly from the capacitance between the drain pad and the substrate. The ultimate frequency limit of NERFET is of the order of 100 GHz [3], which should lead to performance exceeding that of Gunn diodes. In addition, the higher peak-to-valley ratio in the NERFET should result in higher generation efficiency. Finally, the presence of a third electrode in NERFET allows for the unique possibility of direct modulation of the oscillation amplitude.

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# Suppressing Latchup in Insulated Gate Transistors

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*Abstract*—**Two-dimensional computer modeling of insulated gate transistor (IGT) structures has been used to demonstrate the suppression of latchup in the parasitic thyristor by increasing the p-base conductivity using a deep $p^+$ diffusion in the device cells. Experimental verification of these modeling results has been performed with thyristor latching current density of over 1000 A per $cm^2$ achieved in 600-V devices at room temperature.**

## I. INTRODUCTION

THE INSULATED GATE TRANSISTOR (IGT) is a new device concept in which MOS and bipolar technologies have been integrated to obtain superior device characteristics [1], [2]. These devices have the advantages of operating at much higher current densities than power MOSFET's and bipolar transistors and having a high input impedance MOS gate which minimizes gate drive requirements. An additional feature of these devices is their reverse blocking capability. However, the device contains a parasitic p-n-p-n thyristor structure whose latchup can cause loss of gate control. Thus to operate these devices at high current densities with gate turn-off capability it is essential to suppress the latchup of the parasitic thyristor in the IGT. The structure reported in the earlier paper [1] was found to latch up at current densities above 100 A per $cm^2$. In this letter, the development of an improved structure is described by the use of both theoretical and experimental studies which have resulted in increasing the latching current density to above 1000 A per $cm^2$ at room temperature.

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## II. DEVICE MODELING

The basic IGT cell structure is shown in cross section in the inset of Fig. 1. The cell dimensions and the doping levels used in the modeling are indicated in the figure. It was found that when the collector voltage was increased in steps of 0.25 V with a gate bias of +14 V to turn-on the channel, the device operated in the gate controlled mode up to a forward voltage drop of 1.25 V. The collector current density at this point was 71 A per $cm^2$. However, on increasing the collector voltage to 1.5 V, the parasitic thyristor was found to latch on. This is indicated by the electron carrier distribution in Fig. 1. It can be seen here that the electron concentration is high in the p-base region under the emitter indicating that current flow is occurring in the p-n-p-n thyristor section instead of being confined to the inversion channel. The highest gate-controlled collector current density was, therefore, limited to less than 100 A per $cm^2$. The $n^+$ region under the gate between the cells was included to improve the spreading resistance during forward conduction. It had no effect upon the latching current.

In order to suppress latchup of the parasitic thyristor, it is necessary to increase the conductivity of the p-base under the $n^+$ emitter. This allows higher lateral current flow in the p-base before the emitter–base junction is forward biased in excess of the 0.7 Volts required to obtain electron injection from the emitter which causes the regenerative latchup. The best method to achieve this is by the introduction of a highly doped deep $P^+$ diffusion in the cells, as illustrated in the inset of Fig. 2. This method allows control of device threshold voltage with the shallow p-diffusion to form the DMOS

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