Double Gate Coupling and Quantum Tunneling in Ultrathin SOI MOSFETs

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1. Introduction

Silicon-on-insulator (SOI) transistors built in thin fully-depleted Si channels on top of an insulating buried oxide are predicted by the various technology roadmaps[1] to take over from bulk Si complementary metal–oxide–semiconductor (CMOS) devices over the next few years. Fully-depleted SOI MOSFETs with moderately thick bodies have been around for a long time and reliable models are available.[2] Film thinning improves the electrostatic control but also causes interesting coupling effects. The validity of the existing physical models for channels thinner than 10 nm is uncertain, as the film capacitance becomes very large, the coupling between the two interfaces is inhibited, and quantum confinement occurs.

At the same time, the ongoing miniaturization of SOI devices, with available Si channel and gate insulator thicknesses dropping to the nanoscale, is opening the door to quantum effect devices based on tunneling and/or charge quantization fabricated in and integrable with mainstream CMOS. This is significant because it appears unlikely that any incompatible quantum effect architecture will make inroads against CMOS.[3]

As CMOS transistors are downscaled, there is an ongoing debate about the most favorable SOI transistor geometry,[4] hinging on the advantage of double-gate (DG) over single-gate (SG) MOSFETs.[5,6,7] Numerical simulations demonstrate the perfect electrostatic control in DG MOSFETs and their superior scalability, with excellent overall agreement essentially because the same simulators are used everywhere. On the experimental side, however, there are still unanswered questions and inconsistent results. Despite impressive efforts to devise a pragmatic DG process flow, the comparison of DG *vs*. SG is not easy. For

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example, fin-FETs or gate-all-around DG-MOSFETs cannot be operated in SG mode at all.[6,8,9,10,11] In other DG layouts, where a comparison is possible, the usual procedure is to operate the same transistor either in SG mode (with the backgate grounded) or in DG mode. Virtual DG operation is achieved by adjusting the front- and backgate biases to account for existing asymmetries in the gate work functions and/or different thickness of gate and buried oxides.[7,12,13] Such measurements have produced useful insight but also astonishing results: *e.g.* reported subthreshold slope S below 60 mV/decade and giant gains in DG transconductance.[12] Here we study the gate biasing equations, revisit the correct values of the gate voltages which are different for weak and strong inversion, and discuss the proper conditions for measuring S in ultrathin DG MOSFETs that dispel any ambiguity.

Aside from achieving improved electrostatic control by film thinning, our research also focuses on quantum effect possibilities introduced by further downsizing the devices. To date, most of the work in CMOS-compatible tunneling transistors has focused on quantum dots replacing the usual channel,[14,15] wherein tunneling into discrete energy levels combined with Coulomb charging can produce sharp nonlinear features in $I_D(V_G)$. Recently, room-temperature single-electron transistors with an ultrasmall silicon quantum dot in a lateral point-contact channel MOSFET architecture have been reported[16] – albeit with relatively small current drive and difficult device integration. Generally, much research has focused on vertical resonant tunneling (RT) structures, where strongly nonlinear current–voltage $I(V)$ characteristics and negative differential resistance (NDR) arise due to carrier tunneling into a reduced dimensionality density of states – a quantum well (QW), wire or dot confined by epitaxial tunneling barriers.[17,18] The difficulty with Si-based RT structures has been the absence of sufficiently high barriers. Technologically compatible strained Si/SiGe pseudomorphic RT structures[19] operate with tunneling barriers in the 0.2–0.3 eV range, leading to low-temperature operation and much less pronounced NDR, suitable for spectroscopy of confined states in SiGe QWs and dots,[20,21] but problematic for devices. Other Si-based resonant tunneling structures involve exotic materials, such as CaF_2, that are difficult to integrate with silicon technology.[22]

Our ultrathin SOI transistors, produced by conventional technological process, vary from 5 nm to 50 nm in channel thickness t_{Si} and from 1 to 4.5 nm in gate oxide thickness t_{OX}. Below we discuss gate coupling effects and examine the proper biasing for a reliable comparison of SG and DG modes in our SOI MOSFETs. Then discuss a backgate voltage-controlled vertical tunneling transistor[23] based on the same ultrathin SOI structure, that operates in the quantum capacitance mode[24] at low temperature.

2. Device fabrication

Fully-depleted *n*-MOSFETs were fabricated on an 8" silicon line at LETI-CEA on standard UNIBOND SOI substrates (with the buried oxide thickness t_{BOX} = 400

nm) using an existing CMOS mask set. The active region Si was initially thinned to 50 nm using repeated sacrificial oxidation and removal. The transistor body was left undoped (initial wafer doping was $N_A = 5x10^{14}cm^{-3}$). For the devices with thinner body, the channel was locally thinned to t_{Si} ~ 5–10 nm. In some of the wafers with a thin channel, the thermal gate oxide was kept as thin as possible by densifying the native oxide, resulting in a ~1 nm SiO_2 gate oxide used for vertical tunneling transistors (VTTs).[23] Other ultrathin MOSFETs had 4.5 nm gate oxide. After *in-situ* doped poly-Si gate deposition (P-doped to ~10^{19} cm^{-3} range), the devices followed standard transistor processing with low-energy 3 keV As source/drain implants.

In the next Sections 3 and 4, we compare our ultrathin transistors with t_{Si} ~ 9 nm, t_{OX} = 4.5 nm, L_G = 50–150 nm channel lengths and W_G = 10 μm channel width to previously fabricated devices with t_{Si} = 47 nm, t_{OX} = 4.5 nm, and $5x10^{17}$ cm^{-3} channel doping in the context of DG operation. Section 5 presents our study of the VTTs with t_{Si} ~ 5 nm and t_{OX} ~1 nm. The fabrication sequence of the ultrathin devices was simulated on Silvaco software, using the actual implantation and activation anneal parameters. The resulting cross-sectional view of our ultrathin SOI MOSFETs (L_G = 0.1 μm, W_G = 10 μm, t_{OX} = 1 nm) is illustrated in Fig. 1.

3. Coupling effects in ultrathin SOI MOSFETs

The scaling rules for bulk Si MOSFETs converge on reduced junction thickness and increased channel doping, which adversely affect the junction capacitances, carrier mobility, and circuit speed. As compared to bulk MOSFETs, the scaling rules and design windows are different for fully-depleted SOI transistors, where the thinning of the silicon film is the winning strategy. In this section, we focus on the gate coupling effects that are enhanced in ultrathin film MOSFETs.

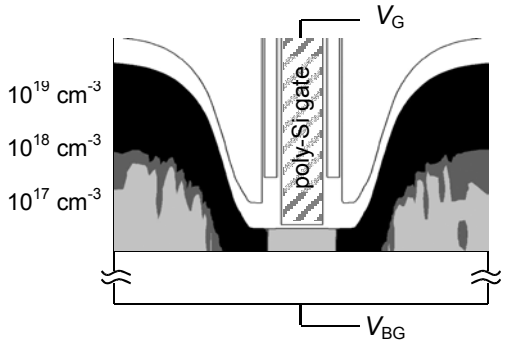

Figure 1. Cross-sectional view of the device: Si channel under the gate is ~5–10 nm thick, the front gate oxide is as thin as ~1 nm. Grayscale contours show the 10^{19}, 10^{18}, and 10^{17} cm^{-3} doping regions in the source and drain extensions, the channel under the gate is essentially undoped.

Figure 2 highlights the influence of the backgate bias V_{BG} on the front-channel characteristics $I_D(V_G)$ of a typical ultrathin SOI MOSFET. The curves shift laterally due to the so-called "interface coupling". The threshold voltage V_{T1} of the top channel decreases with increasing V_{BG}. This variation can be modeled by the classical coupling relation formulated by Lim and Fossum:[25]

$$V_{T1} = V_{T1}^{acc} - \frac{C_1 C_2}{C_{OX}(C_{BOX} + C_{Si})} (V_{BG} - V_{BG}^{acc}) \quad (1)$$

where V_{T1}^{acc} is the frontgate threshold voltage for back channel accumulation and V_{BG}^{acc} is the corresponding back gate bias, $C_{Si} = \varepsilon_{Si}/t_{Si}$ is the depleted Si film capacitance, C_{OX} and C_{BOX} are frontgate and backgate oxide capacitances, and we ignore the interface traps. In general, for our devices C_{Si} and $C_{OX} >> C_{BOX}$.

Reciprocal back-channel characteristics $I_D(V_{BG})$ provide the variation of the corresponding threshold voltage with the front-gate bias V_G. The variations of the front and back threshold voltages with opposite gate bias, $V_{T1}(V_{BG})$ and $V_{T2}(V_G)$ respectively, are superimposed in Fig. 3. In relatively thick devices, the two curves have a clear intersection, as illustrated in Fig. 3(a). The difference in the two slopes rises with the film thickness. For the front channel we have:

$$\Delta V_{T1} \cong -(t_{OX}/t_{BOX})\Delta V_{BG}\,, \quad (2)$$

whereas the back channel is dictated by:

$$\Delta V_{T2} \cong -[(t_{BOX}/t_{OX})\ \frac{C_{Si}}{C_{OX} + C_{Si}}\ ]\ \Delta V_G\,. \quad (3)$$

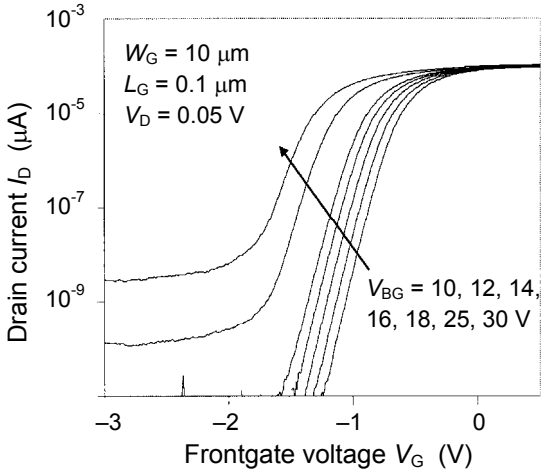

Figure 2. Drain current characteristics as a function of backgate voltage in t_{Si} = 9 nm SOI MOSFETs (V_D = 50 mV, L_G = 0.1 μm, W_G = 10 μm).

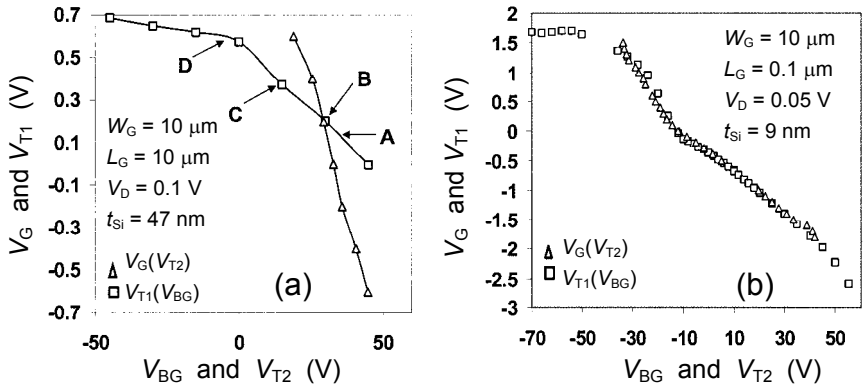

Figure 3. Front channel threshold voltage *vs.* backgate bias $V_{T1}(V_{BG})$ and influence of frontgate bias on back channel threshold $V_G(V_{T2})$ for SOI MOSFETs with (a) t_{Si} = 47 nm thick (L_G = 10 μm, W_G = 10 μm); (b) t_{Si} = 9 nm (L_G = 75 nm, W_G = 10 μm).

On the other hand, our ultrathin transistors behave differently and the two curves tend to coincide, as shown in Fig. 3(b). The slopes of in Eqs. (2) and (3) become identical slopes as soon as the film capacitance C_{Si} exceeds the gate oxide capacitance C_{OX}, which happens for small t_{Si} as long as t_{OX} is not too thin. It is worth noting that in such ultrathin films, the classical distinction between front and back channels is exaggerated because the minority carriers tend to spread over the whole film thickness, an effect often termed volume inversion. The result is that when one interface is driven into inversion, the potential at the opposite interface is also dragged from depletion to weak and even strong inversion. This effect can be understood by considering the body as a narrow, rectangular well with a rather flat potential. Super-coupling arises: raising the potential on one side, raises the potential of the entire Si channel. Accordingly, concurrent inversion of one interface and accumulation of the other may not be possible in extremely thin films. This feature has been verified by a transient experiment. The front gate was biased in inversion and the backgate was switched from zero to –30 V. In a thick film, such a negative switch drives the back interface into accumulation. Since the necessary majority carriers are slowly supplied by electron-hole generation process, a long I_D undershoot is normally observed.[2,26] In the 9 nm thick MOSFET, there is no transient at all, simply because the accumulation region could not be formed.

As a relevant application of the super-coupling effects described above, the next section will discuss virtual DG operation in ultrathin SOI MOSFETs, a rigorous comparison of DG and SG modes in the same transistor, and the trans-conductance advantage of the DG mode.

4. Virtual double gate operation: weak and strong inversion

Double-gate (DG) MOSFETs exhibit nearly perfect potential control and excellent performance. This is why DG MOSFETs are considered as unchallenged devices for ultimate integration.

The comparison of SG and DG modes of operation in asymmetric SOI structures with different t_{OX} and t_{BOX} often relies on the following simple recipe:

$$V_{BG} - V_{T2} = (t_{BOX}/t_{OX})(V_G - V_{T1}) \, . \tag{4}$$

Equation (4) accounts for the difference in oxide thickness and is valid in strong inversion. It guarantees the same amount of inversion charge at the front and back channels. Yet we will show that using Eq. (4) outside the strong inversion regime requires extreme caution.

- *Weak inversion*

An instructive exercise is illustrated in Fig. 4(a) showing the simulated subthreshold characteristics of a virtual DG transistor biased according to Eq. (4) for several ratios of S_2/S_1 ($S_{1,2}$ are the subthreshold slopes simulated independently for the front- and back channels, respectively) at a fixed oxide thickness ratio t_{BOX}/t_{OX} = 10. One of the curves (S_2/S_1 = 1) shows a subthreshold swing of 7 mV/decade, nearly an order of magnitude smaller than the idea 60 mV/decade value and hence obviously unphysical. Evidently, Eq. (4) is just not valid in weak inversion, where the current increases exponentially with gate bias. For ideal DG operation, we need same charge in the two channels, which yields the correct biasing condition in weak inversion:

$$V_{BG} - V_{T2} = (S_2/S_1)(V_G - V_{T1}) \, . \tag{5}$$

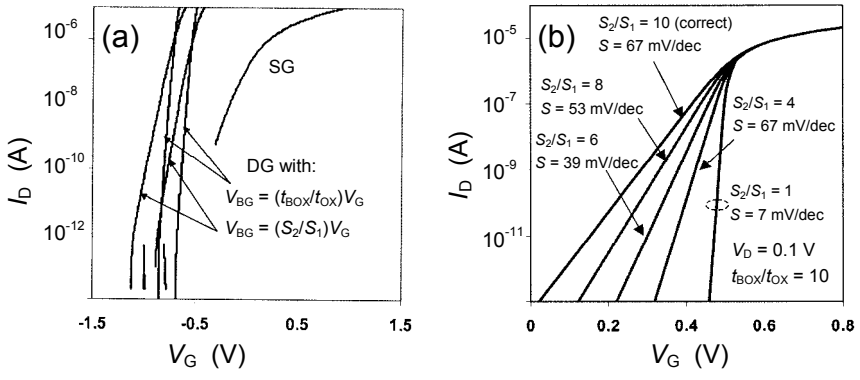

Figure 4. (a) Simulated DG subthreshold characteristics of an ultrathin (t_{Si} = 9 nm) SOI MOSFET comparing Eqs. (5) and (6); (b) virtual double-gate $I_D(V_G)$ characteristics simulated with Eq. (5) for several S_2/S_1 ratios and t_{BOX}/t_{OX} = 10.

A clarifying example is given in Fig. 4(b), where simulated DG curves are shown for a fixed ratio t_{BOX}/t_{OX} = 10 and several ratios S_1/S_2. As noted above, biasing according to Eq.(5) yields exaggerated S values, reaching a record 7 mV/decade value for S_2/S_1 = 1. This extravagant result is due to the fact that the backgate bias was actually 10 times larger than required by Eq. (5). Since the swing is referred to the frontgate bias V_G, the resulting S appears 10 times lower. For comparison, a proper device biasing according to Eq.(5) results in a reliable value of 67 mV/decade, as shown in Fig. 4(b). Of course, in extremely thin transistors, where C_{Si} dominates, Eqs. (4) and (5) do not differ as markedly.

- *Strong inversion*

In strong inversion Eq. (4) holds, but the question still arises: since V_{T1} depends on V_{BG} and V_{T2} depends on V_G, what threshold values should we use?

In the literature, a common choice is V_{T1} and V_{T2} measured with the opposite gate grounded – but this is not accurate. Genuine DG operation and volume inversion implies that strong inversion is reached *simultaneously* in both channels. Therefore, the correct V_{T1} and V_{T2} threshold values correspond to the intersection between $V_{T1}(V_{BG})$ and $V_G(V_{T2})$ plotted in Fig. 3. Thus, Fig. 5(a) shows transconductance curves, measured for threshold value pairs (V_{T1}, V_{T2}) indicated by the points A, B, C and D in Fig. 3(a). The transconductance is highest close to the intersection point B; it decreases when the channels are unbalanced (A and D).

In ultrathin films, the bias selection is even murkier, as the two curves in Fig. 3(b) merge. We argue that all points located on the common curve of Fig. 3 (b) are acceptable. To clarify this point, consider an arbitrary backgate bias, for example V_{G2} = 10 V. We now select the corresponding threshold frontgate bias V_G = –0.68 V, as shown in Fig. 3(b). The potential is quasi-flat across the ultrathin Si film (rectangular well). Raising Si potential by $2\Phi_F$ at the top oxide interface also raises the potential at the BOX interface by the same value. In other words, an arbitrary bias V_{BG} works as the threshold voltage for the back channel.

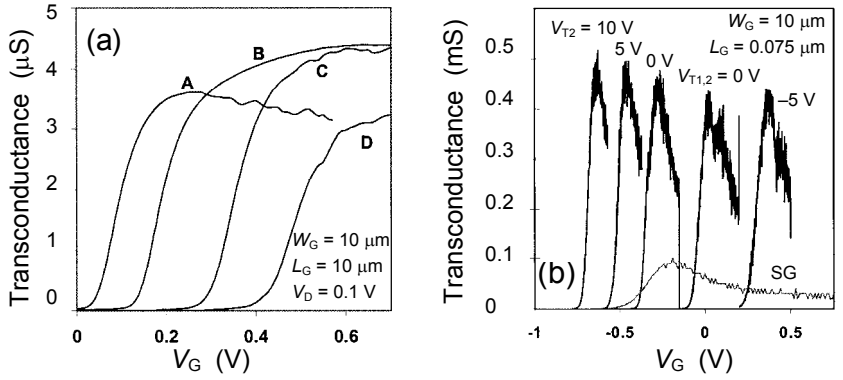

Figure 5. Transconductance in DG mode of SOI MOSFETs with (a) t_{Si} = 47 nm, V_D = 0.1 V and (b) t_{Si} = 9 nm, V_D = 0.05 V for various (V_{T1}, V_{T2}) choices.

This is experimentally confirmed in Fig. 5(b). The curves are obviously shifted as the offset voltages $V_{T1,2}$ are modified, but the transconductance peak remains nearly constant. It is worth noting that the residual variation of the transconductance peak may be due to the modulation of the series resistance by the backgate. According to Allibert and co-workers,[27] a more positive V_{BG} induces volume inversion in the film and also accumulation at the bottom of source and drain extensions. This reduces the series resistance and increases the transconductance peak.

The outstanding feature in Fig. 5(b) is that the transconductance peak in DG is much more than double the SG peak, whereas only a doubling of the transconductance can be attributed to the doubling of the inversion charge. The superior gain tends to support earlier results which have claimed an improved carrier mobility in DG mode.[12,28,29,30] The behavior of carrier mobility in ultrathin DG transistors is far from established, because several competing mechanisms come into play. A discussion is offered by Esseni and co-workers elsewhere in this volume.

5. Vertical tunneling operation

In this section we report on the operation of our ultrathin SOI transistors in the vertical tunneling mode. The devices underwent the same standard SOI process steps, with L_G = 0.1 μm gate length, W_G = 10 μm, and the Si channel thinned down to ~5 nm to foster size quantization. The key difference from our other ultrathin SOI MOSFETs discussed in the preceding sections is that the gate oxide is reduced to ~1 nm to create a tunneling barrier. Nonetheless, these devices exhibit good transistor $I_D(V_G)$ and $I_D(V_{BG})$ curves at both room and cryogenic temperatures – see Fig. 6.

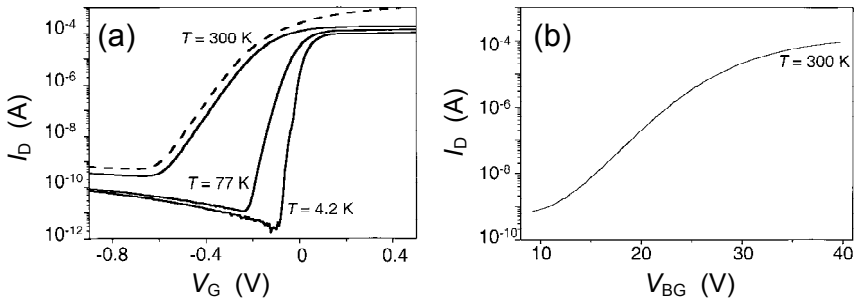

Figure 6. (a) Standard $I_D(V_G)$ transfer characteristics at T = 300, 77, and 4.2 K for V_D = 0.1 V (and V_D = 0.6 V at T = 300 K, dashed line), V_{BG} = 0. (b) Backgate $I_D(V_{BG})$ transistor characteristics for V_D = 0.1 V, V_G = –0.8 V at T = 300 K.

Standard transistor $I_D(V_G)$ at $V_{BG} = 0$ and $V_D = 0.1$ V are shown in Fig. 6(a) for $T = 300$, 77, and 4.2 K. Because of n^+-poly gate material, the threshold $V_T < 0$, but otherwise the room-temperature characteristics show good subthreshold slope and acceptable drain-induced barrier lowering (compare $V_D = 0.1$ and 0.6 V at $T = 300$ K). Once the channel is depleted with $V_G < V_T$, an even more negative V_G results in a slowly increasing and relatively temperature-insensitive tunneling current through the ultrathin gate oxide. Figure 6(b) shows the room-temperature backgate operation $I_D(V_{BG})$ at $V_G = –0.8$ V and $V_D = 0.1$ V.

At low $T = 4.2$ K temperature we observe two quantum effects. First, at $V_G <$ –0.1 V and small $V_D = 1$ mV, the drain current $I_D(V_{BG})$ exhibits clear steps near the threshold as the transistor is turned on by V_G – see Fig. 7(a). These steps, which persist in a weaker fashion at $T = 77$ K, correspond to quantized subbands in the Si channel being pulled down below the source Fermi level. As is clear from Fig. 7(b), changing frontgate V_G shifts the $I_D(V_{BG})$ curve along the V_{BG} axis: for ΔV_G = 12.5 mV, the corresponding $\Delta V_{BG} \sim 0.6$ V due to ratio of t_{BOX} to the combination of $(t_{OX} + t_{Si})/2$. The results of Fig. 7 are quite similar to the Si quantum dot transistors,[14-16] except that in dots the I_D exhibits sharp peaks followed by NDR regions corresponding to tunneling into discrete states, whereas here we have tunneling into effectively two-dimensional (2D) subbands E_N in the channel. Since these 2D subbands contain higher-energy states corresponding to in-plane motion, the NDR is weakened by impurity and phonon scattering-assisted tunneling into these states.[31] Also, inhomogeneities in the Si channel thickness and the SiO_2/Si interface are certain to broaden E_N and, hence, the $I_D(V_{BG})$ steps.

Given the existence of quantized 2D subbands E_N in the Si channel and a tunneling t_{OX} we can operate the device as a three-terminal vertical tunneling transistor (VTT). The drain current in the VTT is due only to tunneling from the gate (the source is shorted to drain) and V_{BG} is used to modulate I_D by changing

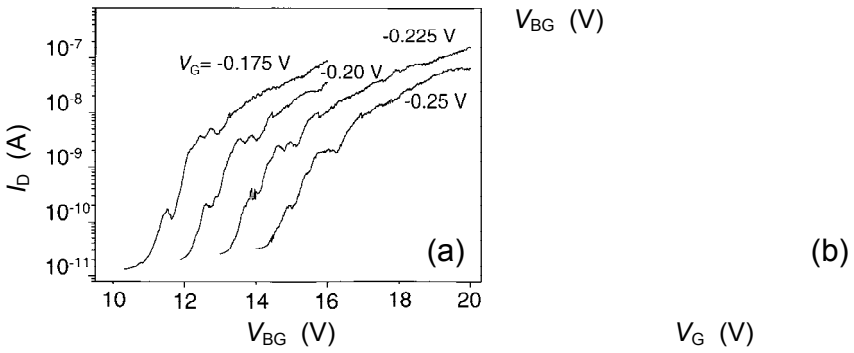

Figure 7. (a) Drain current $I_D(V_{BG})$ characteristic at T = 4.2 K and V_D = 1 mV for several values of $V_G < V_{T1}$. The current steps correspond to the population of quantized subbands E_N in the channel under the gate. (b) Linear variation of the V_{BG} position of the first current step in (a) plotted against V_G.

alignment of E_N with the occupied states in the gate. This type of operation was first discussed by Luryi in the context of the quantum capacitance mechanism[24] and first observed in III–V structures by Morkoç and co-workers.[32]

Figure 8 illustrates the quantum capacitance mode of operation of this device. The gate is grounded and acts as the "emitter", the source and drain electrodes are shorted and biased to V_D, and I_G is modulated by the substrate voltage V_{BG} which induces an electric field and alters the alignment between the channel and the gate.[24,18] The schematic vertical band diagram through the midpoint of the device and the tunneling current are shown in Fig. 8(a), with the $t_{OX} \sim 1$ nm acting as the thin first barrier, the BOX acting as an impenetrable second barrier, and t_{Si} acting as the QW containing 2D subbands E_N (only E_1 is shown). Electrons tunnel from the n^+-poly-Si gate into E_1 and are extracted laterally via the source and drain contacts. The tunneling I_G is the only current component in this biasing mode (no measurable substrate leakage is observed for any V_{BG}). As in all RT structures, this tunneling I_G depends on the alignment of E_1 with the occupied states in the gate. Once E_1 is lowered below the bottom of the occupied states in the gate, I_G is cut off by the energy and transverse momentum conservation.[17] In an ideal structure, this should lead to a sharp negative transconductance, $g \equiv dI_G/dV_{BG} < 0$.

The first signature of Si VTT operation can be seen in Fig. 8(b), where we plot the $I_G(V_{BG})$ and the transconductance g for $V_G = 0$ and $V_S = V_D = 0.2$–0.35 V. For a given value of V_D, as V_{BG} is increased from zero, g first increases and then drops, with one or more (at higher V_D) clear minima in-between. The initial increase of g with V_{BG} corresponds to the V_{BG}-induced lowering of E_1 with respect to the gate, leading to a higher tunneling I_G. The eventual drop in g at large

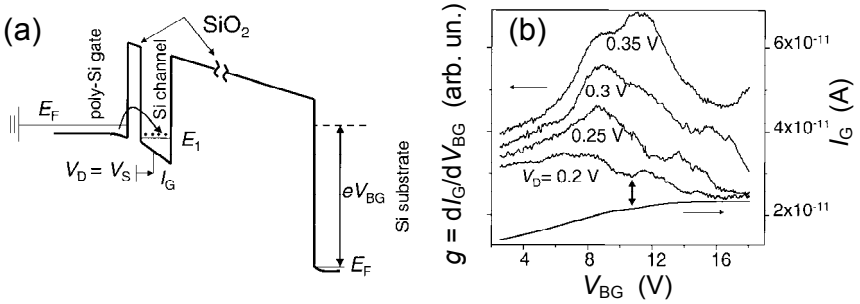

Figure 8. (a) Schematic vertical band diagram through the device midpoint under bias, indicating electron tunneling into the lowest 2D subband E_1 of the quantized Si channel and their subsequent lateral extraction via the (shorted) source and

drain contacts. Backgate V_{BG} alters the alignment of E_1 with poly-Si gate E_F and modulates the tunneling current. (b) Tunneling $I_G(V_{BG})$ characteristic at T = 4.2 K for $V_S = V_D$ = 0.2 V (arrow marks the transconductance $g \equiv \partial I_G/\partial V_{BG}$ minimum), together with smoothed $g(V_{BG})$ for various $V_S = V_D$ = 0.2–0.35 V.

$V_{BG} > 15$ V corresponds to a large carrier density being established in the Si channel. The tunneling oxide emitter barrier is then completely screened from the electric field produced by V_{BG}. The minima in g at intermediate V_{BG} correspond to the E_N subband going out of alignment with the occupied states in the gate. The transconductance g does not actually go negative, as the effect is weakened by energy or transverse momentum nonconserving tunneling, as well as broadening of E_1 due to Si channel fluctuations, and the possible inhomogeneous broadening of the emitter states in the gate electrode due to quantum-size energy shifts in small poly-Si grains.[33] The actual alignment of the 2D subbands with the gate is a complex electrostatic problem that will be the subject of future study.

In estimating the potential impact of such devices, it is worth noting that an analogous RT structure was originally fabricated in a III–V heterostructure by Morkoç and co-workers.[32] There, both barriers were AlGaAs, with a much thicker second barrier ensuring the isolation between the GaAs QW and the substrate. The main difficulty in the III–V implementation was making good contact to the QW without leakage to the substrate. This problem is absent in SOI devices, where the buried oxide is essentially impenetrable. For the current generation of UNIBOND substrates, the required V_{BG} to shift quantized subbands in the Si channel runs to >10 V because t_{BOX} = 400 nm, but much thinner buried oxides will become available as SOI transistors are scaled down.

4. Conclusions

To summarize, we have addressed the typical coupling effects in ultrathin film SOI MOSFETs. The accurate bias for emulating DG operation in thin and ultrathin devices has been reexamined, based on our measurements of threshold shifts with front and backgate bias. In a 9 nm thick SOI MOSFET, super-coupling between the front and back interfaces was experimentally confirmed: inversion of one interface simultaneously induces inversion at the opposite interface.

The analysis of the coupling effects enabled us to propose a correct procedure for achieving virtual DG mode operation. In weak inversion, the subthreshold swing ratio between front and back channels should be used, instead of the oxide thickness ratio. Furthermore, the threshold voltages V_{T1} and V_{T2} should be chosen carefully: the threshold voltage of each interface must be measured with the opposite interface in inversion. Using this method, we have found experimentally that the transconductance in virtual DG mode operation is dramatically improved, with a gain markedly exceeding a factor of two as compared to SG operation. This confirms the promise of ultrathin DG SOI MOSFETs for further scaling.

We have also reported on the dual functionality of ultrathin SOI devices with very thin tunneling oxides. Our proof-of-concept SOI vertical tunneling

transistors combine standard transistor $I_D(V_G)$ transfer characteristics at large V_D with backgate control of the tunneling current $I_G(V_{BG})$ as the source and drain are shorted and the front gate is used as the tunneling emitter. For now, features in the tunneling transconductance are observed at T = 4.2 K, but with improved fabrication the operating temperature will increase. Our tunneling transistors offer, at least in principle, the prospect of enhancing silicon ICs with SOI tunneling devices featuring functionally useful nonlinear and NDR characteristics.

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References

1. The latest publicly released version of the ITRS roadmap is available on the http://public.itrs.net web site.
2. S. Cristoloveanu and S. S. Li, *Characterization of Silicon-On-Insulator Materials and Devices*, Boston: Kluwer Academic Publishers, 1995, p 381.
3. P. M. Solomon "Strategies at the End of CMOS Scaling," in: S. Luryi, J. M. Xu, and A. Zaslavsky, eds., *Future Trends in Microelectronics: The Nano Millennium*, New York: Wiley-Interscience, 2002, pp. 28–42.
4. G. K. Celler and S. Cristoloveanu, "Frontiers of silicon-on-insulator," *J. Appl. Phys.* **93**, 4955 (2003).
5. H-S. Wong, D. J. Frank, and P. M. Solomon, "Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFETs at the 25nm channel length generation," *Tech. Digest IEDM* (1998), p. 407.
6. J.-P. Colinge, *SOI Technology: Materials to VLSI*, 2nd ed., Boston: Kluwer, 1997.
7. F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon on insulator transistor with volume inversion: a new device with greatly enhanced performance," *IEEE Electron Dev. Lett.* **8**, 410 (1987).

8. D. Hisamoto, T. Kaga, and E. Takeda, "Impact of the vertical SOI 'DELTA' structure on planar device technology," *IEEE Trans. Electron Dev.* **3**, 1419 (1991).
9. J. Kedzierski, M. Ieong, and E. Nowak, "Issues in high performance FinFET and FDSOI transistor design," in: S. Cristoloveanu *et al.*, eds., *Silicon-on-Insulator Technology and Devices XI*, Pennington, NJ: Electrochemical Society Press, 2003, pp. 185–196.
10. X. Huang, W-C. Lee, C. Kuo, *et al.*, "Sub 50-nm fin-FET: PMOS," *Tech. Digest IEDM* (1999), p. 67; X. Huang, W-C. Lee, C. Kuo, *et al.*, "Sub 50-nm fin-FET," *IEEE Trans. Electron Dev.* **48**, 880 (2001).
11. S. Xiong and J. Bokor, "Sensitivity of double-gate and fin-FET devices to process variations," *IEEE Trans. Electron Dev.* **50**, 2255 (2003).
12. T. Ernst, S. Cristoloveanu, G. Ghibaudo, *et al.*, "Ultimately thin double-gate SOI MOSFETs," *IEEE Trans. Electron Dev.* **50**, 830 (2003).
13. D. Esseni, M. Mastrapasqua, C. Fiegna, G. K. Celler, L. Selmi, and E. Sangiorgi, "An experimental study of low filed electron mobility in double-gate, ultra-thin SOI MOSFETs," *Tech. Digest IEDM* (2001), p. 445.
14. Y. Takahashi, M. Nagase, H. Namatsu, *et al.*, "Fabrication technique for Si single-electron transistor operating at room temperature," *Electron. Lett.* **31**, 136 (1995).
15. E. Leobandung, L. Guo, Y. Wang, and S. Y. Chou, "Observation of quantum effects and Coulomb blockade in silicon quantum-dot transistors at temperatures over 100 K," *Appl. Phys. Lett.* **67**, 938 (1995); E. Leobandung, L. Guo, and S. Y. Chou, "Single hole quantum dot transistors in silicon," *ibid.* **67**, 2338 (1995).
16. M. Saitoh, T. Saito, T. Inukai, and T. Hiramoto, "Transport spectroscopy of the ultrasmall silicon quantum dot in a single-electron transistor," *Appl. Phys. Lett.* **79**, 2025 (2001), also see T. Hiramoto's chapter in this volume.
17. S. Luryi, "Frequency limit of double-barrier resonant-tunneling oscillators," *Appl. Phys. Lett.* **47**, 490 (1985).
18. An overview of the quantum effect tunneling devices is available, for example, in S. Luryi and A. Zaslavsky, "Quantum effect and hot electron devices," chapter in: S. M. Sze, ed., *Modern Semiconductor Device Physics*, New York: Wiley-Interscience, 1998, pp. 253-341.
19. H. C. Liu, D. Landheer, M. Buchanan, and D. C. Houghton, "Resonant tunneling in $Si/Si_{1-x}Ge_x$ double-barrier structures," *Appl. Phys. Lett.* **52**, 1809 (1988).
20. U. Gennser, V. P. Kesan, D. A. Syphers, T. P. Smith III, S. S. Iyer, and E. S. Yang, "Probing band structure anisotropy in quantum wells via magneto-tunneling," *Phys. Rev. Lett.* **67**, 3828 (1991).
21. J. Liu, A. Zaslavsky, and L. B. Freund, "Strain-Induced quantum ring hole states in a gated vertical quantum dot," *Phys. Rev. Lett.* **89**, 096804 (2002).

22. M. Watanabe, Y. Iketani, and M. Asada, "Epitaxial growth and electrical characteristics of CaF_2/Si/CaF_2 resonant tunneling diode structures grown on Si(111) 1°-off substrate," *Jpn. J. Appl. Phys. Part 2* **39**, L964 (2000); T. Terayama, H. Sekine, and K. Tsutsui, "Fluoride resonant tunneling diodes co-integrated with Si-MOSFETs," *Jpn. J. Appl., Phys. Part 1* **41**, 2598 (2002).
23. A. Zaslavsky, C. Aydin, S. Luryi, S. Cristoloveanu, D. Mariolle, D. Fraboulet, and S. Deleonibus, "Ultrathin silicon-on-insulator vertical tunneling transistor," *Appl. Phys. Lett.* **83**, 1653 (2003).
24. S. Luryi, "Quantum capacitance devices," *Appl. Phys. Lett.* **52**, 501 (1988).
25. H.-K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFETs," *IEEE Trans. Electron Dev.* **30**, 1244 (1983).
26. S. S. Sinha, A. Zaleski, and D. E. Ioannou, "Investigation of carrier generation in fully depleted enhancement and accumulation mode SOI MOSFETs," *IEEE Trans. Electron Dev.* **41**, 2413 (1994).
27. F. Allibert, A. Zaslavsky, J. Prétet and S. Cristoloveanu, "Double-gate MOSFETs: Is gate alignment mandatory?" *Proc. ESSDERC* (2001), p. 267.
28. F. Gámiz, J. B. Roldán, J. A. López-Villanueva, P. Cartujo-Cassinello, and F. Jiménez-Molinos, "Monte Carlo simulation of electron mobility in silicon-on-insulator structures," *Solid State Electronics* **46**, 1715 (2002).
29. D. Esseni, M. Mastrapasqua, G. Celler, C. Fiegna, L. Selmi, and E. Sangiorgi, "An experimental study of mobility enhancement in ultrathin SOI transistors operated in double-gate mode," *IEEE Trans. Electron Dev.* **50**, 802 (2003).
30. C. Fiegna, A. Abramo and E. Sangiorgi, "Single- and double-gate SOI MOS structures for future ULSI: A simulation study," in: S. Luryi, J. M. Xu, and A. Zaslavsky eds., *Future Trends in Microelectronics: The Road Ahead*, New York: Wiley-Interscience, 1999, pp. 115–124.
31. V. J. Goldman, D. C. Tsui, and J. E. Cunningham, "Evidence for LO-phonon-emission-assisted tunneling in double-barrier heterostructures," *Phys. Rev. B* **36**, 7635 (1987).
32. H. Morkoç, J. Chen, U. K. Reddy, T. Henderson, and S. Luryi, "Observation of a negative differential resistance due to tunneling through a single barrier into a quantum well," *Appl. Phys. Lett.* **49**, 70 (1986).
33. N. Lifshitz, S. Luryi, and T. T. Sheng, "Influence of the grain structure on the Fermi level in polycrystalline silicon: A quantum size effect?" *Appl. Phys. Lett.* **51**, 1824 (1987).