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Influence of a Resistive Sublayer at the Polysilicon/Silicon Dioxide Interface on MOS Properties

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Abstract—**We suggest that a thin ($\lesssim$100 Å) resistive sublayer of polysilicon near the oxide interface can have a pronounced effect on the MOS capacitance-voltage characteristics. On the depletion side of the *C-V* curve, the lower effective work-function difference leads to a higher threshold for strong inversion. On the accumulation side, the MOS capacitance is lowered due to the added thickness of the depletion sublayer.**

With the help of the sublayer model, we attempt to explain the anomalous behavior often observed in MOS capacitors with silicide/polysilicon gates. The sublayer depletion activates traps due to the heavy impurities (Cu, Fe, and Ta) at the interface, a considerable amount of which were observed in these samples by Auger spectroscopy.

I. INTRODUCTION

IT IS WELL KNOWN that MOS capacitance-voltage curves and MOSFET thresholds are sensitive to the presence of various states in oxide and at the silicon-oxide interface [1]. One is usually concerned with the state of the Si/SiO_2 interface or with charged states within the gate oxide but rarely with those on the outer interface of the oxides. Of course, neglecting the latter is well justified when the layer immediately over the oxide is a metal or highly doped polysilicon.

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The situation may be quite different when the doping profile in a polysilicon gate is nonuniform. In particular, one may have a very thin (~100 Å) but resistive sublayer of polysilicon immediately adjacent to the gate oxide. The existence of such a layer can be brought about by the very presence of the poly/oxide boundary which serves as a natural stop for the diffusion of certain deep-level impurities, such as Cu and Fe. Moreover, in the vicinity of the interface, a greater percentage of donor impurities is inactive compared to that in the bulk of polysilicon which also contributes to enhanced resistivity.

The presence of this resistive sublayer would produce little effect on such characteristics as sheet resistivity of the polysilicon. On the other hand, it should manifest itself through a degradation of MOS *C-V* characteristics. Qualitatively, for n-poly gate and p-subtrate, the effect is twofold. First, the slope of *C-V* curves becomes less steep and threshold voltage of n-channel devices is shifted to higher voltages. Secondly, the MOS capacitance in the flat-band to weak-accumulation region of the *C-V* curve is lower due to the finite thickness of the resistive sublayer. The latter effect is unobservable on the depletion side of the curve and disappears in strong accumulation.

The purpose of this paper is to suggest a possible explanation to the unusual behavior often observed in MOS devices containing a silicide-polysilicon gate structure with the metal silicide

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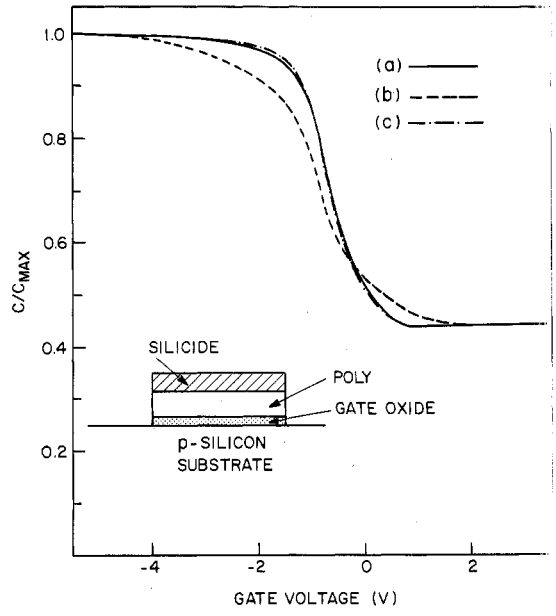

Fig. 1. *C-V* characteristics of MOS capacitor with silicide gates; (*a*) before sintering; (*b*) after 30-min sintering at 900°C; (*c*) after subsequent phosphorus diffusion (15 min, 900°C) with silicide layer removed.

produced by sputtering and sintering. They consistently exhibited degraded *C-V* characteristics after high-temperature sintering. We believe that our model, which postulates the existence of a resistive sublayer at poly-SiO_2 interface, can account for all essential features of the observed behavior. From the observed *C-V* curves we make an estimate of the required thickness of the resistive layer to be of order 60 Å, which is not unreasonable. Furthermore, our model is indirectly supported by Auger data [4] which showed a large concentration of heavy impurities at the poly/SiO_2 interface. It is probable that these impurities (Cu and Fe) segregate at the interface during the sintering step.

II. Experimental

Thermal oxide 4000 Å thick was grown on Wacker p-type ⟨100⟩ oriented wafers. The wafers were implanted through the oxide with boron to achieve a carrier concentration of $4 \times 10^{16}cm^{-3}$ at the Si/SiO_2 interface. The oxide was subsequently etched away and a 250-Å-thick gate oxide was grown. A polysilicon layer of thickness 3500 Å was then deposited and doped with phosphorus by diffusion from PBr_3 source. Tantalum silicide layer (2500 Å) was cosputtered on polysilicon surface. The structure was then patterned and reactive ion etched so as to form MOS capacitors with poly/silicide upper electrodes.

After patterning, the samples were sintered at 900°C for 30 min in Ar atmosphere to form a stable low-resistivity $TaSi_2$ [2]. It was noticed that after the high-temperature sintering, *C-V* characteristics underwent a drastic change.

A typical result is shown in Fig. 1. Before sintering, the shape of the curve (*a*) is similar to that usually obtained with the polysilicon gate (without silicide). After sintering, the *C-V* curve (*b*) behaves in a manner similar to that usually attributed to the presence of a large number of interface traps [3]. This characteristic behavior includes a degraded and uneven slope as well as a washed out threshold point. The unwelcome changes were clearly introduced during the sintering. An additional high-temperature anneal produced no improvement in the characteristics.

Although the *C-V* characteristics shown in Fig. 1 [curves (*a*) and (*b*)] can undoubtedly be explained in a conventional way, assuming interface traps and fixed oxide charges at the Si/SiO_2 interface, such an explanation would necessarily involve a number of *ad hoc* assumptions. In particular, one would have to postulate a special combination of interface traps and fixed oxide charges in order to explain the observed intersection of curves (*a*) and (*b*). Moreover, such a peculiar combination would appear unlikely to result from a short 900°C sintering step. We were, therefore, led to consider an alternative explanation, based on the idea that it was the state of the outer interface, viz., SiO_2/poly, rather than that of the inner oxide interface, that was responsible for the degradation of the *C-V* characteristics.

To confirm this hypothesis, we took some of the samples which exhibited the after-sintering characteristic [Fig. 1, curve (*b*)] and etched the silicide away. After this step, the measured curves were still identical to curve (*b*). However, after 15 min of phosphorus diffusion at 900°C, the MOS characteristics returned to their original undistorted shape, [Fig. 1, curve (*c*)]. In our view, this experiment gives a conclusive evidence of the importance of the outer interface since a brief diffusion step could not possibly affect the inner interface. Furthermore, we carried out another experiment which also resulted in a complete rehabilitation of the degraded capacitors. This time we did not remove the silicide. After high-temperature sintering, the silicide gates were implanted with arsenic (60 kV with 7×10^{15}-cm^{-2} dose). After the implantation, devices were covered by CVD oxide (1200 Å thick) and annealed at 900°C for 1 h. Next, windows to the silicide gates were patterned and etched through the oxide, and then the *C-V* characteristics were taken again. This time we found the original ideal curves shown in Fig. 1, curve (*a*). It should be emphasized that a similar treatment *not* preceded by implantation of As into the silicide produced no change in the degraded *C-V* characteristics. Our explanation of this effect will be discussed in Section IV.

III. The Model

Our model assumes that during the high-temperature sintering, heavy impurities (e.g., Cu or Fe), which are present in the silicide or polysilicon, diffuse in polysilicon towards the oxide and sink at the interface, giving rise to a high density of surface traps of acceptor type. On the other hand, the dopant concentration in polysilicon during high-temperature sintering is decreased due to diffusion of phosphorus into silicides. The compensation effect of the surface traps brings about the formation of a highly resistive layer in polysilicon.

Next, we consider the band diagram of the gate structure, Fig. 2. At equilibrium, $V_G = 0$, the silicon layer under the oxide is in depletion (Fig. 2(a)). The broken lines correspond to the presence of a depleted sublayer of polysilicon and solid lines show the case of a uniformly and heavily doped polysilicon.

Consider now how our model explains the essential features of the observed *C-V* characteristics. First, we note that the

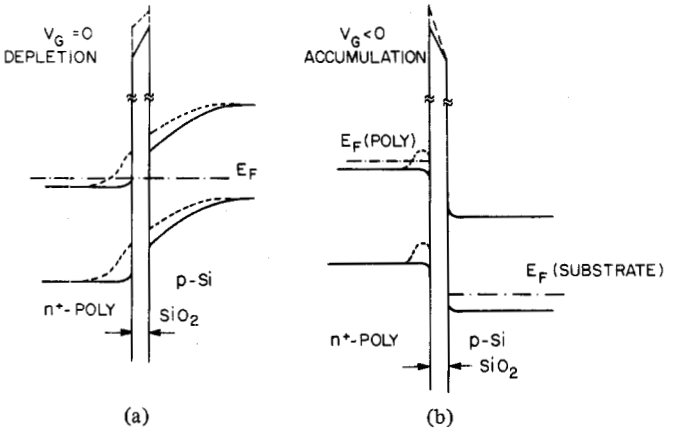

Fig. 2. Band-diagrams of the polysilicon-oxide-silicon gate structure. (a) Depletion or weak inversion at $V_G = 0$. (b) Accumulation, $V_G < 0$. For clarity, the pictures are drawn with different scales in polysilicon (where the depletion depth is of order 100 Å or less) and Si (where this depth is $\lesssim 1$ μm).

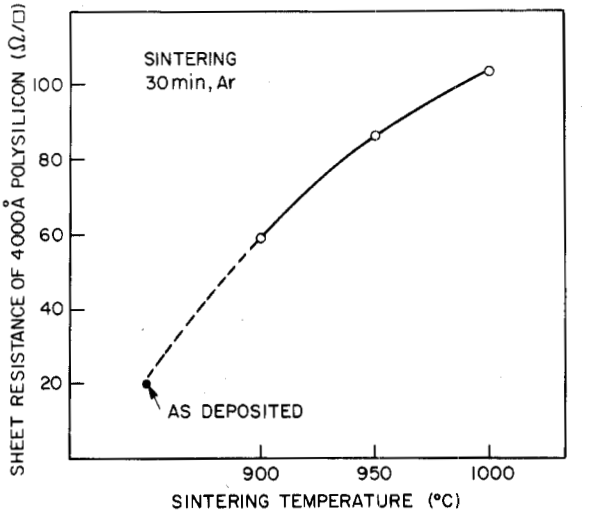

Fig. 3. Sheet resistance of 4000-Å polysilicon film after 30-min sintering with a tantalum silicide cap. The increase in resistivity is associated with the depletion of phosphorus caused by its diffusion into the silicide.

existence of the resistive layer lowers the built-in voltage between the n-polysilicon gate and the p-Si substrate. This clearly increases the threshold voltage for strong inversion. In depletion at the same applied voltage, e.g., at $V_G = 0$, the electric field in the oxide is less than in the ideal case, shown in Fig. 2(a). This leads to a narrower depletion region in silicon and hence a higher capacitance. Qualitatively, this effect is similar to the usual case when the traps are on the Si/SiO_2 interface. As usual, charging and discharging of the fast traps leads to a degraded slope of the C-V curve [3].

However, the crossing of the original and degraded curves is peculiar to our model. In weak accumulation (Fig. 2(b)) the existence of a depleted sublayer results in *lower* capacitance. It is easy to show that this sublayer of thickness d gives rise to a relative change in the capacitance $\Delta C/C$ given by

$$\frac{\Delta C}{C} = \frac{d}{d_{ox}} \frac{\epsilon_{ox}}{\epsilon}$$

where d_{ox} is the oxide thickness (~250 Å) and ϵ_{ox}, and ϵ are, respectively, the oxide and the polysilicon dielectric constants. The maximum $\Delta C/C$ occurs at $V_G \approx -1.4$ V and equals approximately 7 percent which gives $d \approx 60$ Å. Such thickness of the resistive layer seems to us not unreasonable. We can also estimate from Poisson's equation the required density N^- of fixed negative charge which accounts for the band bending in the depleted layer of polysilicon. With the above value for d one finds, typically, N^- of order $10^{19}\,cm^{-3}$. The actual amount of this charge is determined self-consistently by the position of the bands with respect to the Fermi level and it varies with the applied bias. At higher negative voltages, the depleted region is no longer present and the capacitance reaches the ideal value associated only with the oxide.

Auger spectroscopy studies [4] of samples consisting of a sandwich of SiO_2, polysilicon, and Ta silicide give further support to our model. High density of impurities, such as Cu, Fe, and Ta, was found at the poly-SiO_2 interface of the samples. The bulk of polysilicon did not show the presence of any of these impurities. The results indicate that the poly-SiO_2 interface indeed behaves as a sink for impurities. When polysilicon under silicide is heavily doped with the mobile charge uniformly extending down to the contaminated interface, the latter cannot affect the MOS properties of the capacitor. However, during high-temperature treatment, redistribution of phosphorus between poly and $TaSi_2$ occurs. Furthermore, it is likely that the source of heavy impurities is contained within the $TaSi_2$ layer so that during the high-temperature sintering the density of these impurities in polysilicon is increased due to diffusion from the source. Quite generally, the effect of the heavy impurities is compensating as they trap and deplete the mobile charge. In Fig. 3, we plot sheet resistance of a poly layer 4000 Å thick covered by a $TaSi_2$ layer as a function of sintering temperature (30 min in Ar). After each temperature cycle, the silicide layer was plasma etched and the sheet resistance of the poly layer measured. Original sheet resistance was 20 Ω/□. It grew to 59 Ω/□ during the 900°C sintering which is a standard process step. It is plausible that this change is associated with a combination of depletion and compensation of polysilicon away from the oxide interface. As discussed previously, these effects are more severe near the boundary. Under such conditions the detrimental effects of the contaminated interface come into play.

IV. Discussion

We have suggested a model which shows that under certain circumstances the state of the outer oxide interface (polysilicon/SiO_2) can have a tangible detrimental effect on the MOS properties of capacitors and transistors with polysilicon gates. It is an essential part of our model that a thin ($\leqslant$100 Å) depleted sublayer can exist in polysilicon near the oxide boundary. In the presence of the depleted sublayer impurities, such as Co, Fe, and Ta which readily diffuse through poly layer and are stopped by oxide, form traps at the poly-SiO_2 interface and degrade the MOS properties of the structure. With the help of our model we have suggested a tentative explanation for the observed anomalous behavior of MOS capacitors with silicide/polysilicon gates.

Further experimental work is clearly required to confirm or reject our hypothesis. Of particular interest are the mechanisms responsible for the formation and destruction of the depleted sublayer. We have suggested that the sublayer is formed during the sintering step due to diffusion of heavy impurities from a naturally contaminated tantalum silicide. (It should be noted that we observed quite similar effects on samples covered with $CoSi_2$.) We are less certain about the mechanism responsible for the rehabilitation of the MOS properties of the same devices at the end of the MOSFET fabrication sequence. In one set of our experiments the "cure" was brought about during a brief phosphorus diffusion at 900°C, with silicide removed. It is possible that during this step, an outdiffusion of heavy impurities occurred from the interface into the bulk of polysilicon.[1] On the other hand, a mere enhancement of the mobile charge concentration by the diffusion of phosphorus could also eliminate the depleted sublayer. It appears that the second mechanism (with As rather than P being the additional dopant) was operating in the other set of our experiments discussed at the end of Section II.

In these experiments, the rehabilitation of C-V characteristics was brought about by ion implantation of As into the silicides followed by a 900°C anneal. We believe that during the anneal, arsenic diffuses through the silicide and polysilicon reaching the SiO_2 interface. Our experiments show that the degradation of C-V curves is not very sensitive to the duration of sintering and that most of the change occurs during the first 15 min. This means that the flow of heavy impurities from the silicide falls off before the sintering is over. Therefore, no new traps are formed during the high-temperature anneal after As implantation, while the influx of arsenic produces additional mobile charge in the vicinity of SiO_2 interface and eradicates the resistive sublayer.

In our view, it is this mechanism which is responsible for rehabilitation of the MOS properties at the end of the MOSFET fabrication sequence used in our laboratory. In this sequence, the source and drain contacts are formed by arsenic implantation. During the implantation, the polysilicon/silicide gates (which serve as a self-aligned mask) are exposed to the ion beam.

We have discussed one aspect of the impurity exchange in the polysilicon/silicide system. In general, this phenomenon can be very important in device fabrication and, in our opinion, it deserves a thorough investigation.

[1] This mechanism was suggested by H. J. Levinstein.

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