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Title: **Wafer - Coordinates Identification of Integrated - Circuit Chips**

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ABSTRACT

We describe simple means of recording the coordinates of each chip of an integrated circuit wafer on the chip itself. The information is recorded in the form of a map of wafer, which, in addition to preserving a measurable record of the exact position in the array from which the chip was separated, provides a visual determination, either approximate or exact, of the chip's position in the wafer array. The proposed method can be accomplished with as few as two extra cards in the array deck, as opposed to 45 to 50 cards required by the presently used coordinate numbering. A further advantage of our method is that the positional information recorded in the map is easily machine-readable.

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MEMORANDUM FOR FILE

It is sometimes necessary to know the exact position in the IC wafer array from which a separated chip has been taken. Such a need arises, for example, when one wishes to correlate the statistics of chip failures in the field with chip location on the wafer. The recorded coordinate information can also be useful in providing a means of production control in cases in which processing parameters are intentionally varied across the wafer to bracket a desired electrical characteristic. This information is expected to be of particular importance whenever one deals with device structures whose behaviour is critically dependent upon their vertical composition, such as the oxide thickness for ultrathin oxides or thicknesses of layers grown by Molecular Beam Epitaxy.

An obvious way of providing the positional information is to print on each chip its Cartesian coordinates. This method of chip labeling is presently used in BTL bubble technology. Although the coordinate information is thus given directly, it is not easily machine-readable. Furthermore, writing the coordinate numerals on each chip requires an extra 45 to 50 cards in the wafer array deck.

In contrast, the method described in this memo requires only two extra cards. The recorded positional information is illustrated in Fig. 1. (The corresponding Cartesian coordinates are also

shown). Each of the nine chips forming a 3×3 array contains a fixed square (rectangle, generally) called the bounding matrix. This matrix represents a map of the entire wafer. The black square seen in a different position on each map marks the geographical location of its chip on the wafer. This square, called the mapping dot is a separate chip arrayed to overlie the primary array at a slightly greater step-and-repeat spacing in both x and y directions. The resulting picture of a dot moving with respect to the bounding matrix by increments δx and δy contains all the positional information.

This information is read as follows. Let Δx and Δy be the step and repeat spacings of the primary chip array, and $\Delta x + \delta x$ and $\Delta y + \delta y$ be those of the mapping dot array. Let n_x and n_y be the coordinate indices of a particular chip, so that the products $n_x \Delta x$ and $n_y \Delta y$ represent the coordinate distances of this chip from the origin. By measuring the offsets d_x and d_y of the mapping dot from the edges of the bounding matrix we can determine the indices n_x and n_y, viz.

$$\begin{aligned} n_x &= d_x/\delta_x \\ n_y &= d_y/\delta_y \end{aligned} \tag{1}$$

It is also easy to determine the coordinate indices visually. To facilitate this we have added an interior grid to the bounding matrix, cf. Fig. 2. If the grid spacing be made no more than 5 times δx and δy, then the exact visual determination of coordinate indices should pose no problem. The lower left-hand corner of the matrix is distinguished as the origin by a special mark. The actual reference point on the mapping dot is also its lower left-hand corner.

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Atts.
Figure Captions
Figures 1 & 2

FIGURE CAPTIONS

Fig. 1 Schematic illustration of coordinate identification on a 3 × 3 chip array, showing both the moving dot method of this memo and the presently used labeling of coordinate indices.

Fig. 2 RAPID - coded plot of a mapping matrix with the mapping dot overlying it at (10, 10).

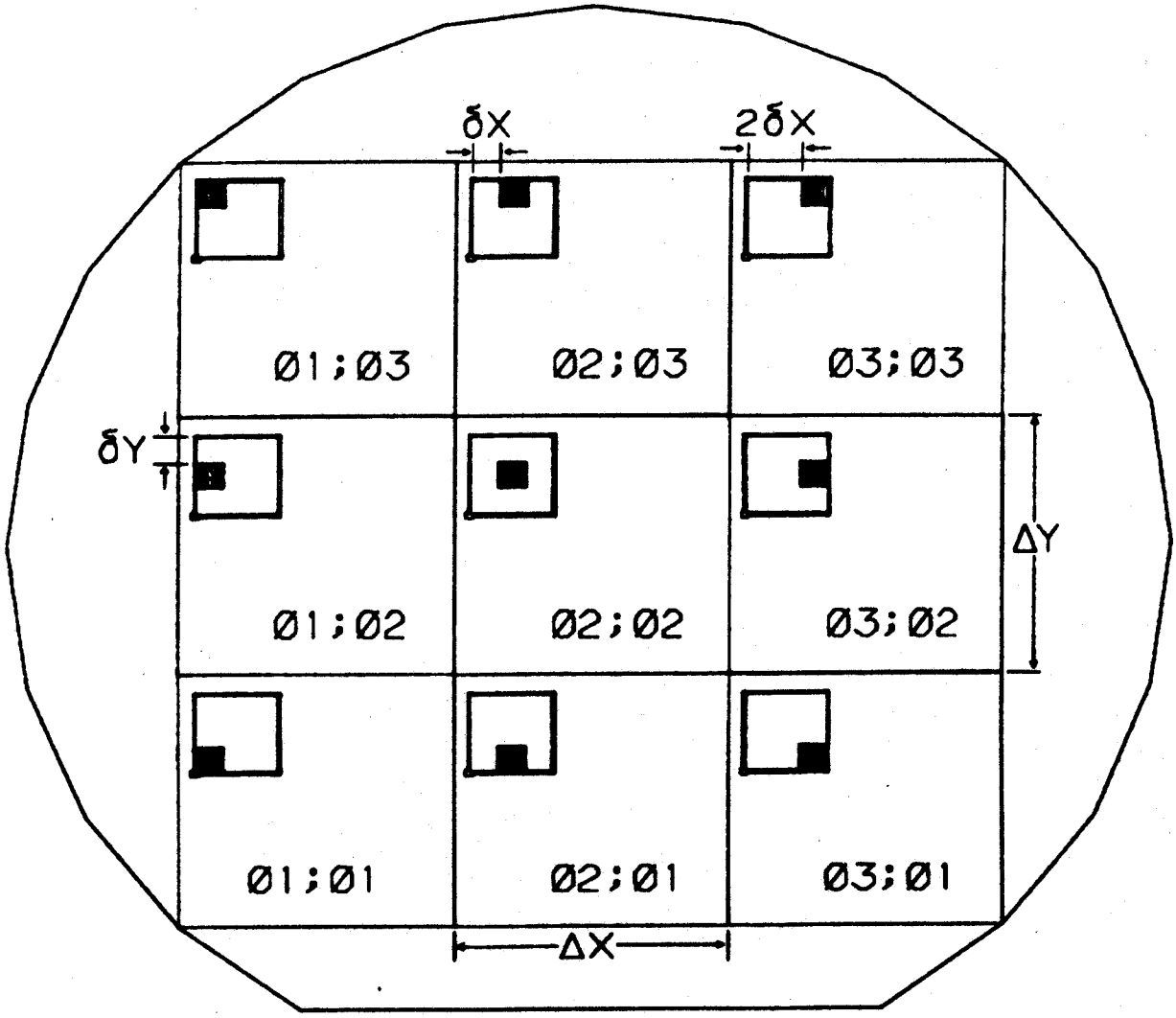

Fig. 1

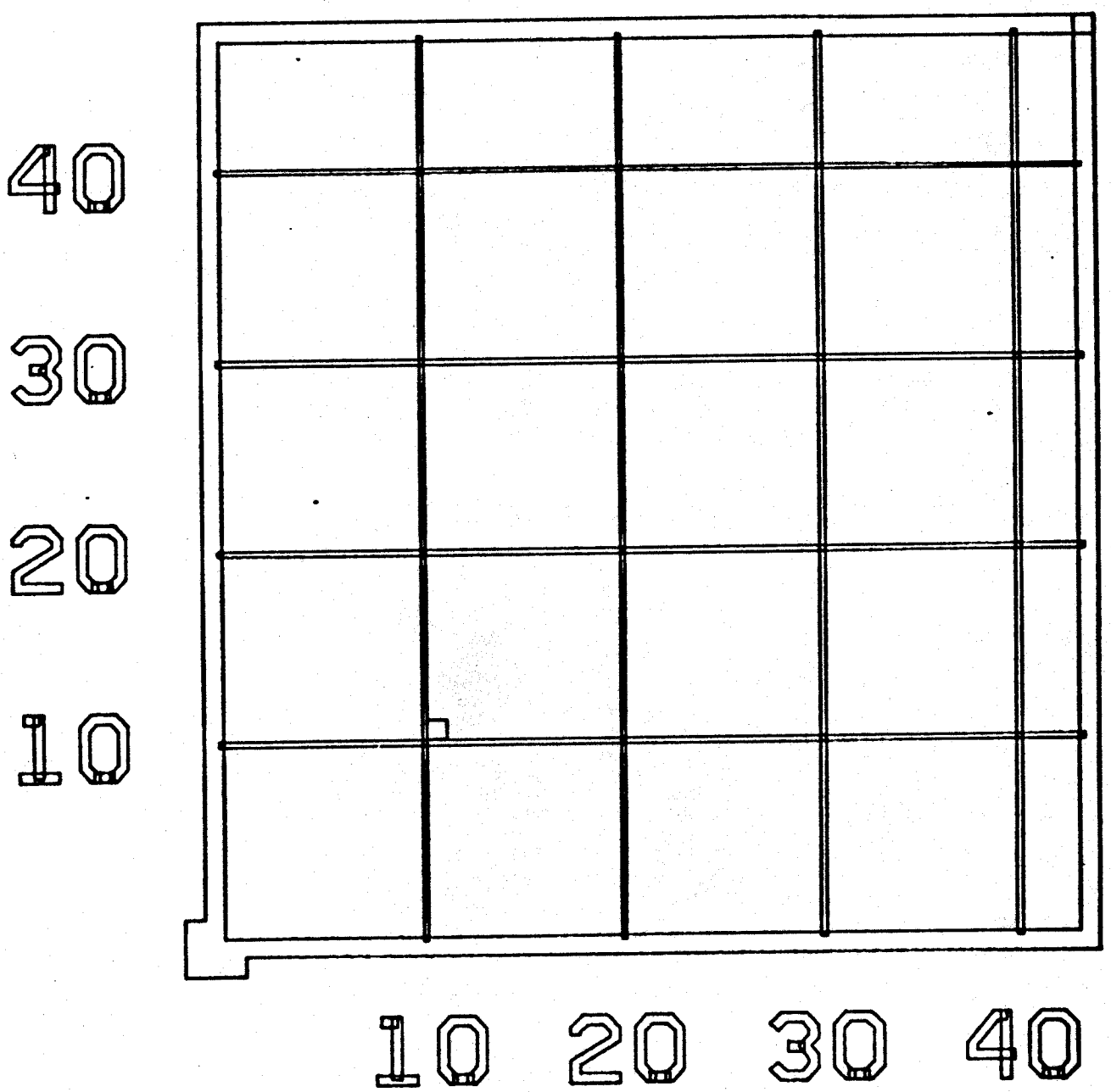

Fig. 2