Enhanced Channel Mobility in Polysilicon Thin Film Transistors

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***Abstract*—Due to scattering by charged grain boundaries, carrier mobility μ in the channel of polysilicon thin film transistors (TFT) is usually much lower than the bulk silicon value. We have studied a series of p-channel TFT devices with varying gate oxide thicknesses d_{ox} and found that μ shows a strong increase when d_{ox} is reduced below 150 Å. We attribute this effect to the screening of the charged grain boundary by the gate conductor. The screening becomes effective when the characteristic length associated with the potential barrier at charged grain boundaries becomes comparable to the optical distance between the grain boundary charge and its mirror image in the gate electrode. From the known structure parameters the onset of the strong screening is estimated to occur at oxide thicknesses of about 100 Å.**

I. Introduction

The presence of grain boundaries has a profound effect on the performance of polysilicon thin film transistor (TFT). In the *off* state of the device, grain boundaries generate an undesirable field-emission current. In the *on* state, potential barriers associated with charged grain boundaries impede carrier transport in the channel. Because of that the channel mobility μ in TFT's is usually much lower than that in bulk silicon [1], [2]. We have studied the channel mobility as a function of the gate oxide thickness d_{ox} in p-channel TFT and found that μ shows a strong increase when d_{ox} is reduced below 150 Å.

II. Device Structure

We investigated devices with an inverted structure, with the gate underneath the channel (see ref. 3). Polysilicon of the inverted gate was heavily doped with phosphorus. The gate oxide was formed by LPCVD deposition from TEOS. As deposited, the oxide was 250 Å thick; variations in d_{ox} were obtained by submerging groups of wafers in a 100 : 1 HF solution for different lengths of time. The actual thickness of the gate oxide was determined by ellipsometry. Device channel was formed by the CVD of a 400 Å amorphous silicon layer with a subsequent grain-size enhancing anneal [4], resulting in an average grain size of 2500 Å. Source and drain regions were formed by patterning and BF_2 implantation. For the mobility measurements, we chose devices with as-drawn gate length of 1.4 μm; we estimate the outdiffusion from the source and drain regions into the channel at the processing heat cycle (the highest temperature 800 °C) to be 0.1 μm, therefore, the actual channel length was 1.2 μm.

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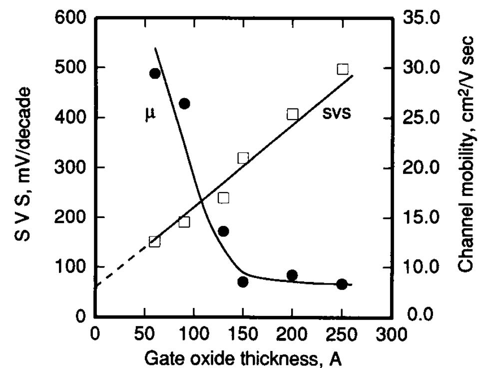

Fig. 1. Channel mobility and subthreshold voltage swing in polysilicon TFT plotted as a function of gate oxide thickness.

III. Results

The low-field channel transconductance g_m was measured as a function of the gate voltage at drain voltage of -0.1 V, and μ was determined by the standard procedure, at the gate voltage corresponding to the maximum transconductance. Fig. 1 presents the dependence of the channel mobility on the gate oxide thickness. For thick oxides, in the range d_{ox} = 150–250 Å, we find μ = 8–9 cm^2/V· sec. In this range, the mobility exhibits no dependence on d_{ox}. For thinner oxides, however, we see a striking enhancement of the mobility, as d_{ox} is reduced.

Also shown in Fig. 1 is the measured dependence of the subthreshold voltage swing (SVS) on the gate oxide thickness. The behavior is similar to that in a single-crystal silicon device: the linear dependence SVS (d_{ox}) intercepts the ordinate at $\sim$ 60 mV/decade, which corresponds to an ideality factor of unity. However, the steep slope of the dependence is indicative of a high trap density at the interface.

As an illustration, Fig. 2 shows the linear drain current and the transconductance as a function of the gate voltage, for a device with d_{ox} = 130 Å. The threshold voltage of the device V_{th} is determined graphically as the intercept with the voltage axis. Also shown is the voltage V_m, corresponding to the maximum in the transconductance. The difference between V_m and V_{th}, divided by d_{ox}, yields the electric field $E(V_m)$ in the gate oxide at the point of maximum transconductance.

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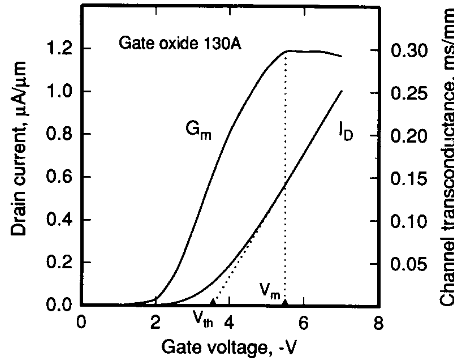

Fig. 2. Extraction of the threshold voltage and gate bias corresponding to maximum transconductance for $d_{ox} = 130$ Å.

TABLE I
THE PEAK TRANSCONDUCTANCE AND THRESHOLD VOLTAGES, AND CORRESPONDING OXIDE FIELDS FOR DIFFERENT THICKNESSES OF THE GATE OXIDE

d_{ox}, A	60	90	130	150	200	250
V_m, V	2.62	3.22	5.50	6.50	8.38	11.04
V_{th}, V	1.74	2.04	3.54	4.04	5.36	6.98
$E(V_m)$, MV/cm	1.47	1.33	1.51	1.67	1.50	1.60

The values of V_{th}, V_m, and $E\ (V_m)$ are gathered in Table I. One can see that in the entire range of d_{ox} studied, the transconductance peaks at the oxide field of ~ 1.5 MV/cm.

IV. DISCUSSION

Each grain boundary represents a meandering wall that cuts the channel in some random direction, cf. Fig. 3. The height of the wall is approximately the channel thickness, $h \approx 400$Å. In the *on* state of the device, the trap states on the grain boundary are charged. When the gate is far away (thick d_{ox}) the trapped charge is compensated by a depletion of the channel in a narrow region of thickness L along the wall.

The potential barrier at the grain boundary arises due to the dipolar field between these oppositely charged meandering walls. The barrier has a pagoda shape and extends over a distance of order L. The characteristic length L can be estimated by equating the charge $h \cdot n_{\text{T}}$ at the grain boundary with the compensating charge $L \cdot n_{\text{S}}$ in the channel:

$$L \cdot n_{\text{S}} = h \cdot n_{\text{T}}, \quad (1)$$

where n_{T} is the density of states at the grain boundary ($n_{\text{T}} \approx 2 \cdot 10^{12}$ cm^{-2}) and n_{S} is the induced charge density in the channel (at electric field of 1.5 MV/cm $n_{\text{S}} \approx 3 \cdot 10^{12}$ cm^{-2}).

Carrier transport along the polysilicon channel is impeded by this potential barrier. However, for a sufficiently thin gate oxide, the motion of carriers is also influenced by the mirror image of the meandering-wall dipole in the heavily doped gate. When the gate conductor plane is near the channel, the dipole is screened and the potential barrier for the in-plane motion of carriers becomes lower. This effect is manifested by an increase in the channel mobility. The screening becomes stronger for thinner oxides.

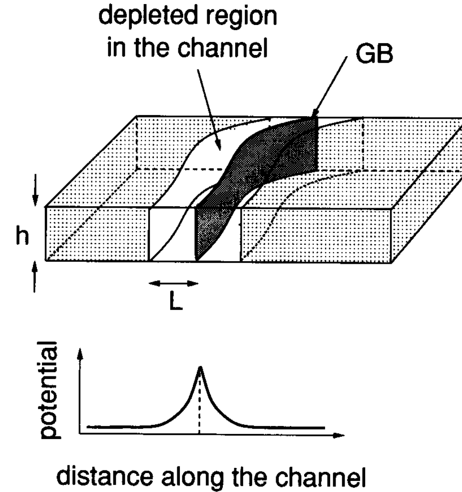

Fig. 3. Schematic illustration of the in-plane potential barrier formation in the *on* state of a thin film transistor. Top picture shows the 400 Å-thick channel in accumulation. The meandering grain boundary (shaded) extends into the page, with depletion regions on both sides.

Let us estimate the characteristic thickness d_{ox} of the gate dielectric, corresponding to the onset of a strong screening. Obviously, the gate screening becomes effective when d_{ox} (weighted by the permittivity ratio $\alpha = \epsilon_{Si}/\epsilon_{ox}$) becomes comparable to L, given by (1). The relation $\alpha d_{ox} \leq L$ gives an estimate of $d_{ox} \approx 130$ Å for the critical thickness, which is in accordance with our observations.

The high channel mobility and low SVS make thin oxides very attractive. However, thinning of the gate oxide leads to high electric fields in the vicinity of the drain in the *off* state and unacceptably high *off* state currents. Normally, this problem is dealt with by using device structures with a drain offset [5]. However, this solution would eliminate the advantage of a high μ, since most of the drain voltage drops in the offset region. An elegant solution would be to employ the recently proposed active gate TFT structure [6]. Its key element is a lightly doped part of the gate near the drain; only the gate region adjacent the source is heavily doped. In the *off* state, the lightly-doped region is depleted and acts like a drain offset. In the *on* state, the lightly-doped region is in accumulation and acts as a conventional heavily doped gate. The active gate structure allows practical implementations of the enhanced mobility effect in thin-oxide TFT's.

Another problem of a thin-oxide device is the gate leakage. At gate voltages corresponding to peak transconductance we observed a leakage in a range $\sim 10^{-10}$–10^{-11} A/μm, much higher than could be expected from the Fowler-Nordheim tunneling at 1.5 MV/cm. Gate leakage is likely due to imperfections in the CVD oxide. Thus, improving the oxide quality (e.g., using silane/nitrous oxide CVD) should improve the leakage characteristics. Moreover, since CVD deposited oxides form a low-quality SiO_2 interface anyway, we should consider replacing them with high-permittivity materials [7]. The onset of the mobility enhancement can then be expected at

dielectric thicknesses of order several hundred angstroms; for thicknesses less than 100 Å the channel mobility will approach that in a single-crystal transistor.

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