Multi-Terminal Light Emitting Logic Device Electrically Reprogrammable between OR and NAND Functions

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Abstract

A monolithic multi-terminal logic device that functions both optically and electrically as an "ORNAND" gate, is demonstrated for the first time. The device, based on the real-space transfer of hot electrons into a complementary collector layer, has been implemented in MBE-grown InGaAs/InAlAs heterostructure. Excellent performance is obtained at room temperature. The output current and optical power both exhibit **or** and **nand** functions of voltages of any two of the three input terminals, these functions being interchangeable by the voltage on the third terminal.

Introduction

An important direction in the microelectronics research is the development of new *functional devices*, which can perform logic tasks that would normally require an assembly of several transistors. The charge injection transistor (CHINT) [1]) offers interesting opportunities in this context. The concept of CHINT refers to a class of devices based on the real-space transfer (RST) of hot electrons between independently contacted layers. A number of functional devices employing this principle have been discussed in the literature [2-9].

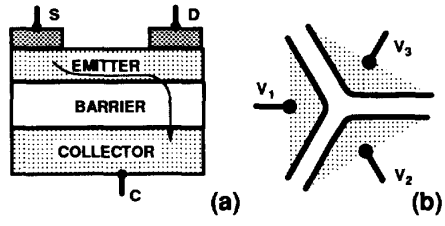
The generic CHINT structure is illustrated in Fig. 1a. One of the conducting layers, the emitter, plays the role of a hot-electron cathode. The other conducting layer, the collector, is separated by a heterostructure barrier. The RST effect manifests itself in the increase of the collector current I_C at a constant positive collector bias V_C, when a sufficiently high heating bias V_{DS} is applied. In the optoelectronic version [5,8,9] of CHINT the RST occurs into a *complementary* collector layer and results in a luminescence signal proportional to I_C.

A fundamental property of RST transistors is the *symmetry equivalence* [10] between the internal states $S[V_D, V_C]$ of the device at different applied biases:

$$S[V_D, V_C] \rightleftarrows S[-V_D, (V_C - V_D)] . \qquad (1)$$

This correspondence follows from the reflection symmetry of the device. Although a similar relation exists between internal states $S[V_D, V_G]$ in a FET, the difference is that the CHINT collector is the output terminal and the symmetry expressed by (1) implies that I_C is invariant under an interchange of the input voltages V_S and V_D. Thus the device exhibits an exclusive-OR dependence of the output current $I_C = \mathbf{xor}(V_S, V_D)$ on the input voltages, regarded as binary logic signals.

Powerful logic functionality is obtained in a RST device with three input terminals [4]. This device, which we shall refer to as the ORNAND gate, has a cyclic 3-fold symmetry, Fig. 1b. Its truth table (Fig. 1c) corresponds to $\mathbf{ornand}(\{V_j\}) = \mathbf{or}(V_1, V_2)$ when V_3 is low, and $\mathbf{ornand}(\{V_j\}) = \mathbf{nand}(V_1, V_2)$ when V_3 is high.



logic input	V_3	0				1			
	V_2	1	0	0	1	1	0	0	1
	V_1	0	0	1	1	0	0	1	1
output	I_C	1	0	1	1	1	1	1	0
function		or				nand			

(c)

Fig. 1: Charge injection transistor principle and the RST logic.
(a) Schematic diagram of a CHINT. Emitter electrons, heated by the field applied between electrodes *S* and and *D*, undergo RST into the collector layer, as indicated by the arrow.
(b) ORNAND logic gate. Input terminals arranged with a 3-fold cyclic symmetry define three channels 1-2, 2-3, and 3-1.
(c) Truth table of $I_C(V_1, V_2, V_3)$. The RST current is *off* in two states when $V_1 = V_2 = V_3$ and *on* in the other six states. By symmetry, every *on* state has the same I_C.

Electric **ornand** operation has been demonstrated [4] using an assembly of three discrete unipolar devices. Optoelectronic **xor** operation of a complementary CHINT has also been demonstrated [8,9]. The present work reports the first realization of a monolithic ORNAND gate. The use of a complementary collector structure enables both electrical and optical output signals.

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Epitaxial structure and device fabrication

The epitaxial structure shown in Fig. 2 is generally similar to those used in our previous studies [8,9] of the complementary CHINT, but there are several noteworthy differences. The present structure is grown on a p-type substrate and uses a more heavily doped collector contact layer to reduce the parasitic series resistance in the collector circuit. The emitter channel is also more heavily doped to avoid its complete depletion by the surface potential and ensure a "normally-on" channel, which conducts even in the absence of a positive V_C. Each channel has length $L_{CH} = 1\,\mu m$ and width $W = 40\,\mu m$. Instead of a triangular arrangement of the electrodes, the required cyclic symmetry is obtained with four electrodes $1, 2, 3, \tilde{3}$, the latter two being logically identical ($V_{\tilde{3}} \equiv V_3$) though physically split.

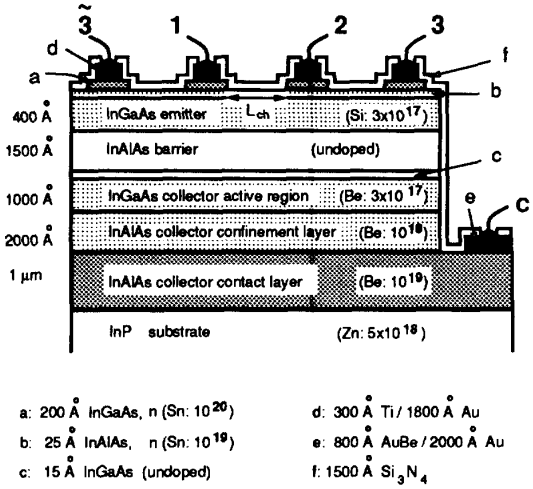


Fig. 2: Cross-section of the device structure. Three channels are defined by 1 μm trenches etched in the cap layer (*a*). Cyclic symmetry of an ORNAND gate results from the periodic boundary condition $V_{\tilde{3}} \equiv V_3$.

Properties of a Single Channel

The multi-terminal logic device actually forms three channels: $1-2$, $2-3$, and $\tilde{3}-1$. Fig. 3 shows the typical room-temperature characteristics, measured in the channel $\tilde{3} \rightarrow 1$. Here and below, the direction source $\rightarrow$ drain in a particular measurement is indicated by an arrow. Characteristics of different channels coincide quite closely, but there is a slight asymmetry under the source-drain interchange in a single channel, due to an unavoidable off-center misalignment of the channel position. Thus the $\tilde{3} \rightarrow 1$ characteristics are slightly different from those measured in the $1 \rightarrow \tilde{3}$ configuration.

The characteristics in Fig. 3 are taken at a constant positive collector bias $V_C = 2.3\,V$. As the heating voltage V_D increases, the channel current I_D first increases like in a FET. When V_D is high enough to establish a significant RST injection I_C^{RST}, the drain current shows a negative differential resistance. Prior to the onset of RST, I_C is seen to decrease due to the reduction of the collector leakage current I_C^{LKG} in the drain area with diminishing collector-to-drain bias.

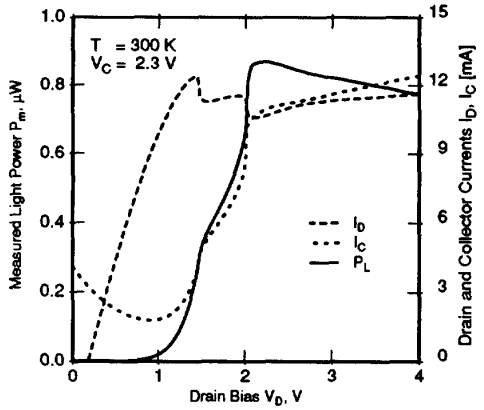


Fig. 3: Room temperature current-voltage and light-voltage characteristics of a single-channel $\tilde{3} \rightarrow 1$ at a fixed collector bias $V_C = 2.3\,V$. Electrode $\tilde{3}$ is grounded and 1 acts as the drain. Electrodes 2 and 3 are floating.

In addition to currents I_D and I_C, Fig. 3 plots the luminescence power P_L, measured with a broad-area Ge photodiode and suitable focusing optics. The emitted light spectrum is narrow and peaks at 1.6 μm. Note that prior to the onset of RST, there is virtually no light output, even though the collector current is non-negligible. As discussed in detail in Ref. [9], this results from I_C^{LKG} being almost entirely due to thermionic emission of holes from the collector active layer (in the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterojunction the valence band discontinuity $\Delta E_V \approx 0.2\,eV$ is substantially lower than the conduction band discontinuity $\Delta E_C \approx 0.5\,eV$). Holes injected into the channel have a vastly lower radiative efficiency, because they are likely to reach a heavily doped contact before they recombine radiatively with electrons. In contrast, electrons injected into the collector are confined in the active region. Virtually all of the optical output can be attributed to recombination of injected electrons in the collector active layer. The estimated internal radiative efficiency at 300 K is approximately 5 % for I_C^{RST} and only about 0.03 % for I_C^{LKG}. At $T = 6\,K$, the radiative efficiency in the collector active layer increases to 30 %.

Single-channel characteristics of present devices are significantly improved over those reported earlier [9]. The key improvement lies in larger values of I_C^{RST}, which are moreover achieved at lower V_C. This can be attributed to a reduction of parasitic resistances. The present device, because of its multiterminal nature, naturally lends itself to a measurement of the series resistance R in electrodes 1 and 2. We have found $R = (10 \pm 1)\,\Omega$, dominated by the contact resistance.

Logic

Since we set the periodic boundary conditions $V_{\tilde{3}} = V_3$, our multi-terminal device has effectively three input terminals. One of these can be viewed as a control electrode which determines which of the two logic functions **or** or **nand** is executed on the other two inputs. Choice of the control electrode is arbitrary. The collector current I_C and the light power P_L represent the logic output. We shall refer to the states with *high* and *low* values of the output as *on* and *off* states, respectively.

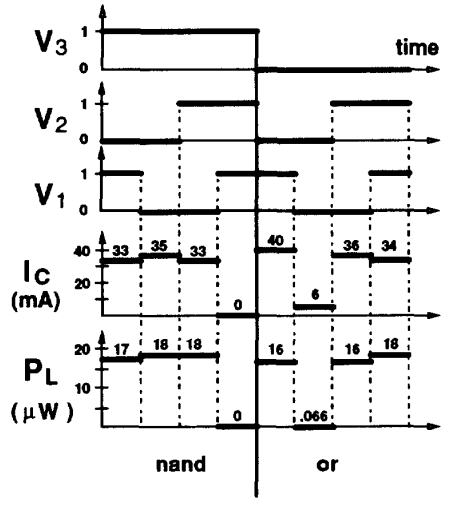
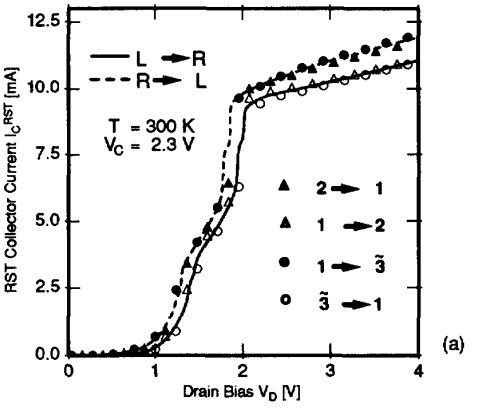


Fig. 4: Optical and electrical logic operation of the ORNAND gate, obtained in a quasi-stationary measurement at room temperature and $V_C = 2.4\,V$. Electrodes 3 and $\tilde{3}$ are tied together. The binary values "logic-0" and "logic-1" of the input signals V_1, V_2, and V_3 correspond to 0 and 3 V, respectively.

Fig. 4 demonstrates the room-temperature logic operation of our multi-terminal device. The light signal has been detected from the back of the polished substrate using a microscope objective to collect the light. The substrate thickness has been polished down to 35 μm reducing the free carrier absorption in the substrate. The collector bias is fixed at $V_C = 2.4\,V$ and the input signals V_1 and V_2 are varied between *low* = 0 and *high* = 3 V, while the split electrode, chosen as the control, is fixed either at the *low* value $V_3 = 0$ for the **or** function or at the *high* value $V_3 = 3\,V$ for the **nand** function.

As seen from Fig. 4, the symmetry between different *on* states is well maintained, both for I_C (±8%) and P_L (±6%). The larger variation in I_C is due to the variation in the leakage current of holes. Different *on* states correspond to different areas A_S of the source contact: A_S is 25% of the total emitter area for **nand**(0,1) and **nand**(1,0), while $A_S = 75\%$ for **or**(0,1) and **or**(1,0), and $A_S = 50\%$ for **nand**(0,0) and **or**(1,1). The larger the source area the larger is the leakage current which is added to the RST current. Since the radiative efficiency of I_C^{LKG} is negligible [8,9] compared to that of I_C^{RST}, the *on* states are more homogeneous in the measured light output. The low radiative efficiency of I_C^{LKG} also explains the fact that the *off* state of the **or** function is less than perfect electrically (the ratio $on/off \approx 7$ in I_C), while more than satisfactory optically ($on/off \gtrsim 200$ in P_L). In the *off* state there is no RST and most of leakage results from holes injected in the emitter layer.



input V_1, V_2	0,1	0,0	1,0	1,1
or $V_3 = 0$	1 → 2 3 → 2		3̃ → 1 2 → 1	3̃ → 1 3 → 2
nand $V_3 = 1$	1 → 3̃ 1 → 2	1 → 3̃ 2 → 3	2 → 1 2 → 3	

(b)

Fig. 5: Off-center channel asymmetry in the ORNAND gate.
(a) Comparison of the RST for two opposite orientations of the channel field in two different channels. Leakage current I_C^{LKG} is subtracted [9].
(b) Table of the channels under the heating field in all logic states of the gate. Position of the arrow describes the trench misalignment. Thus, the symbol $L \rightarrow R$ indicates that the trench is closer to the right (R) electrode.

Variation in the effective source area is not the only cause for a violation of the basic symmetry (1). Another way to break this symmetry is to displace the channel-defining trench in the n^+ cap layer from its nominal position in the middle between neighboring electrodes. Figure 5a shows the single-channel $I_C^{RST}(V_D)$ characteristics for two different channels and two different source$\rightarrow$drain orientations. We see that curves corresponding to the same orientation in two different channels coincide more closely than those for the same channel but different orientations. This observation holds true for all devices examined. We remark that the data in the present report have been collected from a wafer with an exceptionally lucky alignment of the trench and the source/drain masks. In other wafers, the difference between the RST in opposite orientations of the same channel is still larger. Nevertheless, this has no effect on the symmetry of *on* states in the ORNAND gate. Indeed, the symmetry break due to a trench misalignment has to be identical in all the three channels, cf. Fig. 2. Since each of the six *on* states has two channels under field – one of each orientation – this systematic asymmetry cancels out in the ORNAND logic operation, cf. the Table in Fig. 5b.

Conclusion

A multiterminal logic device, that functions both optically and electrically as an ORNAND gate, has been demonstrated for the first time. The device, based on the real-space transfer of hot electrons into a complementary collector layer, is implemented in a InGaAs/InAlAs heterostructure. The collector current and the optical output power both exhibit the **or** and the **nand** functions of any two of the three input terminals. These functions are not fixed by the layout but are interchangeable by the voltage on the third ("control") terminal. The logic nature of the gate is thus electrically reprogrammable in the course of a circuit operation. Choice of the control electrode is, moreover, arbitrary. This is the first implementation of a single logic device with such powerful capabilities.

The demonstrated device is an incoherent light-emitting source, similar to an ordinary LED. In order to increase its output power and improve the frequency performance, we must take advantage of the stimulated emission in a resonant optical cavity. The high injection current density, $J_C \gtrsim 25\,\mathrm{kA/cm^2}$, obtained in the present device and its high internal radiative efficiency, comparable to that in conventional LED's, are promising for the future implementation of a real-space transfer logic laser.

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