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Symmetry of the real-space transfer and collector-controlled states in charge injection transistors

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Abstract. The charge injection transistor, or CHINT, is a three-terminal semiconductor device based on controlled real-space transfer of hot electrons *between two conducting layers separated by a potential barrier*. The symmetry of hot-electron injection by real-space transfer with respect to the polarity of the heating field allows the implementation of novel circuit elements. Thus, in the basic CHINT structure, the collector current is an exclusive OR function of voltages applied to the emitter electrodes. Moreover, we have proposed and demonstrated a multiterminal device structure with three symmetric logic inputs that performs both the NOR and the AND logic functions, and can be switched between these functions in the course of the circuit operation. Symmetry properties of real-space transfer transistors have been studied theoretically, with the help of continuation modeling and transient device simulation. These studies reveal a variety of instabilities and a striking novelty of *multiply connected* current–voltage characteristics. We have found that the CHINT can support anomalous steady states in which hot-electron injection occurs in the absence of any voltage between the emitter electrodes. In these states, some of which are not only stationary but also *stable* with respect to small perturbations, the electron heating is due to the fringing field from the collector electrode. Some of the anomalous states break the reflection symmetry in the plane normal to the channel at midpoint. The study elucidates the formation of hot-electron domains.

1. Introductory review

The concept of real-space transfer [1] (RST) describes the process in which electrons in a narrow semiconductor layer, accelerated by an electric field parallel to the layer, acquire high average energy (become 'hot') and then spill over an energy barrier into the adjacent layer. This principle underlies the operation of a three-terminal hot-electron heterojunction device, called the charge injection transistor or CHINT [2, 3]. Figure 1 shows the structure of this device, implemented in the InGaAs/InAlAs heterosystem, lattice-matched to InP. The emitter layer (d) has two contacts, S and D, and plays the role of a hot-electron cathode. The collector layer (a) is separated from the emitter by a potential barrier (c). Transistor action consists of the control of the injection current I_C by the voltage V_D, applied between S and D.

Charge injection by RST is an efficient process. Even though only a small fraction of electrons in the high-energy tails of the hot-carrier distribution function participate, those tails are replenished at a fast rate corresponding to the energy relaxation time, mainly owing to electron–electron collisions. Multiple collisions result in a Gaussian distribution of carrier velocities, which can be interpreted as a Maxwellian ensemble with an effective electron temperature T_e. The injection process can then be considered analogous to the usual thermionic emission.

Advantages of the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterosystem for RST transistors stem from the low effective mass of electrons in the Γ valley of InGaAs, the high conduction-band discontinuity ($\Delta E_C \approx 0.5\,eV$), and the still higher satellite-valley separation ($\Delta E_{\Gamma L} \approx 0.55\,eV$). In this system, the RST has a lower threshold than the Gunn effect. The relatively large ΔE_C leads to an improved performance at room temperature. The lower effective mass favours the efficiency of electron heating in an electric field.

The transistor structure shown in figure 1, and its variations, have been employed in a series of experimental studies [4–8]. Figure 2 illustrates the basic device characteristics at both room and cryogenic temperatures. Typically, the onset of charge injection leads to highly nonlinear effects, including a strong negative differential resistance (NDR) in the $I_D(V_D)$ dependence. Sharp steps, seen in figure 2, are indicative of an internal switching and the formation of high-field domains. These instabilities arise due to a positive feedback between the RST and the heating electric field in the emitter channel [4]. Significant progress in the understanding of these pro-

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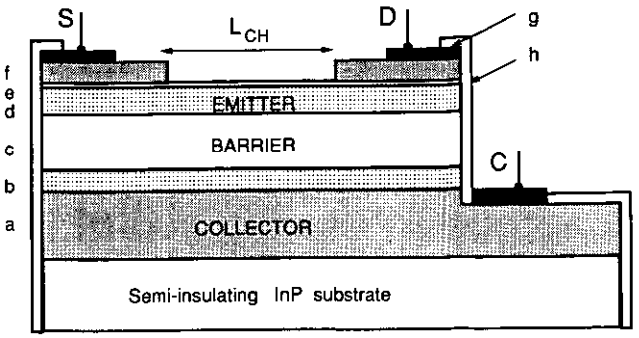

a: 5000 Å InGaAs n^+ (Si:10^{19})
b: 500 Å InGaAs n^- (Si:10^{17})
c: 2000 Å InAlAs u
d 500 Å InGaAs n (Si:10^{16})
e: 25 Å InAlAs n^+ (Si:10^{19})
f: 200 Å InGaAs n^+ (Sn:10^{20})
g: 500 Å Ti / 1000 Å Au
h: Si_3N_4

Figure 1. Cross section of a charge injection transistor implemented in the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As/InP$ heterostructure [6]. The epitaxially-grown heavily-doped capping layer, f, forming the S and D contacts, is patterned lithographically with the help of the etch-stop layer e.

cesses has been achieved recently, with the help of continuation modelling and transient device simulation, discussed in section 3.

The charge injection transistor is attractive for high-speed electronics since its ultimate performance is believed to be limited only by the time of flight of hot electrons over high-field regions of the device. These include the barrier layer and the domain in the emitter channel (the size of the domain is determined by electrostatic forces and hence also roughly corresponds to the barrier layer thickness). Another delay, associated with the time required for the electron scattering to establish an effective temperature in the emitter channel, is expected to be shorter than 1 ps. For the device in figure 1, the transit time can be estimated to be of the order of 3 ps, which sets the unity-gain cut-off frequencies at around 50 GHz. The cut-off frequencies, extrapolated from the microwave measurements of scattering parameters in this structure [7], were 40 GHz for both the current and the power gain. The ultimate speed performance can be achieved with an inverted CHINT structure in which the collector is the top layer [9]. This allows the reduction of the parasitic drain–collector capacitance and therefore the use of narrower barriers. With sufficiently narrow barriers, the CHINT can be expected to outperform a field-effect transistor of similar geometry (the RST collector corresponding to the FET gate, etc) because the speed of CHINT is not limited by the time of flight between the source and the drain.

A number of functional applications have been contemplated [10] based on the unique characteristics of three-terminal RST devices. Recently, the scope of such applications was expanded by the invention [5] of a new multiterminal device structure, called the NORAND. Its principle embodies the basic symmetry inherent in the charge injection by RST: the direction of the collector current is the same irrespective of the polarity of the heating voltage. The NORAND has three symmetric logic inputs and performs both the NOR and the AND logic functions – interchangeably in the course of the circuit operation. This operation has been demonstrated experimentally [5] and will be discussed in the next section.

The invention of NORAND has focused our attention on the symmetry properties of RST transistors. It is clear that the device illustrated in figure 1 has an approximate symmetry with respect to reflections in the mid-plane normal both to the layers and to the plane of view (the symmetry would be exact if not for the one-sided placement of the collector electrode). This symmetry implies a correspondence between the states of the device at the external biases $[V_D, V_C]$ and $[-V_D, (V_C - V_D)]$. In particular, states at $V_D = 0$ must either be symmetric or form symmetry-related doublets. As will be discussed in section 3, there is indeed a variety of such states, some of

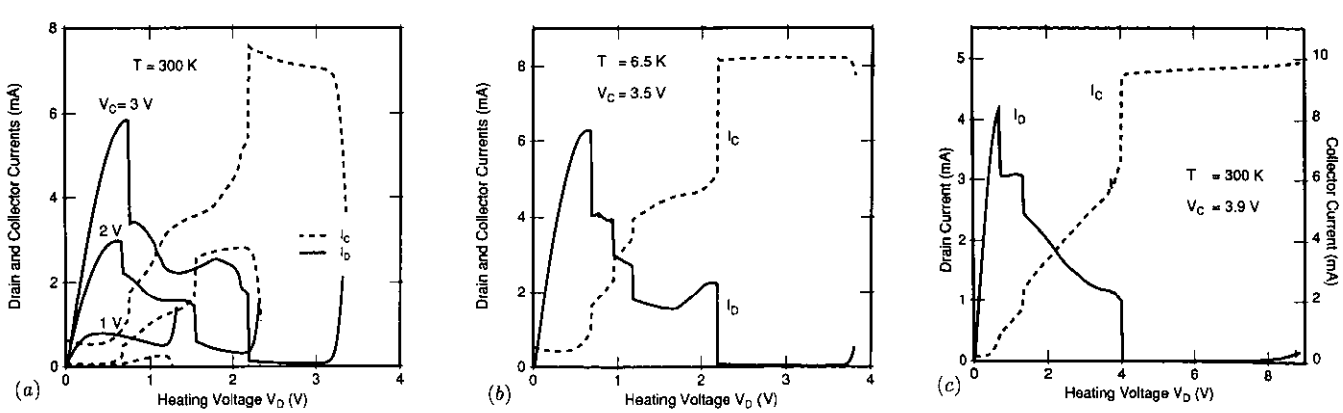

Figure 2. Current–voltage characteristics of InGaAs/InAlAs charge injection transistors [4–6]. The drain current (I_D) and collector current (I_C) are plotted against the heating drain voltage V_D at fixed values of the collector bias. (*a*), (*b*) Characteristics of a CHINT device with the emitter channel length $L_{CH} = 1\ \mu m$ and emitter width $W = 50\ \mu m$. The device structure [4] is similar to that in figure 1, except for the absence of the etch-stop layer, e, and the subcollector layer, b, introduced later [6]. (*c*) Room temperature characteristics of a device with $W = 25\ \mu m$ and $L_{CH} = 1\ \mu m$. The device structure [6] corresponds to figure 1.

which are not only stationary but also *stable* with respect to small perturbations. In these states, the electron heating is due to the fringing field from the collector electrode. Our study shows that the formation of hot-electron domains at $V_D > 0$, represents a transition to a collector-controlled state that is continuously related to one of the anomalous states at $V_D = 0$.

2. Charge injection logic

The fact that the RST current I_C does not depend on which of the two surface terminals, S or D, is chosen to be the source, allows the implementation of devices in which the role of a particular terminal in the circuit is not defined by the layout. Consider the circuit illustrated in the top portion of figure 3, not as a transistor but as a logic element with inputs S and D corresponding to the biases on the S and D electrodes, respectively. The point to note is that the logic function OUT(S, D) represents an exclusive NOR, since OUT is high when I_C is low (no RST) and OUT is low when the injection current is flowing. The latter situation results only when the voltages of S and D are sufficiently different.

The bottom part of figure 3 is a schematic diagram of the proposed logic element NORAND which has three logic inputs X_j ($j = 1, 2, 3$) and one output OUT. Which of the X_j will serve as a source and which as a drain is determined only at the time when a particular logic operation is performed. The value of OUT is high

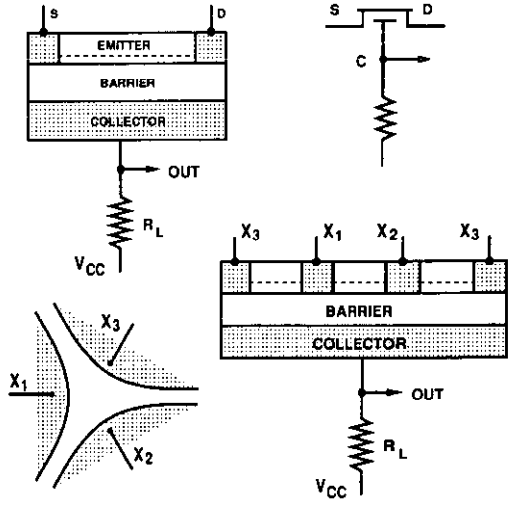

Figure 3. Schematic illustration of the charge injection logic [5]. Top figure on the right introduces a circuit symbol of the CHINT. The bottom figures illustrate the NORAND element. The figure on the bottom left describes a symmetric arrangement of three identical channels, X_{3-1}, X_{1-2}, and X_{23}. By symmetry, one has the same amount of hot-electron injection for any of the six states of binary input in which at least one of the three X_j is different from the other two. The bottom right-hand figure describes an asymmetric NORAND layout. One of the electrodes is physically (but not logically) split, resulting in a 'periodic' boundary condition, equivalent to the three-fold rotational symmetry of the figure on the left.

(logic 1) only when all three X_js have the same value (high or low). All the other six possible logic input configurations lead to the same high injection current resulting from hot-electron emitters formed in two of the three channels, X_{3-1}, X_{1-2}, and X_{2-3}. Three of these configurations correspond to the presence of two sources and one drain, the other three to one source and two drains.

It is easy to see that the logic function OUT ($\{X_j\}$) is given by

$$\text{OUT}(\{X_j\}) = (X_1 \cap X_2 \cap X_3) \cup (\bar{X}_1 \cap \bar{X}_2 \cap \bar{X}_3) \quad (1)$$

where the symbols $\cap$, $\cup$, and $\bar{\text{A}}$ stand for logic functions AND, OR, and NOT A, respectively. We see that the NORAND operates as a $\text{NOR}(X_1, X_2) = \overline{X_1 \cup X_2}$ when the input to X_3 is *low*, X_3 = logic **0**, and as an $\text{AND}(X_1, X_2) = X_1 \cap X_2$ when X_3 = logic **1**. It is clear that the three-fold symmetry of the device ensures that the injection current has the same value in all the six states corresponding to OUT = logic **0**. Of course, one can achieve a similar effect without an exact three-fold symmetry, e.g. with a 'cylindrically' symmetric arrangement of the $\{X_j\}$ electrodes, as illustrated in the bottom right-hand part of figure 3.

The NORAND functional element departs radically from all previously contemplated uses [10] for multi-terminal RST devices. Compared with all existing logic families, it offers a considerable economy in the layout of basic functional elements. Moreover, it promises faster operation of these elements, since the entire function is implemented within one gate delay of a high-speed transistor. The operation of NORAND has been demonstrated [5] with a circuit consisting of three discrete CHINT devices with similar characteristics. This circuit is functionally equivalent to a monolithic structure with three input terminals.

In order that a logic device could be used in integrated circuits, it is necessary that its input and output voltages be consistent. In the case of NORAND this requires additional level-shifting circuitry. In principle, this would not be a necessary requirement if only the NOR part of the NORAND truth table were to be employed. In the NOR configuration, the device has a well-defined ground level, and a consistent range of input–output characteristics can be found, as has been ascertained experimentally. On the other hand, in the AND configuration the low-OUT voltage must be higher than the lowest of the input voltages. In an optimized device, this difference can be made small, but since it would still accumulate after several stages, the level shifting will be mandatory. Of course, it is well known that all logic functions can be implemented on the basis of a NOR element alone.

In all charge-injection transistors demonstrated so far, the injection occurs between layers of the same conductivity type, because RST of minority carriers would be of no apparent advantage for transistor applications. However, it can be used for generating light by recombination [11]. Light-emitting devices based on the RST of minority carriers will have a logic functionality in the

light output with respect to two or more electrical inputs. In particular, it is possible to implement an optoelectronic analogue of the NORAND element, its optical output, **L**, being complementary to the logic value of NORAND's OUT signal. This element, which may be termed ORNAND, gives $\mathbf{L} = \text{OR}\ (X_1, X_2)$ when the input to X_3 is low, and $\mathbf{L} = \text{NAND}\ (X_1, X_2)$ when X_3 is high. In our opinion, such an element will find important optoelectronic applications.

3. Collector-controlled states and hot-electron domains

Symmetry properties of real-space transfer transistors have been studied theoretically, with the help of continuation modelling and transient device simulation. Details of the program and computational methods are described elsewhere [12–13]. The analysis is based on the solution of a set of coupled partial differential equations, including Poisson's equation and expressions [14] for the current continuity and the energy balance, in a two-dimensional sample, subject to the boundary conditions on voltage and/or current at the three electrodes. Models for the local hot-electron mobility, $\mu(T_e)$, and the energy relaxation time, $\tau_E(T_e)$, are chosen so that in a uniform electric field, F, one obtains a given velocity-field, $v(F)$, and temperature-field, $T_e(F)$, characteristics. The current density is assumed to consist of drift ($en\mu\nabla V$) and thermodiffusion ($\mu\nabla[nkT_e]$) components, where n is the electron concentration and V the electrostatic potential.

The results presented correspond to a specific choice of an InGaAs/InAlAs heterostructure, as in figure 1. In particular, the barrier height separating the emitter and collector layers is taken equal to 0.5 eV. In order to disentangle our results from negative differential mobility effects arising from the momentum-space transfer, we have chosen the $v(F)$ dependence in a simple form [15], $v = \mu_0 F[1 + (\mu_0 F/v_{sat})^2]^{-1/2}$, parameterized by the low-field mobility, μ_0, and the saturation velocity, v_{sat}. We have checked that our results remain qualitatively similar for a more realistic $v(F)$ model, appropriate for InGaAs. To simplify the discussion further, we have excluded the phenomena of impact ionization and tunnelling.

In the examples below, we assumed the lattice temperature $T = 300$ K, a constant (T_e-independent) diffusivity [16], $D = \mu_0 kT/e$, and a $\mu_0(N_D)$ that is a function of the local ionized impurity concentration (in the low-doped regions, $\mu_0 \approx 10^4\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$). We have performed a number of simulations, varying the geometry (channel length L_{CH} and barrier thickness d_B), the transport parameter v_{sat}, and the external bias conditions.

Figure 4 shows an example of the CHINT characteristics, $I_D(V_D)$, at a fixed collector voltage, $V_C = 2$V, relative to the S electrode. Because of their multivalued nature, such dependences are difficult to obtain by a straightforward solution of stationary transport equations. To circumvent this difficulty, we used the continuation method [12] which traces a connected

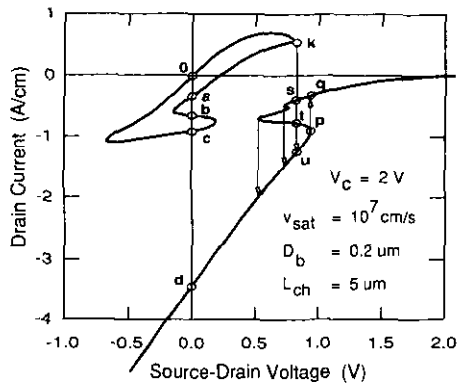

Figure 4. Current–voltage characteristics obtained by the continuation method. Arrows indicate the transitions studied by transient simulations.

component of the characteristic, starting from any established state within the component. The curves in figure 4 correspond to the locus of points [17] in the (V_D, I_D) plane for which the device has a steady state at a given V_C. To our knowledge, the displayed $I_D(V_D)$ dependence represents the first example of a multiply connected two-terminal current–voltage characteristic. The known NDR devices may exhibit multivalued functions in the $I(V)$ dependence (e.g. the pnpn diode), in the $V(I)$ dependence (the Esaki tunnel diode, the Gunn diode), or even in both (the thyristor [12], the resonant tunnel diode in the intrinsic-bistability range [18])—but these can always be traced as a continuous curve in the (V, I) plane.

Points, separated by a finite distance on a (V, I) plane, correspond to macroscopically distinct states of the device. Any transition between disconnected components of the graph requires a global redistribution of the state fields, corresponding to the formation or repositioning of high-field, high-temperature domains in the structure. Such a redistribution, reminiscent of a phase transition, is forced as V_D increases beyond the rightmost point, (**k**), of the bounded graph component. The potential profiles, $V(x)$, along the channel—before and after the transition—are shown in figure 5(*a*). Of the three collector-controlled states, **s**, **t**, and **u**, corresponding to the same ($V_D \approx 0.82$ V) external bias as the state **k**, two (**s** and **u**) are stable. The actual transition occurs into the state **u** which has the highest value of the collector current. This has been ascertained by a time-dependent simulation in which the initial state **k** was perturbed by a small step $V_D(\mathbf{k}) \rightarrow V_D(\mathbf{k}) + \delta V_D$. The hot-electron domains in the state **u** are characterized by a strong field concentration, accompanied by a dramatic rise in T_e. The electron concentration in the domains is depleted so that the collector field remains unscreened and the local potential goes below that of the drain [19], resulting in a negative I_D.

Increasing V_D beyond $V_D(\mathbf{u})$ results in a smooth evolution of the field distribution inside the device – until another instability is encountered at $V_D \approx 0.94$ V and the device switches between states **p** and **q**. The potential profiles in these two states are shown in figure 5(*b*). On

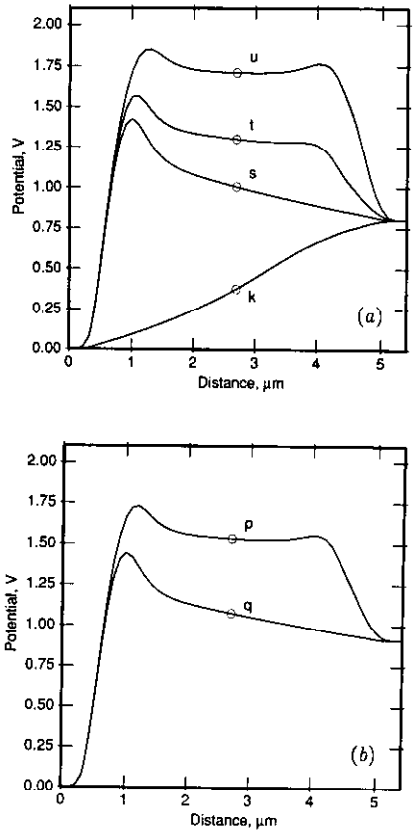

Figure 5. The channel potential profile, $V(x)$, in different CHINT states at the same external bias ($V_C = 2$ V, V_D). States are labelled as in figure 4. (*a*) $V_D = 0.8246$ V, states **k**, **s**, **t**, and **u**; (*b*) $V_D = 0.9378$ V, states **q** and **p**.

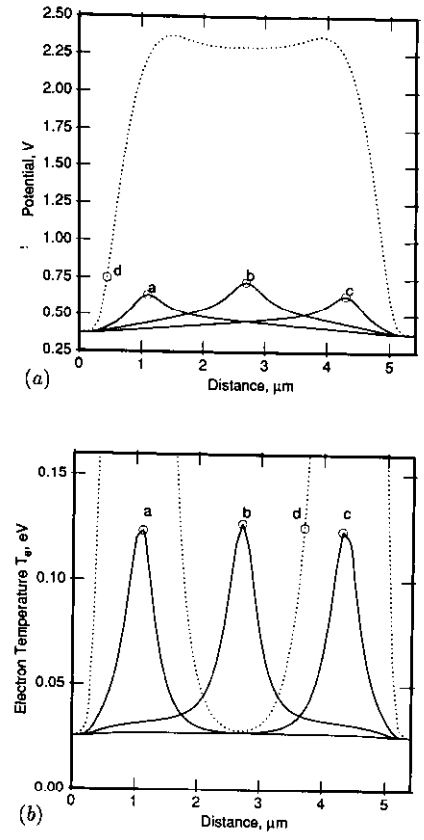

Figure 6. (*a*) the channel potential and (*b*) the electron temperature in the four anomalous states at $V_D = 0$. Solid lines correspond to states on the bounded component of the graph in figure 4, dotted lines to the unbounded component.

the way back (decreasing V_D), the device remains stable at **s**, but at $V_D \approx 0.73$ V (the small knee in figure 4) it suffers another instability and goes over into a high-current state similar to **u**. The large knee at $V_D \approx 0.52$ V is in an unstable region and cannot be reached. On the other hand, all states on the high-current branch **p**–**u**–**d** of the collector-controlled component are perfectly stable and experimentally accessible by a quasi-static variation of V_D. Of particular interest is the state **d**, corresponding to $V_D = 0$.

At $V_D = 0$, the equations governing the device behaviour have a perfect symmetry with respect to reflections in the plane normal to the channel at mid-point. Analysis of the CHINT states in the symmetric configuration indicates that the domain formation is a symmetry-breaking phenomenon. In addition to the normal [20] state **o** at $V_D = 0$, figure 4 reveals four anomalous states (**a**, **b**, **c**, and **d**). From the profiles of $V(x)$ and $T_e(x)$ along the channel, shown in figure 6, the nature of the anomalous state is clear: the heating is due to the lateral component of the fringing field from the C electrode. Accelerated by this field, electrons undergo RST and do not accumulate in the central portion of the channel. Hot-electron domains are formed when the finite supply rate of electrons to a 'hot spot' is exceeded by the RST flux from that spot. The supply is limited by the electronic transport with a saturated velocity along the channel. Hot-electron domains suppress the screening of the electric field from C by the channel electrons, and the RST becomes collector controlled. States of a multiterminal RST device under general bias are 'adiabatically' connected to the anomalous states of the symmetric configuration at $V_D = 0$.

Because of the nonlinear nature of the problem, the actual stationary states at $V_D = 0$ may not transform according to irreducible representations of the symmetry group. Thus, states **a** and **c** under reflection transform into each other, even though the reflection group has only one-dimensional linear representations. On the other hand, states **o**, **b**, and **d** are symmetric. A conjecture can be made that in general, at $V_D = 0$, we can expect an odd number m_S of symmetric states and an even number m_A of asymmetric ones. Varying V_C, we have been able to realize cases with $(m_S, m_A) = (1, 0), (3, 0), (3, 2), (3, 4)$, and $(5, 4)$. The above conjecture is based on the plausible proposition that there should always be one and only one unbounded path in the (V_D, I_D) plane and the symmetry requirement that asymmetric states come in pairs [21].

Of the five states at $V_D = 0$ and $V_C = 2$V, only two (**o** and **d**) are stable with respect to small perturbations. This has been ascertained by following the evolution of states in the vicinity of the steady states at $V_D = 0$. In these simulations, figure 7, the initial states $\mathbf{a}_\pm$, $\mathbf{b}_\pm$, and $\mathbf{c}_\pm$ have been assumed to coincide with a state on the loop displaced from **a**, **b**, and **c**, respectively, by an infini-

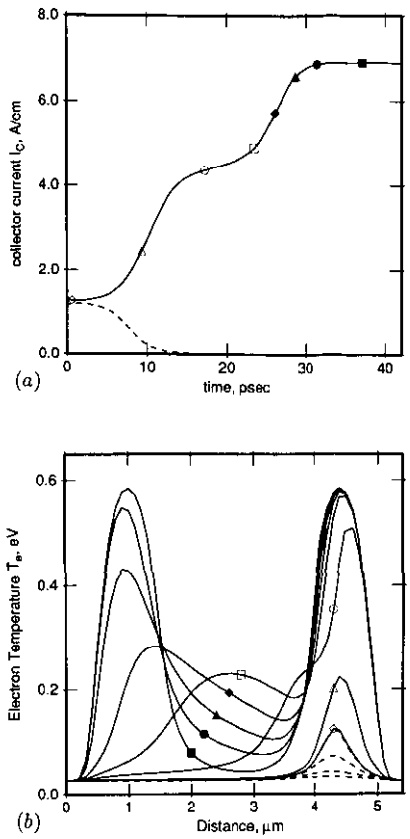

Figure 7. Evolution of the non-stationary states $\mathbf{c}_+$ (solid lines) and $\mathbf{c}_-$ (dashed lines) at $V_D = 0$. Time dependence of the injection current is shown in (*a*); symbols mark the selected times in the evolution, at which the electron temperature profiles are plotted in (*b*). The 'plateau' in the $I_C(t)$ dependence near $t = 20$ ps evidently corresponds to the situation when a fully developed hot-electron domain exists already near D but not yet near the S electrode.

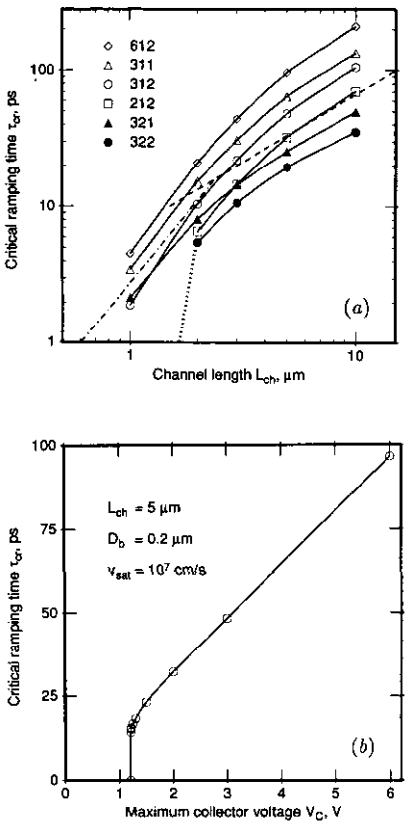

Figure 8. Critical ramping speed for the formation of a stable anomalous state at $V_D = 0$. The collector bias is ramped linearly $V_C = 0 \rightarrow V$ in the time interval τ. For $\tau > \tau_{cr}$ the device settles in the normal state, for $\tau < \tau_{cr}$ in the anomalous state **d**. (*a*) The values of τ_{cr}, determined to within 0.1 ps, are plotted against the separation, L_{CH}, between the emitter contacts. The key labels the curves with the number 'VSD' indicating the end-ramp voltage (V) in volts, the saturated velocity (*S*) in $10^7\,\mathrm{cm\,s^{-1}}$ and the barrier thickness (*D*) in 1000 Å. The dashed and stipple lines indicate linear and quadratic dependences, respectively. (*b*) The dependence of τ_{cr} on the end-ramp voltage for a 5 μm device. The value of V_C^{cr} for this device is 1.211 V.

tesimal voltage $\delta V_D = \pm 10$ mV. Even though these states are virtually indistinguishable from the corresponding stationary ones, we found that $\mathbf{a}_+, \mathbf{b}_-$, and $\mathbf{c}_-$ evolved into **o**, and $\mathbf{a}_-$, $\mathbf{b}_+$, and $\mathbf{c}_+$ into **d**. The instability of states **a** and **c** is associated with an NDR in the $I_C(V_C)$ dependence, $(\partial I_C/\partial V_C)_{a,c} < 0$, and that of **b** with both $(\partial I_C/\partial V_C)_b < 0$ and $(\partial I_D/\partial V_D)_b < 0$. All these instabilities develop on a rapid time scale, corresponding to electron travel over distances of the order of the domain size. They result in either the formation (repositioning) of a hot-electron domain, or its complete quenching due to the screening by channel electrons.

The fact that the state **d** is stable suggests that it can be arrived at by a shock excitation of an initially unbiased device. We have performed a number of time-dependent simulations, in which both S and D electrodes were kept grounded, while V_C was linearly ramped from 0 to a maximum value V. Depending on the ramping time, τ, the device settles in either the normal state ($\tau > \tau_{cr}$) or the anomalous state ($\tau < \tau_{cr}$) carrying a large RST current. The values of τ_{cr}, determined to within 0.1 ps, are plotted in figure 8(*a*) against the emitter channel length L_{CH} for different assumed values of v_{sat}, barrier thicknesses, and ramp-end voltages V. For short L_{CH} the dependence $\tau_{cr}(L_{CH})$ is approximately quadratic, and for long L_{CH} the dependence is linear. The anomalous state at $V_D = 0$ exists only for a sufficiently high V_C, and the value of V_C^{cr}, below which the state **d** disappears, depends on the device geometry and v_{sat}. The value of V_C^{cr} is sharply defined, and for the ramp-end voltage V above V_C^{cr}, one has $\tau_{cr} \propto V$ to a good approximation (cf figure 8(*b*)). This indicates that the relevant critical parameter is the displacement current ($\propto dV/dt$), which should be compared with a transient current ($\propto v_{sat}$) associated with electron screening processes in the emitter.

4. Conclusion

The most important potential applications of charge injection transistors are likely to be based on the peculiar symmetry of real-space transfer with respect to the heating field polarity. The same symmetry shows up in

the analysis of the hot-electron domain formation. We have found that the latter is associated with the passage of the control of electron heating to the collector electrode. States of a multiterminal RST device under general bias are 'adiabatically' connected to the anomalous states of the symmetric configuration at $V_D = 0$. The distribution of internal fields in the anomalous states is either fully symmetric, or these states form a set of partners and transform into one another under the symmetry operations. This type of analysis is likely to prove very potent with devices of more complicated symmetry, such as the NORAND, whose symmetry group is C_{3v} (see the bottom left diagram in figure 3).

We have demonstrated that some of the collector-controlled states remain stable in the symmetric bias configuration (e.g. the anomalous state **d** in figure 4). Experimentally, such states can be realized either by an ultra-short symmetric excitation $V_C(t)$ on the scale faster than the electron screening in the channel, or by a quasi-static variation of the symmetry-breaking bias V_D. In the latter case, the 'parasitic' instabilities, associated with the knees on the collector-controlled component of the current–voltage characteristic (figure 4), can be eliminated. Indeed, varying the device parameters (e.g. for $V_C > 2.25$ V), we found that these instabilities can be moved to higher values of V_D, well past the rightmost point **k** on the loop. Possible realization of the state **d** by a quasi-static variation of V_D may have memory applications and deserves further study.

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[17] We are not guaranteed, however, that all stationary points have been captured, because the graph may have other disconnected components.

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[19] This effect ($I_D < 0$ for $V_D > 0$) had been seen experimentally in RST transistors. However, it was usually attributed to spurious effects and never reported.

[20] In the 'normal' state of the device, for $V_D = 0$, the collector draws only a minimal current, determined by the height of the barrier and the temperature. In this state a variation of V_C has the sole effect of changing capacitively, as in a field-effect transistor, the electron concentration in the channel.

[21] Continuously varying V_C, we were able to realize the situation when the $I_D(V_D)$ curve only touches the $V_D = 0$ axis without crossing. At this singular point there is an accidental degeneracy of two symmetric states and the total number of distinct symmetric states becomes even.