Stony Brook University

Syllabus

1. Course Staff and Office Hours

Instructor: Dr. Peter Milder peter.milder@stonybrook.edu
Light Eng. 231

Office Hours: Tue. 2:00–4:00pm
Thu. 2:00–4:00pm
other hours by appointment

Office hours may change. Please check Blackboard for up-to-date information.

2. Introduction

The field of digital system design has entered a new and complicated era. Digital designers now have increasingly large amounts of chip area to exploit, but they are strictly limited by the amount of power that can be consumed per transistor (the so-called "power wall"). Modern design practices must carefully balance a variety of system tradeoffs such as power, energy, area, throughput, latency, bandwidth, and reusability/customization of digital systems. This course will study how new design abstractions, languages, and tools can help address these problems from the system designer's perspective.

3. Course Description

Content of the course will fall into roughly three categories:

1. **Limitations and Constraints of Modern Digital Systems:** the driving forces and limiting factors in current and near-future digital systems (the "power wall" and "utilization wall"); how these factors affect design practices and lead to a higher level of application-specific customization.

2. **Hardware Design Abstractions, Languages, and Tools:** register-transfer level design, simulation, and verification with the SystemVerilog hardware description language; parameterized "chip generator" tools; high-level synthesis (compilation of hardware from a high-level language); design-space exploration; domain-specific languages and tools.

3. **New Architectures and Paradigms:** the evolution of field-programmable gate arrays; coarse-grained reconfigurable architectures; heterogeneous and hybrid computer systems.

4. Course Catalog Description

This course focuses on languages, tools, and abstractions for design and implementation of digital systems. Course material is divided roughly into three categories: Limitations and constraints on modern digital systems; Hardware design abstractions, languages, and tools (including the SystemVerilog hardware description language); and new architectures and paradigms for digital design. Coursework will be primarily project based; there will also be reading and discussion of published papers in these areas. Students should have experience with hardware description languages (VHDL, Verilog, or SystemVerilog) and software (C, C++ or Java).
Fall, 3 credits, grading ABCF.

5. Objective

By the end of the course, students will understand the challenges and constraints of digital hardware design as well as how languages and design tools can help address these challenges and increase efficiency. Students will demonstrate this knowledge through written and oral paper reviews, a written midterm examination, and project work.

6. Readings

Readings for this course will be in the form of research papers, which will be distributed in class or online.

Optional reference: "SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling," Stuart Sutherland, Simon Davidmann, and Peter Flake. Springer. Paperback (2010, ISBN 978-1441941251) or Hardcover (2006, ISBN 978-0387333991).

7. Grading

Grades will be based on attendance and participation, homework assignments, one midterm examination, and projects.

Attendance and participation	10%
Assignments	20%
Midterm examination	20%
Projects	50%

8. Schedule

Classes will be held in Frey Hall room 216, from 4:00pm to 7:00pm on Wednesdays. Class begins on January 29. Class will meet every Wednesday except March 19 (Spring Recess). The final class will be on May 7.

A full schedule with topics, assignments, and due dates will be available on Blackboard.

9. Electronic Communication Statement

Email and especially email sent via Blackboard (http://blackboard.stonybrook.edu) is one of the ways the faculty officially communicates with you for this course. It is your responsibility to make sure that you read your email in your official University email account. For most students that is Google Apps for Education (http://www.stonybrook.edu/mycloud), but you may verify your official Electronic Post Office (EPO) address at http://it.stonybrook.edu/help/kb/checking-or-changing-your-mail-forwarding-address-in-the-epo.

If you choose to forward your official University email to another off-campus account, faculty are not responsible for any undeliverable messages to your alternative personal accounts. You can set up Google Mail forwarding using these DoIT-provided instructions found at http://it.stonybrook.edu/help/kb/setting-up-mail-forwarding-in-google-mail.

If you need technical assistance, please contact Client Support at (631) 632-9800 or supportteam@stonybrook.edu.

10. Disability

If you have a physical, psychological, medical or learning disability that may impact your course work, please contact Disability Support Services, 128 ECC Building (631) 632-6748. They will determine with you what accommodations are necessary and appropriate. All information and documentation is confidential.

Students who require assistance during emergency evacuation are encouraged to discuss their needs with their professors and Disability Support Services. For procedures and information go to the following web site: http://www.ehs.sunysb.edu and search Fire Safety and Evacuation and Disabilities.

11. Academic Honesty

Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another

person's work as your own is always wrong. Any suspected instance of academic dishonesty will be reported to the Academic Judiciary. For more comprehensive information on academic integrity, including categories of academic dishonesty, please refer to the academic judiciary website at http://www.stonybrook.edu/uaa/academicjudiciary/

12. Conduct

The University at Stony Brook expects students to maintain standards of personal integrity that are in harmony with the educational goals of the institution; to observe national, state, and local laws and University regulations; and to respect the rights, privileges, and property of other people. Faculty are required to report disruptive behavior that interrupts faculty's ability to teach, the safety of the learning environment, and/or students ability to learn to Judicial Affairs.