Analysis and Design of 3D Potentiostat for Deep Brain Implantable Devices

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1 Introduction

Impact of the implantable devices on the health care has been significant and the emerging technological innovations could lead to further breakthroughs in combating wide range of disorders [1, 2]. After the great success of pacemakers [3] and cochlear implants [4], the next generation of the implantable devices that interface the nervous system will have an extremely powerful impact on understanding neural pathways and neurological diseases. To achieve the deep brain implantation, the size of the device is the most stringent constraint due to limited area available in the local region of the brain. Furthermore, a tinier implant mitigates issues encountered during the implantation process, in addition to providing a more robust and longer *in vivo* monitoring and stimulation capability since the microsystem is less sensitive to body movements [5].

1.1 Potentiostat

Neurotransmitters are a class of biomolecules that carry signals across synapses. Real time detection and monitoring of neurotransmitters are highly critical for studies of neural pathways and the etiology of neurological diseases like epilepsy and stroke [6]. Traditionally, electrochemical analysis has been widely used due to high sensitivity and ability to perform distributed measurements [7]. A typical electroanalysis system contains a potentiostat that measures the *redox current* [6]. The magnitude of the redox current ranging from picoamperes to microamperes is proportional to the neurotransmitter concentration such as nitric oxide and dopamine. A three-electrode potentiostat consists of a working electrode (WE), on which an electrochemical reaction takes place; a reference electrode (RE), which is used to measure the solution potential; and a counter electrode (CE), which is an inert conductor supplying the current required for electrochemical reaction at WE. The potential difference between WE and RE is controlled by the potentiostat at a desired potential by adjusting the current at CE.

CMOS technology offers significant advantages to realize an efficient potentiostat such as reduction in size, power, and cost, while increasing the sensitivity and simultaneously recording neurotransmitter levels from a population of neurons rather than a single cell. For implantable applications, integrating multichannel potentiostats is a difficult task due to stringent constraints on area and power.

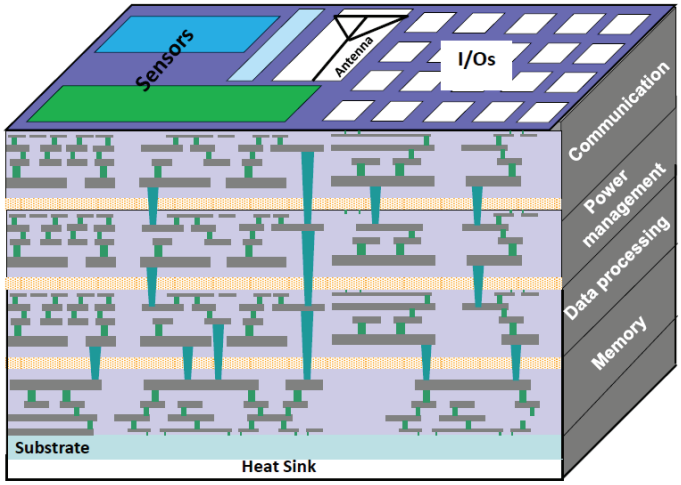


Figure 1: Monolithic 3-D integration technology where through silicon vias (TSVs) are utilized to achieve communication among the planes.

1.2 3D integration

In the past decade, three-dimensional (3-D) integration has emerged as a promising technology to achieve higher integration density (therefore reducing the overall area) and reduce the global interconnect length (therefore power dissipation) [8]. An illustrative example of such a system is shown in Fig. 1, where disparate planes such as sensors, circuit blocks for communication, power management, and data processing are stacked together [8]. Communication among the planes is achieved by vertical *through silicon vias* (TSVs). This hybrid integration capability offered by 3-D technology is highly advantageous for applications in life sciences since each plane can be individually optimized based on the required function and design objectives. For example, the communication plane is designed with physical parameters that enhance the realization of on-chip passive devices, a primary limitation for implantable device. Furthermore, the overall area of the system is reduced, achieving a smaller form factor.

As opposed to a 3-D integrated microprocessor where thermal stability is a primary concern, a 3-D integrated implantable device suffers from significant noise coupling due to dense integration and TSV characteristics.Noise management therefore emerges as a one of the significant limitations in highly heterogeneous 3-D integrated implantable devices. Several noise coupling mechanisms exist in a 3-D circuit through which switching noise can reach sensitive circuits, degrading the performance [9]. As the current magnitude in the neurotransmitter sensing applications ranges from picoamperes to microamperes, the signal is highly sensitive to switching noise.

The implementation of the implantable devices in 3D technology could lead to a significant leap in the implantable technology due to lower form factor and higher input sensitivity as compared to existing techniques. An important application of the implantable device technology with tremendous potential is the deep brain stimulation (DBS) [10, 11, 12]. This technique has been used in the treatment of Parkinson's disease, as well as different tremor disorders [13]. It has been shown that the deep brain stimulation is the most efficient tech-

nique in combating the Parkinson's disease [14, 15]. In existing technology, stimulation is performed through the four closely spaced electrodes placed in the localized brain regions. The stimulation electrodes are connected to a pulse generator through electrode wires. Pulse generator is an electronic device, typically implanted in the chest. This system requires a complex surgical operation and is extremely invasive [15]. A single device in 3D technology would negate the need for the wires that connect the electrodes to the pulse generator in the chest, significantly reducing the risks of infection and invasiveness of the surgical procedure. The recording the neurotransmitter concentration at the site of the stimulation will alleviate the need for the positioning of the stimulation electrodes and provide real-time feedback to the system [16]. The implementation of 3D potentiostat could therefore offer a new technology not only in the treatment of various neurological disorders (achieved by stimulation), but also in the study of these disorders and investigation of the optimal patterns of stimulation (achieved by recording).

2 Potentiostat Implementation in 2-D Technology

The potentiostat is fundamental to modern electrochemical studies using three electrode systems for investigations of reaction mechanisms related to redox chemistry and other chemical phenomena. Basically, a potentiostat has two main functions: 1) controlling the potential difference between WE and RE and 2) measuring the current flowing between WE and CE. To control the potential, a control amplifier with grounded WE or CE is generally used.

The low current measurement system can be realized with a few different circuit configurations. A resistive feedback trans-impedance amplifier based on an operational amplifier is the most typical continuous time current measurement system [17][18]. The operational amplifier clamps the input voltage and record the input current simultaneously. However, for the measurement of small currents, the size of the feedback resistor becomes prohibitively large in terms of area, bandwidth and noise.

To eliminate the negative influence of the resistor, a current integrator circuit based on the feedback capacitor can be used for low-current measurement systems with larger bandwidth. Several implementation of potentiostat with current integrators have been proposed [19][20][21]. In addition to the offset and finite gain of the operational amplifier, the performance of the capacitive feedback system is also degraded by charge injection from the switch capacitor circuits. The correlated double sampling structure can be used to eliminate effectively the charge injection, offset and low frequency noise.

A current conveyor circuit can amplify the low currents while applying the reference voltage without the use of operational amplifier [22][23]. The current conveyor is noisier and more vulnerable to mismatch between the transistors than the capacitor feedback amplifier.

We propose to directly inject the current to a current-mode incremental delta-sigma modulator. By directly integrating the current input within a current feedback modulator loop [6], we avoid the imprecision introduced by the amplification stage. The integration of the input current is embedded within a single-bit delta-sigma modulator loop implementing a first-order incremental analog-to-digital converter for increased sensitivity and integrated digital output. Range selection over 6 decades of input current is performed by a combination of variable duty cycle of current feedback and variable oversampling ratio in the delta-sigma modulator.

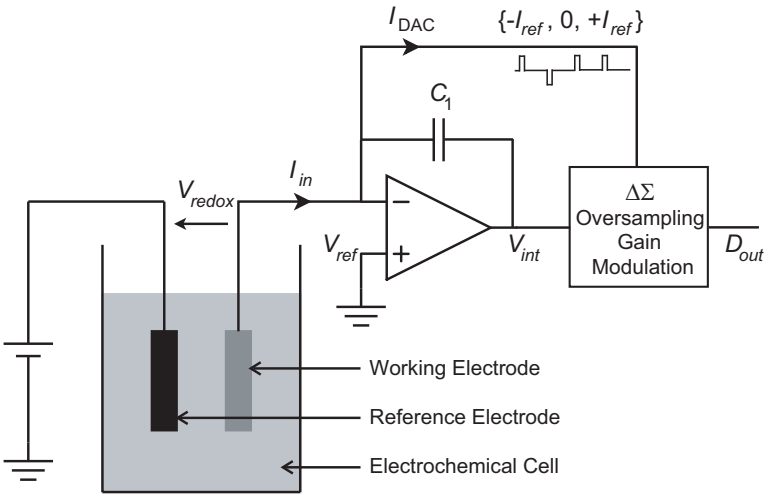


Figure 2: Simplified schematic of potentiostat system and interfacing electrochemical cell.

The simplified interface of the electrochemical cell and the fabricated potentiostat is shown in Figure 2.

2.1 Chip Architecture

For monitoring the concentration of the neurotransmitter molecules, we assume that the input current ranges from picoamperes to microamperes, with time scales ranging from milliseconds to seconds. This wide range of currents calls for multiple scales of measurement, while the long time constants allow for long integration times. Long integration times call for oversampling and support the use of a lower-order delta-sigma modulator. Delta-sigma oversampled data conversion avoids the need for low-pass anti-alias filtering in the input, and decimation reduces high-frequency noise present in the current signal along with the shaped quantization noise.

Wide dynamic range over multiple scales of input current is achieved by a gain-modulation scheme implemented as a variable duty cycle shunting sequence in the D/A feedback loop of the delta-sigma modulator. Digital control over the duty cycle of the shunting sequence directly sets the gain of input amplification, since the duty cycle effectively shunts the strength of the reference signal in the D/A feedback loop by the same factor. Digital shunting of the reference signal is more precise than analog scaling of the reference current, which is prone to mismatch errors. A precise gain factor G is achieved by passing the D/A feedback for a single clock cycle followed by $G - 1$ clock cycles of shunting the feedback. Even though the digital gain modulation over G clock cycles reduces the conversion rate by a factor G, it produces more precise results than increasing the delta-sigma oversampling ratio OSR by the same factor owing to reduced noise, as we analyze in Section 2.2 and experimentally validate in Section 2.3. With fixed reference current but variable feedback digital gain G and also variable oversampling ratio OSR, the potentiostat is capable of ranging digitally over a wide range of currents, spanning 6 decades from 100fA to 500nA.

The digitizing potentiostat is implemented as a first-order incremental ADC, a version of the first-order delta-sigma modulator with a counting decimator [24]. A block diagram for one channel of the potentiostat array is shown in Fig. 3. The first-order incremental topology is

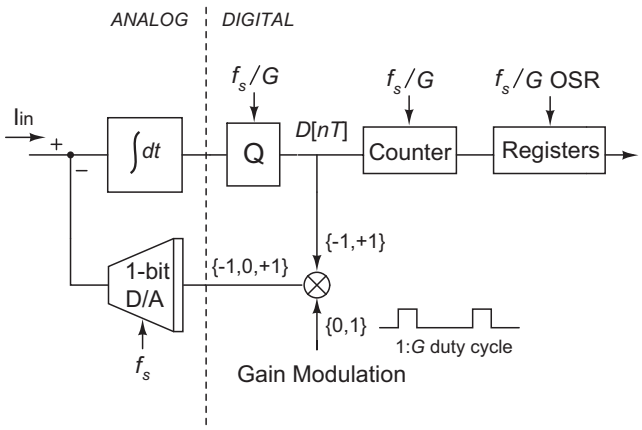


Figure 3: System level diagram of a single channel of the potentiostat.

amenable to simple and compact implementation, leading to significant savings in silicon area and power consumption. A sampled-data switched-capacitor (SC) realization offers low-noise and low-power implementation. Single-bit quantization leads to very robust circuits, relaxing linearity constraints in the design of the D/A converter with decreased sensitivity to mismatch errors. Gain modulation is implemented by shunting the D/A feedback, turning the binary $\{-1, +1\}$ feedback signal into a trinary $\{-1, 0, +1\}$ level signal.

The decimator is implemented using a binary counter, which is clocked synchronous with the rate of digital gain modulation, f_S/G. The decimated digital value is buffered in a register at the end of the conversion cycle, at a rate f_S / GOSR. The digital outputs from all 16 channels are read out asynchronously in bit serial form using an output shift register.

The first-order delta-sigma modulator comprises a current integrator, comparator, and switched-current single-bit D/A converter (DAC) with variable digital gain duty-cycle modulation. The integrator and switched-current DAC are shown in Fig. 4.

2.1.1 Current integrator

To achieve high resolution and minimize distortion, the input current is directly integrated onto a capacitor C_1 in the feedback loop of a low-noise high-gain sense amplifier, converting the integrated current into a voltage signal. One of two values of the current integrating capacitance C_1, 100fF or 1.1pF, is selected by the *scale* bit. The choice of integrating capacitance C_1 depends on the input current range and implies a trade-off between conversion speed and noise performance as analyzed in Section 2.2.

Instead of using a differential operational amplifier as high gain element in the current integrator, we have chosen to use a lower power, single ended inverting amplifier. Correlated double sampling (CDS) establishes the voltage at the virtual ground input to the integrator through a coupling capacitor C_2 inserted in between the integrator input and the inverting amplifier. The capacitor C_2 samples the difference between the inverting amplifier offset and the externally supplied voltage reference V_{ref} at the beginning of the conversion cycle, activated by the *intClk* clock signal. The capacitance C_2 is 1 pF to minimize the effect of charge leakage over the length of the conversion cycle.

The single-stage cascoded inverting amplifier is used as the high-gain amplifier in the cur-

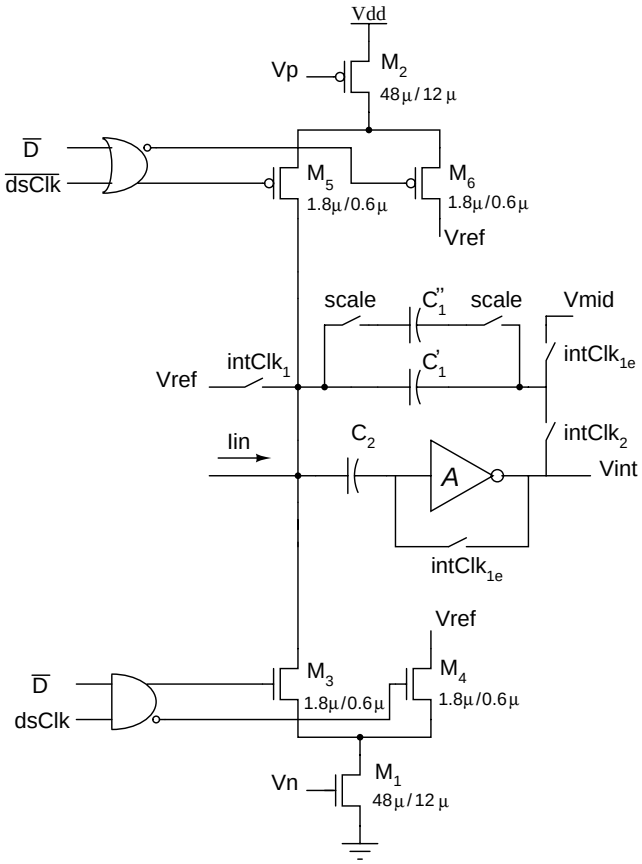


Figure 4: Schematic of delta-sigma current integrator with switched-current single-bit DAC.

rent integrator. The choice of telescopic operational amplifier without tail transistor results in high density of integration and reduced noise and power dissipation [25], and the CDS across the amplifier further reduces effects of flicker ($1/f$) noise [26]. For highest energy efficiency the amplifier is biased on the verge of the subthreshold regime, where the amplifier has maximum transconductance-to-current ratio and low power consumption. The subthreshold operation also provides extended output dynamic range with minimum drain-to-source saturation voltage. At 200 nA of biasing current, 1 pF load capacitance and 3 V supply, simulations indicate an open-loop dc gain of 91 dB and gain-bandwidth product of 844.3 kHz. No additional gain-boosting techniques were attempted, since the dc gain provided was sufficient for the target resolution.

2.1.2 Current feedback DAC

Single-bit D/A conversion and duty-cycle modulation in the delta-sigma feedback loop are implemented by a switched current circuit comprising transistors M_1 through M_6. The switched currents feed directly into the input node, where they are integrated along with the input current. The current sourcing transistors $M1$ and $M2$ generating tail currents $\pm I_{ref}$ are sized with large width and length ($W = 48\mu$m, $L = 12\mu$m) to improve matching between reference currents across channels. Bias voltages V_p and V_n are set with a single externally supplied

current reference I_{ref}. Transistors M_3, M_4, M_5 and M_6 implement minimum-size switches to direct the reference current either into the integrator or to a shunting path at the same reference voltage level V_{ref}. Therefore the current sources M_1 and M_2 are always active, and their drain voltage is maintained at the reference voltage level V_{ref}, decreasing the effect of charge injection noise at the integrator input.

Shunting of the feedback current is controlled by the digital gain modulation clock $dsClk$. When $dsClk$ is active, one polarity of reference current is injected into the integrating node depending on the quantization bit D from the comparator. When $dsClk$ is low, both currents are diverted to the shunting path and cancel onto the V_{ref} node.

2.1.3 Clock timing

The timing of all clocks is generated from a system clock $sysClk$ at sampling rate f_s, nominally 2MHz. Digital gain modulation is served by clock $dsClk$, active for a single cycle in every G cycles, at a rate f_s/G. Example waveforms of the integrator output for different values of G are shown in Fig. 5. The digital gain modulation clock $dsClk$ also clocks the counter in the decimator. The decimated output is available after OSR cycles of $dsClk$, at a conversion rate f_s / GOSR controlled by integrator clock $intClk$. Active during the first $dsClk$ cycle, $intClk$ buffers the decimated output and resets the integrator, comparator and counter for the next conversion cycle. Example clock signals $dsClk$ and $intClk$ generated from $sysClk$ are illustrated in Fig. 6; typical values of G and OSR are much larger in practice (between 1 and 2^{16}).

From the integrator clock $intClk$ non-overlapping clocks $intClk_1$ and $intClk_2$ are derived. The clock $intClk_{1e}$ is the replica of clock $intClk_1$ with rising edge following the rising edge of $intClk_1$ and falling edge preceding the falling edge of the clock $intClk_1$. All the switches are implemented with complementary transmission gate MOSFETs, except the switches controlled by $intClk_{1e}$, implemented as n-channel MOSFETs.

The operation of the modulator over one conversion cycle is summarized as follows. In the reset phase, at the beginning of the conversion cycle, $intClk_1$ is active which precharges C_1 in Fig. 4 to set the integrator input to reference voltage V_{ref} and set the integrator output to the mid point of the voltage range, V_{mid}. On the rising edge of $intClk_{1e}$ the inverting amplifier resets, charging C_2 to sample the difference between V_{ref} and the inverting amplifier threshold. The precharging operations are completed on the falling edge of $intClk_{1e}$, the external reference V_{ref} is disconnected on the falling edge of $intClk_1$, and the integration across C_1 starts on the rising edge of $intClk_2$. The sequence of clocks $intClk_1$, $intClk_{1e}$ and $intClk_2$ implements a correlated double sampling (CDS) operation which removes the offset of the amplifier and establishes a virtual ground at level V_{ref} at the input of the integrator.

The input current is continuously integrated on capacitor C_1, while the feedback current from the D/A converter is integrated only when the clock $dsClk$ is high, at a variable duty cycle set by digital gain G. The single-bit quantization result D from the comparator is latched on rising edge of clock $dsClk$.

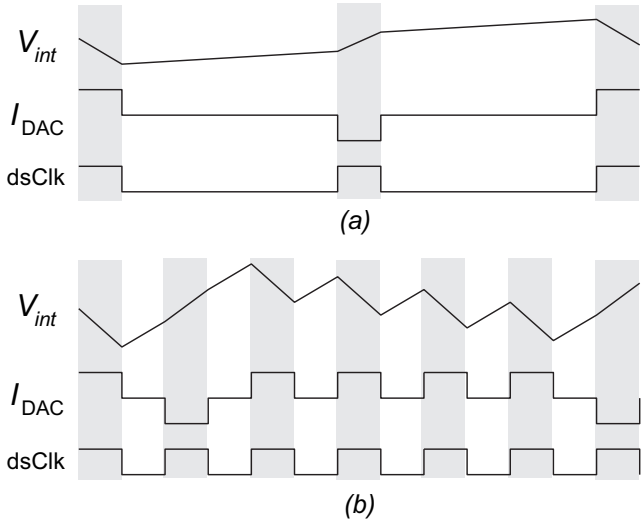


Figure 5: Effect of duty cycle modulation of delta-sigma feedback on the integrated current, illustrated for two values of digital gain G. *(a)* Lower scale of currents at $G = 6$. *(b)* Higher scale of currents at $G = 2$.

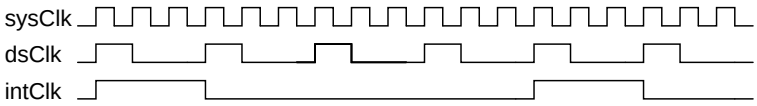


Figure 6: Gain modulation clock *dsClk* and integration clock *intClk*, illustrated for digital gain $G = 3$ and oversampling ratio OSR $= 4$.

2.1.4 Decimator and Serial Output

The decimator is implemented as the simple accumulate-and-dump circuit. The output bits of delta-sigma modulator that represent logic one are counted using 16-bit counter during one conversion period. The conversion period is programmable and represents the period of clock *intClk*. At the end of each conversion cycle, the counter value is written to output register and a new conversion cycle begins with cleared counter. The register can be read asynchronously at any time during conversion cycle. The 16 bits representing the digital value of input current of each channel are shifted out bit-serially using clock independent of system clock and 256 cycles are necessary to read out all 16 channels. The output serial bitstream is amenable to downlink telemetry in an implantable device for transcutaneous communication.

2.2 Performance Limitations and Noise

2.2.1 Range and Resolution

The incremental delta-sigma converter resets the integrator at the beginning of each conversion period. At time nT from reset, with $T = G/f_s$ the period of clock *dsClk*, the integrator output voltage V_{int} equals

$$V_{int}[n+1] = V_{int}[n] + (I_{in} - D[n]\frac{I_{ref}}{G})\frac{T}{C_1}, \tag{1}$$

where $D[n]$ is the comparator output (-1 or $+1$) at time nT, with initial conditions $V_{int}[0] = V_{mid} = 0$ and $D[0] = -1$. At the end of the conversion period, after a number of integration cycles equal to the oversampling ratio OSR, the integrator voltage reaches its final value

$$V_{int}[\mathrm{OSR}] = (\mathrm{OSR}\ I_{in} - \sum_{i=1}^{\mathrm{OSR}-1} D[i]\frac{I_{ref}}{G})\frac{T}{C_1}. \tag{2}$$

Therefore the input current I_{in} (or its average over the integration interval) decomposes into two terms as

$$I_{in} = \sum_{i=1}^{\mathrm{OSR}-1} D[i]\frac{I_{ref}}{G\ \mathrm{OSR}} + \frac{V_{int}[\mathrm{OSR}]}{\mathrm{OSR}}\frac{C_1}{T} \tag{3}$$

where the first term represents the decimated output, and the second term represents the conversion error. The decimated output term defines the LSB resolution of the input current as

$$I_{lsb} = \frac{2I_{ref}}{G\ \mathrm{OSR}}. \tag{4}$$

The resolution is thus given by the reference current I_{ref} scaled by both the digital gain G and the oversampling ratio OSR, whereas the range of input current $2I_{ref}/G$ is scaled by the digital gain G only. Correspondingly, the conversion rate f_{conv} equals

$$f_{conv} = \frac{f_s}{G\ \mathrm{OSR}} \tag{5}$$

which implies a linear trade-off between resolution and conversion bandwidth. This trade-off is further quantified in terms of the voltage range of the integrator.

From (3) the range of the integrator output voltage V_{int}, covering an LSB change in the quantized output, equals

$$V_{range} = 2\frac{I_{ref}}{G}\frac{T}{C_1} = 2\frac{I_{ref}}{f_s C_1} \tag{6}$$

which corresponds to the voltage excursion across the integrator with the reference current I_{ref} active over one master clock cycle $1/f_s$. By combining (4), (5) and (6) we obtain a more fundamental relation between resolution and bandwidth

$$I_{lsb} = f_{conv}\ C_1 V_{range}, \tag{7}$$

which reflects that the voltage excursion corresponding to an LSB increment in the input current over one conversion cycle covers the range of the integrator. From (7) the resolution I_{lsb} that can be attained for a given bandwidth f_{conv} depends only on the value of the integrating capacitor C_1. For a capacitance of 1.1 pF, the input current can be resolved with 100 fA sensitivity in 10 s, as is shown in Section 2.3, Fig. 8. For the smaller value of the integrating capacitance C_1 =0.1 pF, the conversion time is reduced to 1 s at the expense of increased thermal noise in the input voltage. For stability the capacitance C_1 should be larger than the parasitic capacitance at the potentiostat input divided by the gain of the inverting amplifier, which decreases with increasing frequency of fluctuations coupling into the input. The factor G reduction in the bandwidth of current feedback by gain modulation thus also contributes to the stability of the input voltage.

From (7), the current sensitivity appears to be independent of the digital gain G introduced through modulation of current feedback. The obtained resolution for a given conversion bandwidth and sampling rate depends only on the product of G and OSR, and would in principle be identical for an incremental data converter without gain modulation ($G = 0$) and with oversampling ratio G OSR. However, the introduction of digital gain modulation reduces the activity of current feedback onto the input and digital switching in the decimator, and thus reduces noise and power consumption at the same nominal sensitivity and conversion rate. To obtain the same nominal resolution I_{lsb}, the incremental data converter without gain modulation requires G OSR cycles of pulsed current integration, a factor G larger than the gain modulated converter. The effect of gain modulated noise on current sensitivity is analyzed next.

2.2.2 Noise Analysis

The main sources of circuit noise affecting the performance of the potentiostat and current data converter are the inverting amplifier in the integrator, and the DAC reference current sources.

The potentiostat voltage noise is determined by the input-referred voltage noise of the inverting amplifier, dominated by thermal noise of the input transistor operated in subthreshold. This noise contribution is shot noise limited with an input-referred spectral density [27]

$$v_{amp,n}^2 = 2{V_{th}}^2 \frac{q}{\kappa^2 I_b} \Delta f, \tag{8}$$

where $V_{th} = kT_{abs}/q$ is the thermal voltage, k is the Boltzmann constant, T_{abs} is absolute temperature, q is the elementary charge of the electron, κ is the gate effectiveness over bulk back-gate coupling and I_b is the bias current of the amplifier. The contribution of flicker ($1/f$) noise, the dominating noise source at low frequencies, is reduced owing to the effect of correlated double sampling (CDS) [28] across the input capacitor C_2, at the conversion rate f_{conv}. The switch injection noise sampled on capacitor C_2 represents a DC offset to the electrode voltage which is minimized by relatively large sizing of C_2 (1pF).

The input-referred current noise of the potentiostat and data converter is obtained by evaluating the effect of DAC current noise and integrator noise on the decimated output. According to (3), the effect of integrator noise in the decimated output is negligible since it amounts to a variation much smaller than an LSB. Noise in the reference current I_{ref} however directly impacts the decimated output since it is integrated along with the input current on C_1. The reference current noise density is given mainly by thermal noise in the DAC current sources $M1$ and $M2$

$$i_{ref,n}^2 = \frac{2}{3} 4kT_{abs} g_{m1} \Delta f, \tag{9}$$

where g_{m1} is the transconductance of the current sourcing transistor $M1$ operating above threshold. Other sources of noise acting on the DAC feedback current are flicker ($1/f$) and switch injection noise. The effect of $1/f$ noise contributed by M_1 and M_2 is minimized by large transistor sizing ($W = 48\mu$m, $L = 12\mu$m). Noise contributions by charge injection in transistors M_3 and M_5 to the integrated reference current are mimimized by the differential switching topology in Fig. 4 that maintains a constant V_{ref} potential on the drains of $M1$ and $M2$.

Each gain modulation current feedback cycle contributes the noise density (9) over approximately f_s bandwidth, resulting in a total input-referred noise power

$$\begin{aligned} i_{in,n}^2 &\approx \sum_{i=1}^{\mathrm{OSR}-1} \frac{i_{ref,n}^2}{G^2\mathrm{OSR}^2} \\ &\approx \frac{1}{G^2\mathrm{OSR}}\frac{2}{3}4kT_{abs}g_{m1}f_s \\ &= \frac{8}{3}kT_{abs}g_{m1}\frac{f_{conv}}{G}. \end{aligned} \tag{10}$$

The advantage of gain modulation $G > 1$ in improving the current sensitivity of the potentiostat is evident. G-fold gain modulation at G-fold increased reference current yields $\sqrt{G}$-fold reduction in input-referred noise power because of the weak square-root dependence of transconductance on current in $M1$ ($M2$) above threshold, $g_{m1} \propto \sqrt{I_{ref}}$. However, at given nominal target resolution I_{lsb} (4) and given conversion bandwidth (7), the reference current I_{ref} is fixed, and gain modulation yields a net G-fold reduction in input-referred noise power, and hence an $\sqrt{G}$-fold improvement in current sensitivity of the potentiostat (compare with Fig. 10 for experimental validation). Gain modulation also affords a G-fold reduction in dynamic digital power dissipation in the counting decimator owing to the resulting G-fold reduction in oversampling ratio OSR.

2.2.3 Power dissipation

Power dissipation is a limiting factor in the performance of the integrated potentiostat, especially for implantable applications with very low power budgets in the microwatt range. The power dissipation for one channel of the integrated potentiostat and data converter is approximated by

$$P_{diss} = 2I_{ref}V_{dd} + 2I_bV_{dd} + \frac{1}{G}f_{conv}C_{dec}V_{dd}^2 \tag{11}$$

where the first term accounts for both DAC sources $M1$ and $M2$, the second term corresponds to the integrator and comparator amplifiers, and the last term the dynamic power of the decimator with equivalent internal capacitive load C_{dec}.

The limit of energy efficiency for a given resolution G OSR can be readily estimated from (11). According to (4) and (7), the first term reduces to G OSR$C_1f_{conv}V_{range}V_{dd}$. The biasing of the inverting amplifiers in the second term can be minimized subject to bandwidth requirements. To accomodate a signal swing V_{range} in the integrator over a fraction $\lambda < 1$ of one integration cycle $T = G/f_s$,

$$I_b = \frac{1}{\lambda G}f_sC_1V_{range} \tag{12}$$

with an equivalent condition for the comparator biasing. The resulting power decomposes into analog and digital contributions

$$\begin{aligned} P_{diss} &= G\ \mathrm{OSR}f_{conv}\ (\frac{2}{\lambda G}+1)C_1V_{range}V_{dd} \\ &\quad +\frac{1}{G}f_{conv}C_{dec}V_{dd}^2. \end{aligned} \tag{13}$$

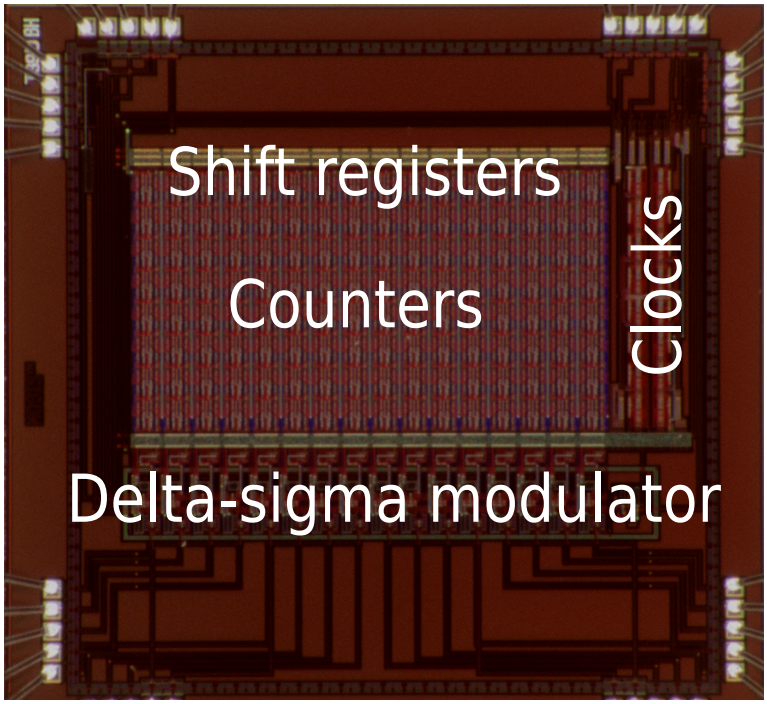


Figure 7: Micrograph of the 16-channel potentiostat. Die size is 3×3 mm^2 in 0.5 μm CMOS technology.

Gain modulation thus reduces the digital power, at the expense of analog power. Even so, for large G the analog power shows a linear dependence on resolution G OSR and bandwidth f_{conv}, tending to a constant figure of merit (FOM). The reciprocal of the FOM, defined as the energy consumed per conversion and per quantization level, is in the limit of large G

$$\frac{1}{FOM} = C_1 V_{range} V_{dd}. \tag{14}$$

For $C_1 = C_3 = 1$pF, $V_{dd} = 3$V, and $V_{range} = 0.5$V, the maximum attainable FOM is 0.7 conversions per pJ of energy. The experimental results confirm this FOM for the analog component of the dissipated power.

2.3 Experimental Results

The potentiostat system integrates 16 identical current input channels onto a single VLSI chip measuring 3×3 mm^2 in 0.5 μm CMOS technology. Figure 7 depicts the micrograph and system floorplan of the chip. Voltage reference levels V_{ref} are set individually for 4 groups each comprising 4 channels. Reference current I_{ref} of the feedback DAC, gain G and oversampling ratio OSR are set jointly for all 16 channels.

The power supply voltage is 3 V, with V_{mid} set to 1.5 V, and cascode biases set for a signal swing of 2.4 Vpp at the cascoded inverting amplifier output. These biases were provided off-chip for test purposes and would incur a small area and power penalty when integrated on-chip. For implantable use, it would also be necessary to generate reference voltages V_{ref}

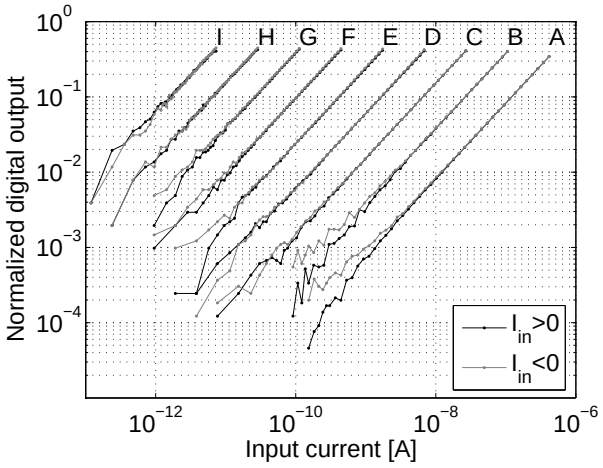


Figure 8: Normalized digital output of the chip for several values of digital gain G, oversampling ratio OSR and both polarities of input currents [30].

Table 1: Parameters for characterization traces shown in Fig. 8.

Trace	*Gain* (G)	*OSR*	*Input current range*	*Conversion time* (ms)	*Power* mW
A	2^0	2^{16}	±500nA	32	1.27
B	2^2	2^{15}	±125nA	65	0.97
C	2^4	2^{14}	±30nA	131	0.67
D	2^6	2^{13}	±8nA	262	0.57
E	2^8	2^{12}	±2nA	524	0.54
F	2^{10}	2^{11}	±500pA	1048	0.54
G	2^{12}	2^{10}	±125pA	2097	0.54
H	2^{14}	2^9	±30pA	4194	0.54
I	2^{16}	2^8	±8pA	8388	0.54

and reference current I_{ref} using on-chip D/A converters. A single clock and configuration bit sequence generates all clock signals internally. The output is read asynchronously in bit-serial form using a separate clock.

2.3.1 Chip Characterization

For performance characterization of the potentiostat chip, multiple input current sweeps were performed using a Keithley SourceMeter model 6430 (Keithley Instruments Inc., Cleveland, OH) controlled via a GBIP interface. In the following tests, the system clock frequency f_s was set to 2 MHz, the DAC reference current I_{ref} was set to 500 nA, and the amplifier bias I_b was set to 200 nA. The input potential V_{ref} was set to 1 V. The digital gain G and oversampling ratio OSR were programmed individually for each test, varying between 1 and 2^{16}.

To verify the range and precision of the potentiostat at fixed value of the reference cur-

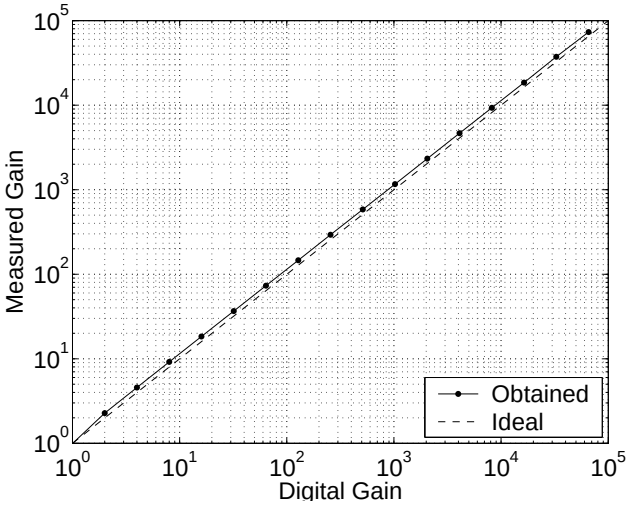
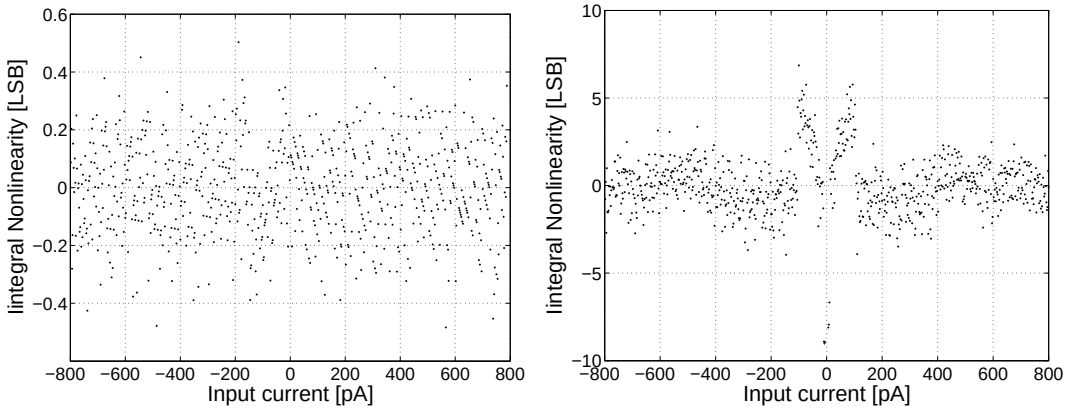


Figure 9: Actual gain as a function of digitally programmed gain G of current measurement.

rent, we swept the input currents logarithmicly over a range spanning over six orders of magnitude [29]. Figure 8 [30] shows the normalized digital output of the chip as a function of input current. The normalization is necessary for comparison across various scales. The gain G, oversampling ratio OSR, and corresponding range of input currents I_{range}, conversion time $1/f_{conv}$ and power dissipation P_{diss} are shown in Table 1 for each of the traces in Fig. 8. The value of the integrating capacitor C_1 was kept at 1.1 pF. In each consecutive sweep, the conversion time was doubled, while the value of current corresponding to the least significant bit was decreased four-fold illustrating the trade-off between conversion speed and resolution of measurement. Figure 9 shows the relation between the digitally programmed gain G and the actual measured gain [31].

The analog power consumption by the chip, covering all 16 integrators, 16 comparators and bias circuits measured 53 μW, identical for each of the range selections in Fig. 8. We did not adapt the amplifier bias (I_b =200 nA) with the value of digital gain G which would lead to further power savings at high G values. At 3.3 μW per channel, the resulting FOM is 0.6 conversions per pJ consistent with (14). The measured digital power consumption by the chip ranged from 1.2 mW for digital gain $G = 1$ down to 495 μW for gains larger than $G = 2^8$. This power measure covers clock generation and bit-serial readout in addition to the 16 decimators. Therefore we anticipate the 495 μW asymptote of the measure excludes the array of decimators, and the digital power ranges between 0 and 44 μW per channel. Digital power consumption could be further reduced by low-power digital design techniques such as Gray-level counters for the decimators.

To demonstrate the utility of digital gain by $1/G$ duty-cycle modulation of current feedback, we compared the sensitivity for digital gain G with that for an equivalent increase in oversampling ratio GOSR. The value of the integrating capacitor C_1 was set at 0.1 pF and a current reference I_{ref} value was 256 nA. The input current was swept from -800 pA to 800 pA in steps of 2 pA. This sweep range covers the $\pm$1 nA range selected by a digital gain G set to 256. Over the same range, the input is observed at the same effective 8-bit resolution by the setting $G = 1$ and OSR = 2^{16}. The integral nonlinearity (INL) measured for both settings



(a) (b)

Figure 10: Measured integral non-linearity (INL) for *(a)* digital gain $G = 256$ and oversampling OSR $= 256$; and *(b)* $G = 1$ and OSR $= 2^{16}$ evaluated over the same range.

of digital gain and oversampling ratio are shown in Fig. 10. As predicted in Section 2.2, even though both settings have the same nominal resolution $1/G\text{OSR}$, the setting with larger digital G gives lower error. The measured improvement in sensitivity in Fig. 10 (a) over (b) is consistent with the $\sqrt{G}$-fold improvement predicted for $G = 256$. The instability in the center region of Fig. 10 (b) is due to the small feedback capacitance $C_1 = 0.1$ pF and increased input capacitance of the autoranging sourcemeter instrument at its lowest scales.

The measured characteristics are summarized in Table 2.

3 3-D Integrated Implantable Devices

The primary purpose of this study is to investigate the switching noise and noise coupling characteristics within heterogeneous 3-D implantable devices. As an example, signal integrity and noise coupling characteristics of a 2-D and 3-D integrated neurotransmitter sensing device are investigated and compared [32]. An electrical model is developed for the substrate, power network, and through silicon vias (TSVs). These models are combined with the neurotransmitter sensing circuit to generate an entire model to analyze signal integrity. To manage computational complexity, the proposed signal integrity analysis focuses on a single channel that consists of a first order delta-sigma modulator, counter for decimation, and shift register, as depicted in Figure 3.

The counter is the primary aggressor whereas the sense amplifier within the current integrator is identified as one of the primary victim blocks. The switching noise that couples from the counter to the sense amplifier is analyzed for different scenarios.

3.1 3-D Electrical Models

The model to analyze switching noise coupling consists of two primary items: (1) monolithic substrate and (2) TSVs.

Table 2: Multi-Channel Potentiostat Characteristics

Technology	0.5 μm 2P3M CMOS
Size	3 mm $\times$ 3 mm
Supply	3 V
Current inputs	16
Current range	100 fA to 1 uA
Minimum detected current	100 fA
Power dissipation	
Array:	
Analog	4.3 uW / chan.
Digital	44/G uW/ chan.
Chip total	450 uW - 1.2mW

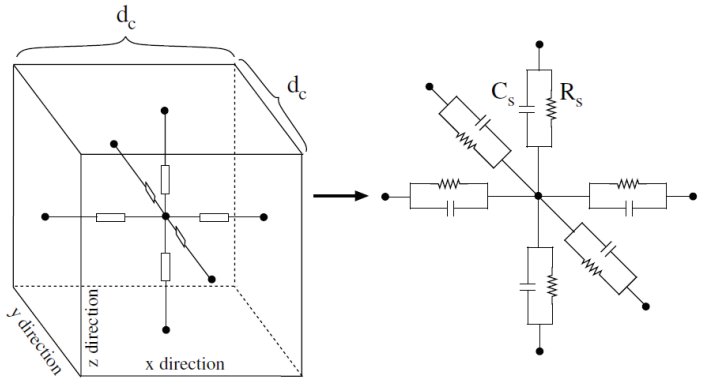


Figure 11: Discrete model of a substrate where each unit is represented by six resistances and capacitances.

3.1.1 Substrate Model

The substrate corresponding to a single channel of the sensing chip is discretized in three dimensions where each cuboid is modeled using RC impedances, as depicted in Fig. 11 [33]. According to this figure, substrate resistance R_s and capacitance C_s are, respectively,

$$R_s = \frac{1}{2}\frac{\rho_s}{d_c}, \tag{15}$$

$$C_s = \epsilon_s 2 d_c, \tag{16}$$

where ρ_s is the substrate resistivity and ϵ_s is the dielectric permittivity of silicon. A bulk type substrate with ρ_s=10 Ωcm is assumed. Note that each dimension of the unit cuboid d_c is 9 μm. To model of the overall substrate of the single channel, a total of 90, 16, and 3 cuboids

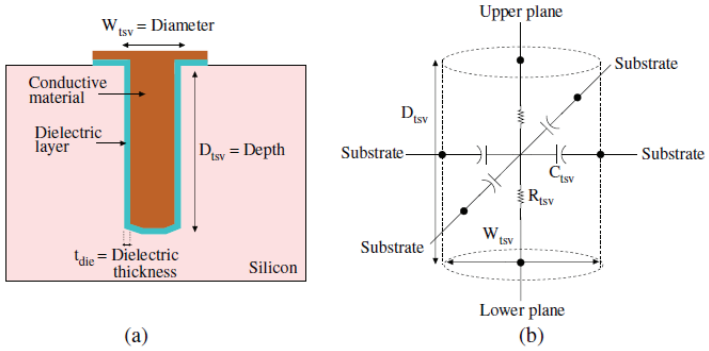


Figure 12: TSV representations: (a) Cross section of a TSV consisting of a conductive material and a dielectric layer, (b) electrical model of a TSV.

are required, respectively, in the x, y, and z directions. Note that the sufficient accuracy of this model has been previously demonstrated [33].

3.1.2 TSV Model

As depicted in Fig. 12(a), a typical TSV is represented as a cylinder with a diameter W and depth D and consists of two parts: (1) conductive material such as copper or tungsten, (2) a dielectric layer that surrounds the conductive material. The dielectric layer, consisting of TiN or TaN, forms a barrier to prevent the conductive material from diffusing into the silicon [8]. The thickness of this dielectric layer t_{die} is in the range of 0.2 μm to 1 μm [34]. In this analysis, t_{die} is assumed to be 0.2 μm.

Aspect ratio of a TSV is determined by D/W. These parameters vary depending upon the specific fabrication technology [8]. For typical 3-D technologies, the diameter of a TSV is in the range of 5 μm to 10 μm whereas the depth varies from 25 μm to several hundred μm [34]. Note that the TSV depth is primarily determined by the wafer thinning capability of the TSV fabrication process. In this analysis, a TSV depth of 27 μm (3x9 μm) is assumed.

An electrical model for the TSV is shown in Fig. 12(b) where the TSV is represented by an L shaped, 2-stage distributed RC circuit. Note that the resistance represents the conductive material whereas the capacitance models the dielectric layer. TSV resistance R_{tsv} and capacitance C_{tsv} are, respectively [35],

$$R_{tsv} = \frac{1}{2}\frac{\rho_c D_{tsv}}{\pi (W_{tsv})^2}, \tag{17}$$

$$C_{tsv} = \frac{1}{2}\frac{\pi \epsilon_{sio2} D_{tsv}}{\ln[\frac{(w/2)+t_{die}}{w/2}]}, \tag{18}$$

where ρ_c is the copper resistivity and ϵ_{sio2} is the dielectric permittivity of silicon dioxide. Note that (15) is based on a cylindrical capacitor formula. Sufficient accuracy of this model has been previously demonstrated [35]. The results of the signal integrity analysis are presented in the following section.

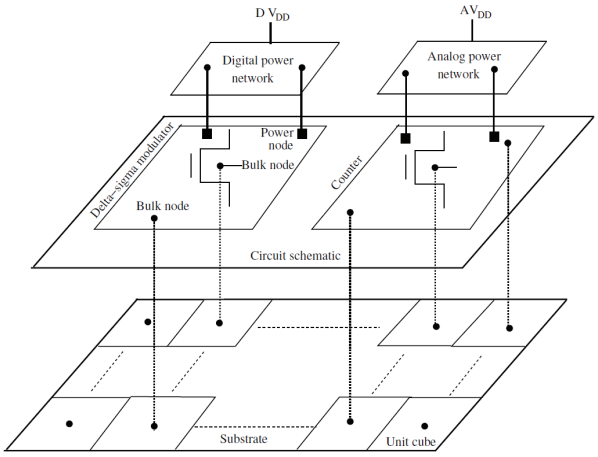


Figure 13: Conceptual representation of the overall model to analyze signal integrity in a 2-D neurotransmitter sensing device.

3.2 Signal Integrity Analysis

Both the substrate and TSV models described in the previous section are utilized in this section to generate an entire electrical model for a single channel of a neurotransmitter chip in both 2-D and 3-D technologies. These models are used to analyze signal integrity in both cases, as described in the following subsections.

3.2.1 2-D Neurotransmitter Sensing Device

The bulk nodes of the transistors (in the circuit schematic view) located within an area of 81 μm^2 are lumped together and connected to the corresponding node on the substrate model, as depicted in Fig. 13. The physical layout of the circuit is utilized to determine the relative location of the blocks in the schematic. Note that those nodes of the substrate that are connected to a substrate contact (tap) including guard rings are biased with the ground voltage in order not to obtain overly pessimistic results. Also note that a lumped resistance of two Ωs and a lumped inductance of one henry is used to model the parasitic effects of both on-chip and off-chip power distribution networks. Thus, an entire electrical model considering the substrate and nonideal power network is generated by connecting the bulk nodes in the circuit schematic to the corresponding nodes on the substrate model.

Since the circuit is designed in 0.5 μm CMOS technology, the overall model is also analyzed in the same technology using Spectre. The noise at the bulk node of a victim device within the delta-sigma modulator is observed for two different cases: (1) when the digital and analog parts of the circuit share a common power network, (2) when the digital and analog parts have dedicated on-chip power networks. Results of a transient analysis is shown in Fig. 14 where the peak noise is illustrated for the aforementioned two cases. Positive peak noise coupling to the victim device is in the range of 3 mV. The effect of utilizing a dedicated on-chip power network for the analog and digital blocks is not significant primarily because off-chip parasitic impedances are dominant. Common substrate forms a conductive medium for the switching noise to reach the victim devices. The rms value of the noise over 10 μs is approximately 232

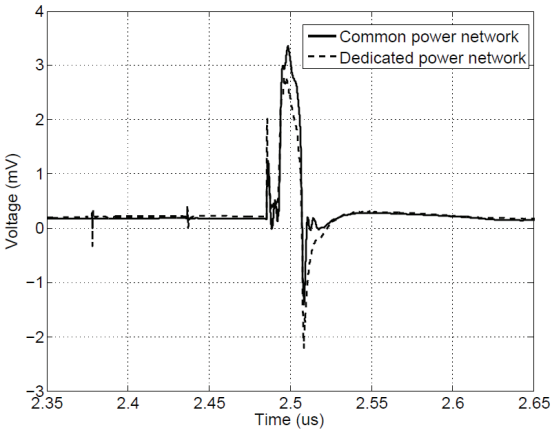


Figure 14: Transient analysis results illustrating peak noise at the bulk node of a victim device for two different cases in a 2-D neurotransmitter sensing device.

μV for common power network whereas the noise is reduced only to 224 μV for dedicated power network. Noise analysis results for the 3-D integrated neurotransmitter sensing device is described in the following section.

3.2.2 3-D Neurotransmitter Sensing Device with Two Stacked Planes

In the 3-D integrated version of the neurotransmitter sensing device, the aggressor (counter) and victim (delta-sigma modulator) are placed on separate planes. Specifically, the top plane (closer to the I/O pads) is dedicated to the victim block whereas the bottom plane (closer to the heat sink) is dedicated to the aggressor block. A 3-D electrical model is generated using the aforementioned substrate and TSV models, as depicted in Fig. 15.

Similar to the 2-D model, the bulk nodes within the schematic are connected to the corresponding nodes on the substrate. In this case, however, two separate substrates exist: (1) substrate of the bottom plane where the bulks of the counter are connected, and (2) substrate of the upper plane where the bulks of the delta-sigma modulator are connected.

As depicted in Fig. 15, a face-to-face bonding technology is assumed with via-first fabrication technique. In this technique, the TSVs go through the upper (analog) substrate and reaches the metal layers of the analog plane. The top most metal layer of the analog plane is connected to the top most metal layer of the digital plane using bumps. Note that a TSV pitch of 9 μm is assumed. Thus, there is at least a single free unit cuboid between the TSVs on the analog substrate. Since only a single channel of the device is modeled, a total of eight TSVs are sufficient. Five TSVs are for the clock signals, two TSVs are used to transmit the power supply voltage, and the remaining TSV is used to route a data signal.

Similar to the 2-D model, a transient analysis is performed and the noise at the bulk of the same victim device is observed. Peak noise is illustrated in Fig. 16 for two different cases: (1) nonideal TSVs with practical capacitance values, (2) ideal TSVs with zero capacitance value. Note that the result of the 2-D analysis (with dedicated power networks) is also included for comparison. As depicted in this figure, the 3-D system with practical TSVs, despite having separate substrates for digital and analog, exhibit significantly higher noise (positive peak

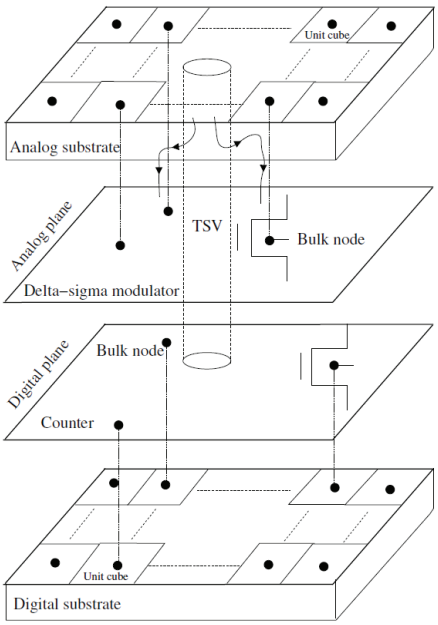


Figure 15: Conceptual representation of the overall model to analyze signal integrity in a 3-D neurotransmitter sensing device.

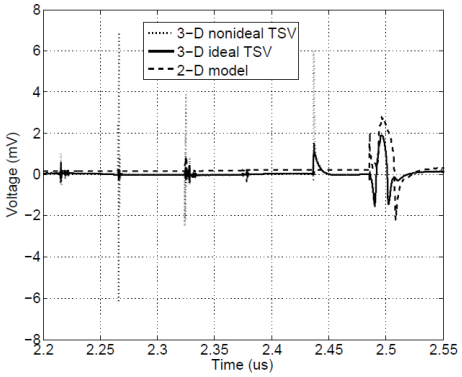


Figure 16: Transient analysis results illustrating peak noise at the bulk node of a victim device for two different cases in a 3-D neurotransmitter sensing chip.

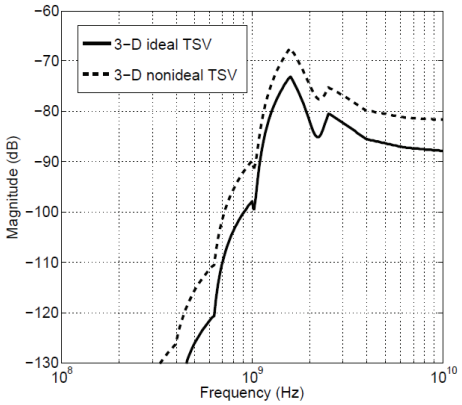


Figure 17: AC analysis results showing the amount of transferred noise from the clock signals to the victim bulk in a 3-D neurotransmitter sensing chip.

Table 3: RMS value of the noise at the bulk node over 10 μs for different cases.

Case	RMS noise at the bulk node
2-D common power network	232 μV
2-D dedicated power network	224 μV
3-D nonideal TSV	242 μV
3-D ideal TSV	107 μV

noise exceeds six millivolts) than the 2-D system.

To evaluate the primary noise coupling mechanism, the capacitance C_{tsv} in Fig. 12(b) of the clock TSVs is removed, producing an ideal clock TSV with no coupling into the substrate. In this case, the peak noise is significantly reduced (to approximately two millivolts) and is smaller than the 2-D system. Thus, in a 3-D system, significant noise couples into the substrate through clock TSVs, as depicted in Fig. 15. This behavior is also analyzed by investigating the AC response. The amount of transferred noise from the clock signals to the victim bulk is shown in Fig. 17 as a function of frequency. According to this figure, the transferred noise is at least 5 dB higher when practical TSVs are used. Note that the ideal TSV is only for the clock TSVs. Noise can still couple into the substrate through the remaining three TSVs (power and data). Finally, the rms value of the noise over 10 μs is listed in Table for all of the cases. The advantage of 3-D technology in terms of noise is obtained only when TSV related noise coupling is alleviated. The implications of this result on the design process are discussed in the following section.

3.3 Discussion

Despite the significant advantages of 3-D integration technology in hybrid systems, TSV related noise coupling is identified as an important limitation. For implantable applications such as the neurotransmitter sensing device analyzed in this work, the top plane should be dedicated to the highly sensitive frontend circuits due to physical proximity to the pads. In this case, however, clock TSVs with short rise times inject significant noise into the substrate of the analog plane since these signals need to reach the bottom plane where the digital circuit

is placed. This coupling mechanism is due to the TSV-to-substrate capacitance C_{tsv} of the TSVs. The distance between an aggressor TSV and a victim device should be carefully considered. Furthermore, efficient and 3-D specific noise isolation strategies should be developed to minimize the effect of TSV related noise coupling on the sensitive circuits.

4 Conclusion

We presented a 16-channel 2-D potentiostat array architecture with a wide dynamic range of currents that span through six orders of magnitude from picoamperes to microamperes and sensitivity down to 100 fA. The current range is controlled through programmable feedback duty-ratio cycle. Signal integrity characteristics of a 2-D and 3-D integrated potentiostat are analyzed. An electrical model is developed to consider the substrate, nonideal power network, and TSVs. Contrary to the common assumption and despite having two separate substrates, 3-D systems do not necessarily exhibit superior noise performance due to TSV related noise coupling. Ignoring this noise coupling mechanism produces 3-D implantable devices with significantly poor signal integrity characteristics.

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