Efficient Characterization of TSV-to-Transistor Noise Coupling in 3D ICs

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ABSTRACT

A methodology is proposed to characterize TSV induced noise coupling in three-dimensional (3D) integrated circuits. Different substrate biasing schemes (such as a single substrate contact versus regularly placed substrate contacts) and TSV fabrication methods (such as via-first and via-last) are considered. A compact π model is proposed to efficiently estimate the coupling noise at a victim transistor. Each admittance within the compact model is approximated with a closed-form expression consisting of logarithmic functions. The methodology is validated using a 3D transmission line matrix (3D-TLM) method, demonstrating, on average, 4.8% error. The compact model and the closed-form expressions are utilized to better understand TSV induced noise as a function of multiple parameters such as TSV type and placement of substrate contacts.

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]: [Miscellaneous]

Keywords

Compact model; TSV; Noise; 3D IC

1. INTRODUCTION

Three-dimensional (3D) integrated circuits (ICs) address some of the critical issues encountered in planar technologies such as the adverse effects of global interconnects [1]. Furthermore, heterogeneous integration of diverse circuits and materials is facilitated. Through silicon via (TSV) based 3D technology is among the most promising vertical integration technologies due to relatively high density vertical interconnects [2]. International Technology Roadmap for Semiconductors identifies three phases for the application of 3D technology: (1) memory stacks, (2) processor-memory stacks, and (3) heterogeneous 3D integration with sensing and communication blocks.

An important challenge in each of these applications is to ensure system wide signal integrity. In addition to traditional noise coupling and propagation mechanisms such as crosstalk, power supply noise, and substrate coupling, 3D circuits also suffer from TSV induced noise coupling [3]. Specifically, during a signal transition within a TSV, noise couples into the substrate due to both dielectric and depletion capacitances. The coupling noise propagates throughout the substrate and affects the reliability of nearby transistors. This issue is exacerbated for TSVs that carry signals with high switching activity factors and fast transitions such as clock signals.

Existing works have investigated the effect of TSV geometry and substrate type on noise propagation [4]. The efficacy of traditional techniques (such as guard rings) in reducing TSV induced noise has also been investigated [5]. These studies, however, do not consider different substrate biasing schemes and distinct TSV fabrication methods. Furthermore, computationally expensive approaches (such as 3D electromagnetic extraction) are utilized, prohibiting the use of these approaches for fast evaluation of different physical structures during the early stages of TSV floorplanning.

The primary contributions of this paper are: (1) a compact model and a closed-form expression for each admittance within this model are developed to efficiently estimate TSV induced noise at a victim transistor, (2) these models (validated using a 3D transmission line matrix method) are sufficiently flexible to consider different substrate biasing schemes and both via-first and via-last TSV characteristics, and (3) design guidelines are provided to reduce TSV induced noise based on the results obtained from these models.

The rest of the paper is organized as follows. A highly distributed electrical model (used as a reference) to analyze noise injection and propagation is described in Section 2. A compact π model is proposed in Section 3 for efficient estimation of TSV induced noise at a victim transistor. To consider different substrate biasing schemes and TSV types, each admittance within the compact model is expressed in Section 4 as a function of multiple physical parameters. The results are discussed and design guidelines are provided in Section 5. Finally, the paper is concluded in Section 6.

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2. DISTRIBUTED MODEL FOR TSV INDUCED NOISE COUPLING

The TSV and substrate models are provided, respectively, in Sections 2.1 and 2.2. These models are based on discretizing the physical structure into unit cells and modeling each unit cell with lumped parasitic impedances. Also referred to as 3D transmission line matrix method (3D-TLM) [6], the

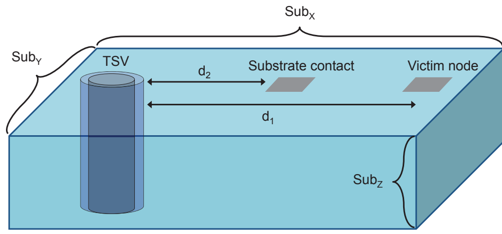

Figure 1: Physical structure discretized based on 3D TLM method to analyze TSV induced noise coupling.

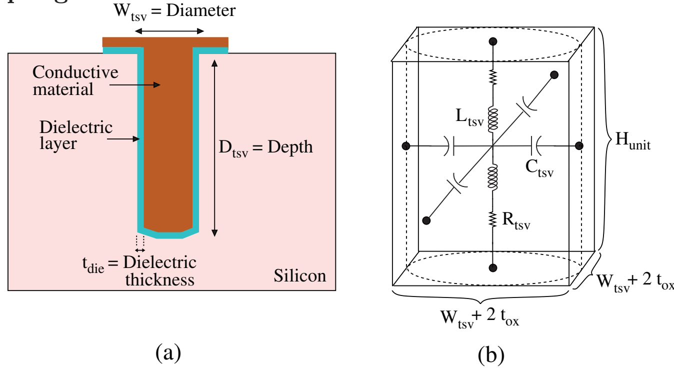

Figure 2: TSV representations: (a) cross-section of a TSV consisting of a conductive material and dielectric layer, (b) electrical model of a unit cell TSV used for discretization.

accuracy of this technique has been previously verified by comparing the results with 3D field solvers [5] and experimental data [7]. This distributed model is used as a reference in this paper to validate the proposed compact model (see Section 3) and closed-form expressions (see Section 4).

2.1 TSV Model

A typical TSV is represented as a cylinder with a diameter and depth, as illustrated in Fig. 2(a). The two primary components of a TSV are (1) conductive filling material such as polysilicon (for via-first TSVs), tungsten (for via-middle TSVs), and copper (for both via-middle and via-last TSVs), (2) a dielectric layer that surrounds the conductive part to prevent the filling material from diffusing into the silicon [8]. In this study, noise coupling analysis is achieved for both via-first and via-last TSVs.

A TSV unit cell consisting of a parasitic resistance R_{tsv}^{unit}, parasitic inductance L_{tsv}^{unit}, and capacitance to substrate C_{tsv}^{unit} is illustrated in Fig. 2(b) [9]. The x and y dimensions of the unit cell are both equal to $W + 2t_{ox}$ as determined by the TSV diameter W and thickness of the oxide layer t_{ox}. The z dimension is equal to H_{unit} as determined by the TSV height and the required resolution in the transmission line matrix method.

Considering the skin effect, the unit TSV resistance R_{tsv}^{unit} is determined by [10]

$$R_{tsv}^{unit} = \frac{1}{2}\sqrt{(R_{AC}^{tsv,unit})^2 + (R_{DC}^{tsv,unit})^2}, \quad (1)$$

where the DC resistance $R_{DC}^{tsv,unit}$ and AC resistance $R_{AC}^{tsv,unit}$ are, respectively,

$$R_{DC}^{tsv,unit} = \frac{1}{2}\frac{\rho_f H_{unit}}{\pi(W/2)^2}, \quad (2)$$

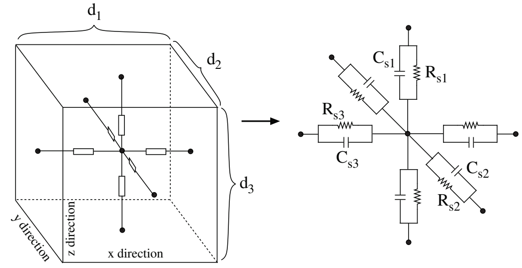

Figure 3: Distributed model of a substrate network where each unit cell is represented by six resistances and capacitances.

$$R_{AC}^{tsv} = \frac{\rho_f H_{unit}}{4\pi(W/2)\delta_{tsv}}. \quad (3)$$

ρ_f is the conductivity of the filling material and the skin depth δ_{tsv} is

$$\delta_{tsv} = \frac{1}{\sqrt{\pi f \mu_f \rho_f}}, \quad (4)$$

where f is the frequency and μ_f is the permeability of the filling material. The unit TSV inductance L_{tsv}^{unit} is

$$L_{tsv}^{unit} = \frac{1}{2}\frac{\mu_o}{4\pi}[2H_{unit}\ln(\frac{2H_{unit} + \sqrt{(W/2)^2 + (2H_{unit})^2}}{W/2}) + (W/2 - \sqrt{(W/2)^2 + (2H_{unit})^2})], \quad (5)$$

where μ_o is vacuum permeability. The unit TSV capacitance C_{tsv}^{unit} is determined from the cylindrical capacitor formula as [11]

$$C_{tsv}^{unit} = \frac{1}{4}\frac{2\pi\epsilon_{ox}H_{unit}}{\ln(\frac{W/2+t_{ox}}{W/2})}, \quad (6)$$

where ϵ_{ox} is the oxide permittivity.

2.2 Substrate Model

A lightly doped bulk type substrate is assumed. Note that an epi type substrate with a heavily doped bulk beneath the lightly doped silicon layer typically produces greater noise coupling and is therefore less applicable to 3D heterogeneous integration where circuits with distinct electrical characteristics coexist.

A similar discretization technique is applied to model the lightly doped substrate. A unit substrate cell consisting of six parallel RC admittances is illustrated in Fig. 3. Referring to this figure, the three substrate resistances R_{s1}, R_{s2}, and R_{s3} are, respectively,

$$R_{s1} = \frac{1}{2}\frac{\rho_s d_3}{d_1 d_2}, \quad (7)$$

$$R_{s2} = \frac{1}{2}\frac{\rho_s d_2}{d_1 d_3}, \quad (8)$$

$$R_{s3} = \frac{1}{2}\frac{\rho_s d_1}{d_2 d_3}, \quad (9)$$

where ρ_s is the substrate resistivity. Similarly, the three substrate capacitances C_{s1}, C_{s2}, and C_{s3} are, respectively,

$$C_{s1} = 2\frac{\epsilon_s d_1 d_2}{d_3}, \quad (10)$$

$$C_{s2} = 2\frac{\epsilon_s d_3 d_1}{d_2}, \quad (11)$$

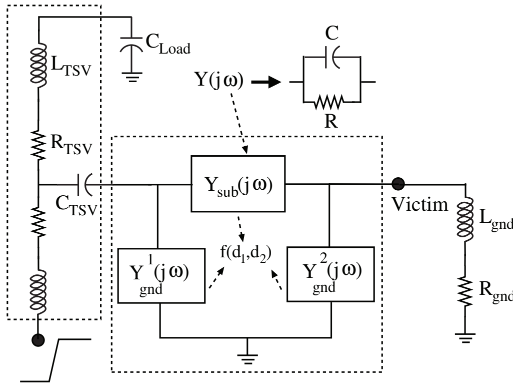

Figure 4: Compact π model to efficiently estimate the noise at the victim node in the presence of a TSV and substrate contacts.

$$C_{s3} = 2\frac{\epsilon_s d_2 d_3}{d_1}, \tag{12}$$

where ϵ_s is the dielectric permittivity of silicon.

The TSV and the substrate unit cells are combined to produce a highly distributed mesh based on 3D TLM. Substrate contacts are also considered in the model to properly bias the substrate. Despite the reasonable accuracy achieved by this model [5, 7], the computational complexity is significantly high, particularly when the dimensions of the unit cells are small. This issue is exacerbated as the distance between the TSV and victim transistor increases. Furthermore, the number and location of the substrate contacts play an important role in characterizing the TSV safe zone. Reanalysis of the distributed structure when these characteristics change is computationally prohibitive. A compact model is proposed to alleviate these limitations, as described in the following section.

3. COMPACT Π MODEL FOR EFFICIENT TSV NOISE COUPLING ANALYSIS

A two-port, linear time-invariant network can be generally characterized with four admittances: $Y_{11}(j\omega)$, $Y_{12}(j\omega)$, $Y_{21}(j\omega)$, and $Y_{22}(j\omega)$. Utilizing this characteristic, the proposed compact model consists of a single cell TSV and an equivalent two-port π network to model noise propagation, as depicted in Fig. 4. Each electrical element within the π network consists of a parallel RC circuit, producing an admittance $(1/R) + j\omega C$. These admittances are obtained from the distributed model (based on 3D TLM) described in the previous section. Specifically, the four $Y(j\omega)$ parameters of the distributed mesh is obtained through an AC analysis. The resistances and capacitances of the π network are determined such that the four $Y(j\omega)$ parameters of the two networks are equal. According to this procedure, the $Y(j\omega)$ parameters of the π network $Y_{sub}(j\omega)$, $Y^1_{gnd}(j\omega)$, and $Y^2_{gnd}(j\omega)$ are determined as follows:

- $Y_{sub}(j\omega) = (1/R_{sub}) + j\omega C_{sub} = Y_{21}(j\omega)$: represents the equivalent substrate admittance between the TSV and victim transistor.
- $Y^1_{gnd}(j\omega) = (1/R^1_{gnd}) + j\omega C^1_{gnd} = Y_{11}(j\omega) - Y_{21}(j\omega)$: represents the equivalent substrate admittance between the TSV and ground node.

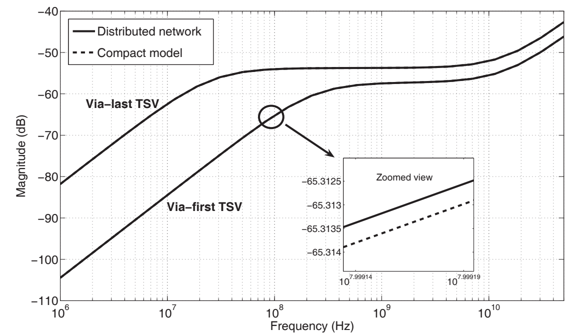

Figure 5: Comparison of the proposed compact π model with high complexity distributed mesh for both via-first and via-last TSVs. The solid line represents noise at the victim node obtained from distributed mesh whereas the dashed line represents noise at the victim node obtained from the compact π model.

- $Y^2_{gnd}(j\omega) = (1/R^2_{gnd}) + j\omega C^2_{gnd} = Y_{22}(j\omega) - Y_{21}(j\omega)$: represents the equivalent substrate admittance between the victim node and ground node.

Note that Y_{11}, Y_{21}, and Y_{12} are obtained by simulating the distributed mesh. Also note that a single RC value is chosen for each admittance since the variation of the resistance and capacitance with frequency is negligible in the frequency range of interest. Specifically, the maximum change is less than 0.1% up to 100 GHz.

The accuracy of the compact model is demonstrated by comparing the transfer function of the compact model with the transfer function of the distributed mesh with significantly higher complexity. Assuming a lightly doped substrate (with 10 Ωcm resistivity and 103.4×10^{-12} F/m absolute permittivity), the two transfer functions are compared in Fig. 5 for both via-first and via-last TSVs. In the distributed model, the dimensions L_{sub}, W_{sub}, and H_{sub} of the unit substrate cell are, respectively, 1 μm, 1 μm, and 1.25 μm. The distance between the TSV and victim node is 10 μm and a single substrate contact is placed between the two ports. The overall length of the substrate is 100 μm. The height of the substrate (determined by the TSV height) is 10 μm for a via-first TSV and 50 μm for a via-last TSV. Alternatively, the width of the substrate (partly determined by the TSV diameter) is 5 μm for a via-first TSV and 12 μm for a via-last TSV. Note that via-last TSVs have greater dimensions as compared to via-first TSVs, significantly affecting the noise at the victim node, as further discussed in Section 5.

Comparison of Complexity: For a via-first TSV, the x and y dimensions of the unit TSV cell are both equal to 4.4 μm ($W + 2t_{ox}$ where $W = 4$ and $t_{ox} = 0.2$), whereas the z dimension is 1 μm. Alternatively, for a via-last TSV, the x and y dimensions of the unit TSV cell are equal to 10.4 μm ($W + 2t_{ox}$ where $W = 10$ and $t_{ox} = 0.2$) and the z dimension is 5 μm. In the distributed model with a via-first TSV, these dimensions produce 48,080 number of circuit elements (resistance, capacitance, and inductance). For a via-last TSV, this number increases to 576,080 due to greater y and z dimensions of the substrate. Alternatively, the compact pi model contains only 11 number of elements for both via-first and via-last TSVs.

Comparison of Accuracy: As illustrated in Fig. 5, noise

Table 1: Fitting coefficients for the function F that approximates the admittances within the compact model (see Fig. 4) for each case. The function F is given by (13).

Cases	Admittances	Fitting coefficients A	B	C	D	E	Average error (%)
Case 1	$R_{sub} = 1000/F$ (kΩ)	27.09	0	0	-0.98	-5.11	6.6
	$C_{sub} = F$ (aF)	326.7	0.41	0.48	-17.26	-67.55	2.8
	$R^1_{gnd} = 1000/F$ (kΩ)	28.31	0	0	-8.14	1.98	1.9
	$C^1_{gnd} = F$ (aF)	301.3	-0.28	0.66	-96.94	30.09	1.6
	$R^2_{gnd} = F$ (kΩ)	45.91	2.30	3.08	-218.3	154.9	9.6
	$C^2_{gnd} = 1000/F$ (aF)	8.05	0.28	0.29	-20.39	12.49	10.4
Case 2	$R_{sub} = 1000/F$ (kΩ)	29.18	0.28	0.38	1.34	-11.78	8.3
	$C_{sub} = F$ (aF)	317.1	2.99	4.24	14.2	-127.6	10.8
	$R^1_{gnd} = 1000/F$ (kΩ)	69.24	-0.046	1.97	-35.05	4.73	0.7
	$C^1_{gnd} = F$ (aF)	758.5	-0.49	21.13	-380.8	51.33	0.7
	$R^2_{gnd} = 1000/F$ (kΩ)	9.50	-0.19	-0.99	-1.95	9.31	1.6
	$C^2_{gnd} = F$ (aF)	106.4	-2.05	-10.99	-20.83	100.7	1.6
Case 3	$R_{sub} = 1000/F$ (kΩ)	27.35	-0.082	0.036	-2.11	-1.12	2.4
	$C_{sub} = F$ (aF)	296.6	-0.89	0.83	-20.78	-13.12	1.9
	$R^1_{gnd} = 1000/F$ (kΩ)	36.16	0.028	0.39	-10.16	1.18	2.4
	$C^1_{gnd} = F$ (aF)	235.6	-1.18	-2.16	-61.86	51.91	6.9
	$R^2_{gnd} = 1000/F$ (kΩ)	11.57	0.11	-0.19	4.43	-5.86	11.6
	$C^2_{gnd} = F$ (aF)	129.1	1.18	-2.22	49.1	-65.23	10.9
Case 4	$R_{sub} = 1000/F$ (kΩ)	24.41	0.13	0.42	1.69	-8.36	8.5
	$C_{sub} = F$ (aF)	265.3	1.40	4.67	17.88	-91.2	7.2
	$R^1_{gnd} = 1000/F$ (kΩ)	117.6	-0.03	0.40	-35.66	3.64	0.3
	$C^1_{gnd} = F$ (aF)	998	0.03	-68.78	37.31	32.11	2.9
	$R^2_{gnd} = 1000/F$ (kΩ)	14.56	-0.01	-0.73	-3.49	5.93	2.4
	$C^2_{gnd} = F$ (aF)	162	-0.13	-8.17	-37.74	64.26	2.5

coupling due to TSVs is accurately estimated by the compact model with negligible error within the frequency range of interest. Note that the noise magnitude at the victim node is higher for via-last TSVs due to higher TSV capacitance and greater substrate dimensions. This difference is more than 20 dB at low frequencies and decreases to approximately 4 dB in the gigahertz range.

The proposed compact model supports the analysis of TSV induced coupling noise. To be able to consider the effect of various design parameters on coupling noise, each RC element within the compact model is expressed as a function of two physical distances, as described in the following section.

4. TSV SAFE ZONE CHARACTERIZATION

To determine TSV safe zone, the dependence of TSV induced noise on design parameters such as distance between TSV and victim node, and the number and location of substrate contacts should be characterized. Two substrate biasing schemes are considered. In the first scheme, as depicted in Fig. 6(a), a single substrate contact is placed between the TSV and victim node. The physical distance between the TSV and victim node is d_1 and the distance between the TSV and substrate contact is d_2. In the second scheme, as depicted in Fig. 6(b), substrate contacts are regularly placed between the TSV and victim node. In this case, d_2 refers to the distance between each substrate contact. The second scenario is considered since substrate contacts can be regularly placed in an automated manner based on latch-up constraints of the technology. These two scenarios are separately investigated for both via-first and via-last TSVs, producing four different cases, as summarized below:

- Case 1: via-first TSV with a single substrate contact between TSV and victim node
- Case 2: via-first TSV with regularly placed substrate contacts between TSV and victim node

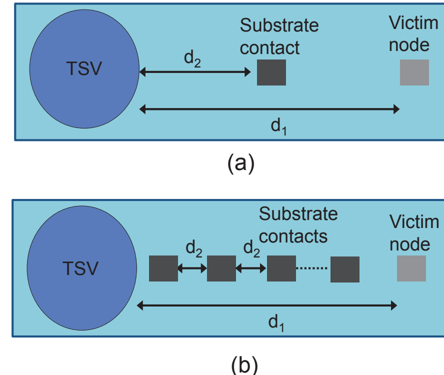

Figure 6: The two substrate biasing schemes used to characterize noise coupling: (a) single substrate contact between a TSV and victim node, (b) regular placement of the substrate contacts between a TSV and victim node.

- Case 3: via-last TSV with a single substrate contact between TSV and victim node
- Case 4: via-last TSV with regularly placed substrate contacts between TSV and victim node

For each case, the $Y(j\omega)$ parameters of the π network are characterized as a function of d_1 and d_2. To evaluate these dependencies, AC analyses of the distributed mesh (based on 3D TLM) described in Section 2 are performed at different d_1 and d_2. The data obtained in this step are used to generate a 3D surface for each resistance and capacitance within $Y_{sub}(j\omega)$, $Y^1_{gnd}(j\omega)$, and $Y^2_{gnd}(j\omega)$. This surface is approximated with a logarithmic function using a 3D least square regression analysis. The logarithmic function F used to approximate the admittances of the π network as a function of the physical distances d_1 and d_2 is

$$F(d_1, d_2) = A + Bd_1 + Cd_2 + D \ln d_2 + E \ln d_1, \quad (13)$$

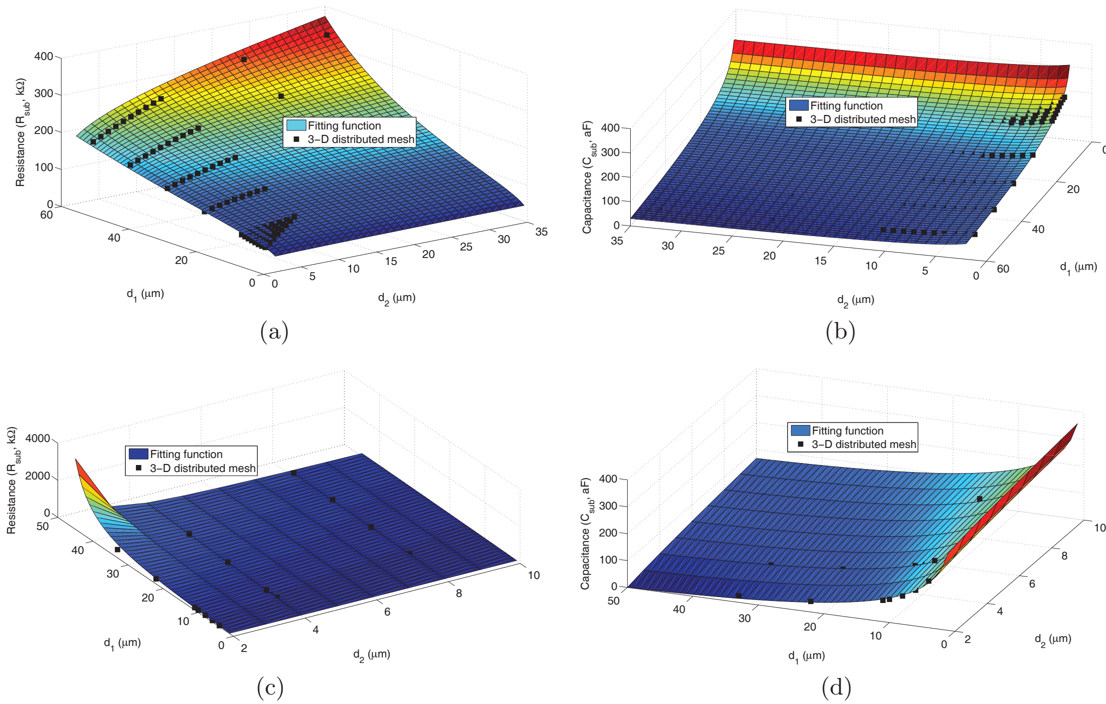

Figure 7: Comparison of the data obtained from the analysis of the distributed mesh with the function F that approximates these data: (a) resistance R_{sub} of the $Y_{sub}(j\omega)$ with a via-first TSV and a single substrate contact (case 1), (b) capacitance C_{sub} of the $Y_{sub}(j\omega)$ with a via-first TSV and a single substrate contact, (c) resistance R_{sub} of the $Y_{sub}(j\omega)$ with a via-last TSV and regularly placed substrate contacts, and (d) capacitance C_{sub} of the $Y_{sub}(j\omega)$ with a via-last TSV and regularly placed substrate contacts.

where A, B, C, D, and E are fitting coefficients. Note that both the resistance (in kilo Ωs) and capacitance (in atto Farads) of each $Y(j\omega)$ within the π network are represented by the function F. Also note that the distances d_1 and d_2 are in μm. Since the π network has three admittances each consisting of a parallel RC circuit, six logarithmic functions are developed for each case, producing a total of 24 functions. The fitting coefficients for each function are listed in Table 1.

As an example, the resistance R_{sub} and capacitance C_{sub} of the $Y_{sub}(j\omega)$ are plotted, respectively, in Figs. 7(a) and 7(b) for a via-first TSV with a single substrate contact (case 1). The same parameters are plotted for a via-last TSV with regularly placed substrate contacts (case 4) in, respectively, Figs. 7(c) and 7(d). The dotted points represent the data obtained from the analysis of the distributed mesh and the surface represents the function F that approximates these data. The procedure is similar for other cases and the RC elements of the remaining admittances ($Y^1_{gnd}(j\omega)$ and $Y^2_{gnd}(j\omega)$) within the compact model. Note that in all cases, d_1 is greater than d_2 since substrate contacts are placed between the TSV and victim node.

The sufficient accuracy of the fitting method is demonstrated by quantifying the average percent error (as compared to the distributed mesh based on 3D TLM) for each resistance and capacitance within the π network. These values are listed in the last column of Table 1. For case 1 and case 3 (a single substrate contact exists between the TSV and victim node), d_1 (distance between TSV and victim node) varies from 4 μm to 55 μm and d_2 (distance between TSV and substrate contact) varies from 2 μm to 33 μm. Alternatively, for case 2 and case 4 (multiple substrate contacts are regularly placed between the TSV and victim node), d_1 varies from 4 μm to 44 μm and d_2 (distance between two substrate contacts) varies from 2 μm to 8 μm. Note that the maximum average error is slightly over 10% for certain resistances and capacitances. This error, however, does not significantly affect the electrical characteristics (and noise estimation at the victim node) since the maximum error occurs at the extreme cases when the resistance is sufficiently large and capacitance is sufficiently small. Also note that the average error over four cases is 4.8%.

The proposed model and the function F can be used to efficiently characterize TSV-to-transistor noise coupling for (1) different design parameters such as the distance between TSV and the victim transistor, number and location of substrate contacts and (2) different TSV fabrication technologies such as via-first and via-last.

5. DESIGN GUIDELINES

Peak-to-peak noise at the victim transistor due to TSV activity is analyzed using (13) and the compact model illustrated in Fig. 4. This noise is depicted in Figs. 8(a) and 8(b) as a function of d_2 when d_1 is constant at 30 μm.

According to Fig. 8(a), where a single substrate contact exists between the TSV and victim node, switching noise is reduced as the substrate contact is placed closer to the victim node as opposed to the TSV. This characteristic is due to TSV height and distributed TSV capacitance to substrate. Thus, a single substrate contact closer to the TSV is not sufficiently effective. Note that based on Fig. 8(a), this characteristic is stronger in via-last TSVs since the height of a via-last TSV is five times greater than a via-first TSV. In traditional 2D circuits, it is typically a physical design deci-

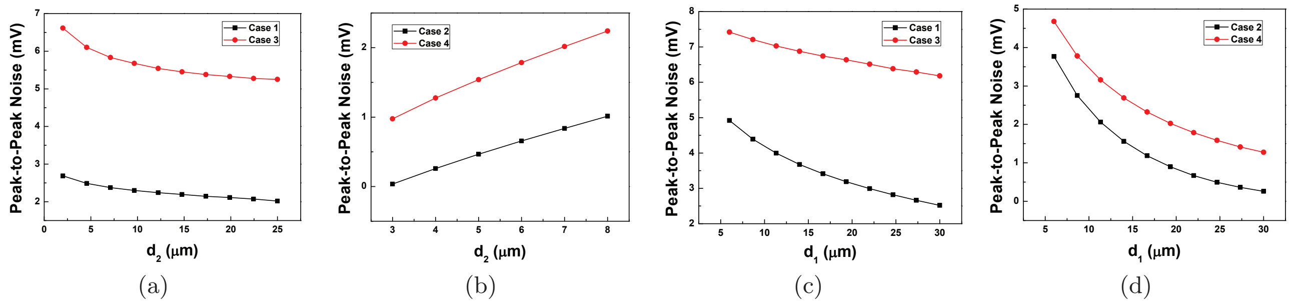

Figure 8: TSV induced switching noise at the victim node: (a) as a function of d_2 at constant d_1 for case 1 and case 3, (b) as a function of d_2 at constant d_1 for case 2 and case 4, (c) as a function of d_1 at constant d_2 for case 1 and case 3, and (d) as a function of d_1 at constant d_2 for case 2 and case 4.

sion to place the substrate contacts (or guard rings) around an aggressor noise source or around a sensitive victim block. In 3D circuits where TSVs are primary source of switching noise, placing the substrate contacts closer to the victim block is more advantageous, as demonstrated in Fig. 8(a).

According to Fig. 8(b), where multiple, regularly placed substrate contacts exist between the TSV and victim node, switching noise is significantly less as compared to Fig. 8(a) and is further reduced as d_2 decreases, *i.e.*, number of substrate contacts increases. Also note that in both figures, switching noise due to via-last TSVs is significantly greater than via-first TSVs since the diameter is larger and height is longer.

Peak-to-peak switching noise at the victim transistor is shown in Figs. 8(c) and 8(d) as a function of d_1 when d_2 is constant at 4 μm. As illustrated in Fig. 8(c), when only a single substrate contact exists, placing the victim transistor farther from the switching TSV is an effective method for via-first TSVs. Alternatively, for via-last TSVs, the noise exhibits low sensitivity to the distance between TSV and victim transistor. This phenomenon is due to longer height (therefore smaller substrate resistances) and larger diameter (therefore larger capacitances) of via-last TSVs.

According to Fig. 8(d), when multiple substrate contacts are regularly placed, increasing the physical distance between the switching TSV and victim transistor is helpful for both via-first and via-last TSVs. In this case, the effective impedance between the TSV and substrate contact becomes significantly lower since the number of substrate contacts increases as d_1 is increased.

6. CONCLUSIONS

TSV-to-transistor noise coupling has been evaluated and quantified in 3D ICs. A compact π model has been proposed to estimate noise at the victim transistor as a function of different substrate biasing schemes (single substrate contact versus multiple, regularly placed substrate contacts) and TSV fabrication methods (via-first versus via-last). A closed-form expression has been developed to approximate each admittance within the π model with a logarithmic function. Both the compact model and the closed-form expression have been validated using a 3D transmission line matrix method with an average error of 4.8%. These expressions and the model have been utilized to better understand the effect of different physical parameters on noise for both via-first and via-last TSVs.

7. REFERENCES

[1] E. Salman and E. G. Friedman, *High Performance Integrated Circuit Design*. McGraw-Hill, 2012.

[2] V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*. Morgan Kaufmann, 2009.

[3] E. Salman, "Noise Coupling Due to Through Silicon Vias (TSVs) in 3-D Integrated Circuits," in *Proc. of the IEEE Int. Symp. on Circuits and Systems*, May 2011, pp. 1411–1414.

[4] N. H. Khan *et al.*, "Through-Silicon Via (TSV)-Induced Noise Characterization and Noise Mitigation Using Coaxial TSVs," in *Proc. of the IEEE Int. Conf. on 3D System Integration*, September 2009, pp. 1–7.

[5] J. Cho *et al.*, "Guard Ring Effect for Through Silicon Via (TSV) Noise Coupling Reduction," in *Proc. of the IEEE CPMT Symposium Japan*, Aug. 2010, pp. 1–4.

[6] P. Saguet, "The 3D Transmission-Line Matrix Method: Theory and Comparison of the Processes," *Int. Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 2, no. 4, pp. 191–201, December 1989.

[7] J. Cho *et al.*, "Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring," *IEEE Trans. on Components, Packaging and Manufacturing Tech.*, vol. 1, no. 2, pp. 220–233, February 2011.

[8] S. Ramaswami *et al.*, "Process Integration Considerations for 300 mm TSV Manufacturing," *IEEE Trans. on Device and Materials Reliability*, vol. 9, no. 4, pp. 524–528, December 2009.

[9] I. Savidis and E. G. Friedman, "Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Trans. on Electron Devices*, vol. 56, no. 9, pp. 1873–1881, September 2009.

[10] J. Kim, J. Cho, and J. Kim, "TSV Modeling and Noise Coupling in 3D IC," in *Proc. of the IEEE Electronic System-Integration Tech. Conf.*, September 2006, pp. 1–6.

[11] J. S. Pak *et al.*, "PDN Impedance Modeling and Analysis of 3D TSV IC by Using Proposed P/G TSV Array Model Based on Separated P/G TSV and Chip-PDN Models," *IEEE Trans. on Components, Packaging and Manufacturing Technology*, vol. 1, no. 2, pp. 208–219, February 2011.