Power Gating Topologies in TSV Based 3D Integrated Circuits

Hailang Wang and Emre Salman
Department of Electrical and Computer Engineering
Stony Brook University
Stony Brook, New York 11794
{haiwang,emre}@ece.sunysb.edu

ABSTRACT

Two topologies are proposed at the physical level to achieve reliable power gating in through silicon via (TSV) based three-dimensional (3D) integrated circuits (ICs). The proposed lumped and distributed power gating topologies address the unique differences among distinct TSV fabrication methods such as via-first, via-middle, and via-last, while achieving, on average, 85% reduction in the leakage power. Related tradeoffs among power supply noise, power gating noise, physical area, and turn-on time are also investigated.

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]: [Miscellaneous]

Keywords

Power gating; TSV; Noise; 3D IC

1. INTRODUCTION

Through silicon via (TSV) based three-dimensional (3D) integration has emerged as a promising technology for both high performance and low power integrated circuits (ICs). Reliable power gating (both at the plane and block levels) is critical for low power 3D systems-on-chip that have long standby operating modes. Idle planes and idle blocks within a plane should be turned off to minimize leakage current while satisfying specific constraints such as power supply noise, power gating noise, area, and turn-on time.

Sleep transistors (with high threshold voltage) are used to achieve power gating. In high performance ICs with multiple (>8) metal layers, the power supply voltage is initially transmitted from the highest metal layer to the lowest metal layer through a stack of vias, reaching the sleep transistor. If the sleep transistor is on, supply voltage propagates back to the metal layers of the semi-global power grid, finally reaching the local power network that supplies current to a specific circuit block. The sleep transistors and the stack of vias introduce additional impedance to a power distribution network.

In 3D ICs, the power distribution networks for each plane are interconnected with the TSVs. The connection scheme depends partly upon the particular TSV fabrication technique [1]. Referring to Fig. 1, in via-first and via-middle technologies, the TSVs typically connect the lowest metal layer of a plane with the highest metal layer of the previous plane. Alternatively, in a via-last technology, the TSVs typically connect the highest metal layers in both planes, thereby causing signal routing blockages. These differences in the connection schemes are important in developing reliable 3D power gating topologies.

In this paper, two power gating topologies are proposed for TSV based 3D ICs while considering the distinct characteristics of via-first, via-middle, and via-last TSVs. The effect of the size of the sleep transistors and number of TSVs on power supply noise, power gating noise, and turn-on time is investigated for both topologies.

GLSVLSI'13, May 2–3, 2013, Paris, France.
ACM 978-1-4503-1902-7/13/05.

2. APPROACH

While fine-grained power gating is similar to traditional 2D power gating methods, plane- and block-level power gating in 3D ICs exhibits different characteristics due to the TSVs. Considering the coarse grain power gating problem, two power gating topologies are proposed based on, respectively, lumped and distributed placement of sleep transistors, as illustrated in Fig. 1 for a three plane 3D IC.

In the lumped power gating topology, as proposed for via-first and via-middle TSVs, all of the sleep transistors are fabricated on the top-most plane. As mentioned earlier, via-first/middle TSVs connect the lowest metal layer of a plane with the highest metal layer of an adjacent plane. Thus, sleep transistors are placed between the lowest metal layer of the top-most plane and TSVs which also land on this layer, as depicted in Fig. 1(a). Two advantages of the lumped topology are (1) maintaining all of the control signals for sleep transistors within a single plane and (2) ensuring higher voltage at the source terminal of the sleep transistors during normal operation.

Alternatively, in the distributed power gating topology, sleep transistors are distributed on each plane. The TSVs are constantly connected to the power supply. Thus, in the distributed scheme, additional stack of vias that transmits the virtual supply voltage (after the sleep transistor) back to the TSV is avoided, thereby enhancing the power supply noise during normal operation.

Another issue related with the power gating topologies in 3D ICs is the sizing of the sleep transistor and the number of the TSVs. The sensitivity of the power supply noise varies depending not only on TSV type, power gating topology, but also on specific design parameters such as the effective width of the sleep transistor and number of TSVs. The

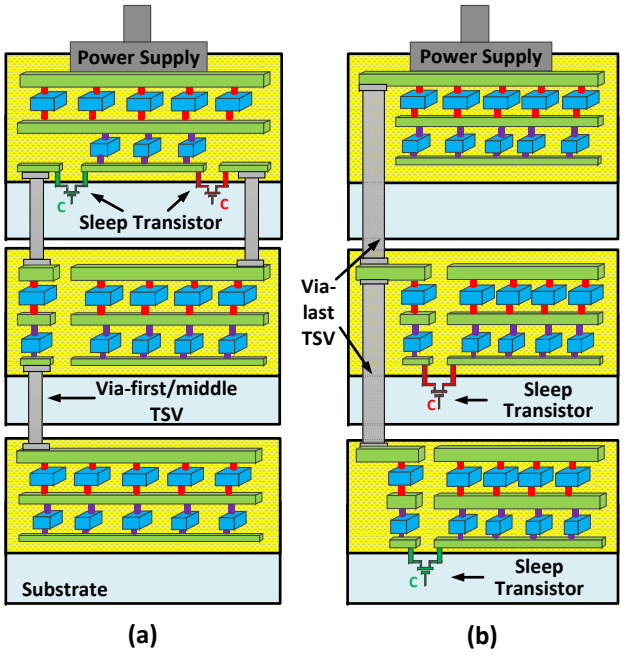

Figure 1: Physical representations of the proposed power gating topologies: (a) lumped topology for via-first and via-middle TSVs, and (b) distributed topology for via-last TSVs.

additional physical area occupied by the sleep transistors and TSVs is an important concern in low power, low cost 3D ICs. A closed-form expression is therefore developed to allocate available area to sleep transistors and TSVs, which minimizes power supply noise during normal operation.

3. PRIMARY RESULTS AND CONCLUSIONS

To evaluate the proposed power gating topologies, simulations are performed in HSPICE using an industrial 65 nm CMOS technology with a nominal supply voltage of 1 V. Electrical models are developed to represent the three plane 3D ICs, as illustrated in Fig. 1.

Distributed and lumped power gating topologies are analyzed for both via-middle and via-last TSVs. A critical step to model the power distribution network is extracting the impedance of the power grid on each plane. The number of interdigitated power/ground lines is obtained from the pitch and width of the lines. The field solver FastHenry is used to extract the effective impedance of the power distribution grid. The package level parasitic impedances are extracted from experimental measurement results [2]. The width of sleep transistor and number of TSVs are varied to evaluate the effect of these parameters on several criteria related to power integrity such as power supply noise, power gating noise, and turn-on time.

To analyze power supply noise, a current switching profile is used during the normal operating of the logic circuit. The worst case power supply noise at the farthest plane is measured. For the analysis of the power gating noise and turn-on time, step voltages are applied to the sleep transistors. The analysis results are qualitatively summarized in Table 1.

Table 1: Qualitative Analysis Results

	Via-middle		Via-last	
	Dist.	Lumped	Dist.	Lumped
Supply noise	Large	Small	Small	Large
Gating noise	Large	Small	Large	Small
Turn-on time	Long	Short	Short	Long

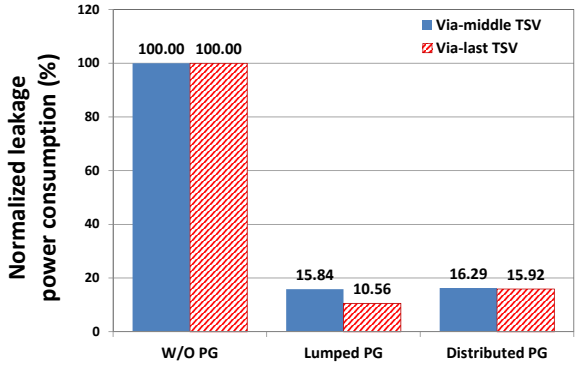

Figure 2: Normalized leakage power consumption achieved by the proposed power gating topologies.

According to Table 1, lumped topology is generally preferable for via-middle TSVs, whereas a distributed topology is preferred for via-last TSVs. The reason is the additional resistance due to stack of vias if lumped topology is used for via-last TSVs and distributed topology is used for via-middle TSVs, as mentioned before. Distributed topology exhibits slightly more power gating noise than the lumped topology for both via-middle and via-last TSVs. This characteristic is because when a plane is turned on, higher current is provided by the neighboring planes in a distributed topology since the impedance between the planes is relatively smaller. Thus, the neighboring planes exhibit slightly more power gating noise in the distributed topology.

The leakage power reduction achieved by the proposed two power gating topologies is also evaluated, as shown in Fig. 2. The leakage power is normalized based on the leakage power consumption of the 3D IC without power gating. For via-middle TSVs, the lumped and distributed power gating topologies can save, respectively, 84.16% and 83.71% leakage power. Alternatively, for via-last TSVs, the leakage power is reduced, respectively, by 89.44% and 84.08%, demonstrating the efficacy of the proposed power gating topologies.

4. REFERENCES

[1] S. M. Satheesh and E. Salman, "Power Distribution in TSV Based 3D Processor-Memory Stacks," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 4, pp. 692–703, December 2012.

[2] M. Gupta, J. Oatley, R. Joseph, G.-Y. Wei, and D. Brooks, "Understanding Voltage Variations in Chip Multiprocessors using a Distributed Power-Delivery Network," in *Proceedings of The Design, Automation Test in Europe Conference Exhibition*, April 2007, pp. 1–6.