

Design And Verification of A PLL Based Clock And Data Recovery Circuit

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Abstract— In this paper, the design and verification of a clock and data recovery circuit (CDR) is presented. The circuit is designed and verified at 90-nm digital CMOS platform of ST Microelectronics and complies with the requirements of Bellcore GR-253 SONET OC-12 standard. The CDR system consists of a Phase Locked Loop (PLL) based dual loop architecture which includes a phase detector, a phase-frequency detector, two charge pumps, a low-pass filter, a voltage controlled oscillator (VCO) and a feedback divider. Due to the use of dual loop architecture, a lock detect circuitry is required. Also, a power down circuitry is designed for determining which of the loops to operate under desired conditions. The final circuit meets and exceeds SONET OC-12 jitter specifications. It can also work at 1.2 Gbps as the highest frequency. At lock condition, it consumes only 3.2 mW at 622 Mbps. The mask layout and verification of the circuit are completed and ready for fabrication.

Index Terms—MMIC, RFIC, analog integrated circuits, CDR, PLL

I. INTRODUCTION

The audio and video transport on communication networks is highly growing in recent years making higher performance serial data transmission techniques very desirable [1,2]. Since the copper links are not so appropriate for increasing data rates, the transmission medium is being converted to fiber links [3,4]. This means that low power, low cost physical layer elements of optical fiber links are very important in terms of better performance. One result is the use of highly integrated multi channel fiber optic transceivers to decrease the overall cost. The main issue in the implementation of the large numbers of channels (>64) on the same chip is the individual power consumption of one channel, because it will basically be multiplied by the total number of channels in the chip.

In this paper, a very low power SONET OC-12 based clock and data recovery circuit, one of the crucial elements of the

receiver side, is described. Its function is basically to extract the clock signal from the incoming distorted data stream and to regenerate clean data at the output while tracking the possible phase deviation at the input data. Although it introduces some design difficulties due to voltage headroom problems [5], 90nm CMOS technology with a V_{DD} of 1V is preferred to provide minimum power consumption. Also, low leakage (high V_i) transistors were used where possible which even aggravates the headroom problem. To overcome this difficulty and limit the power consumption, all blocks were designed with minimal simplicity while satisfying SONET OC-12 jitter specifications.

Matlab analysis was performed to determine loop dynamics, and the system was coarsely verified by means of a Simulink model before starting the transistor level design. The top level architecture of the CDR is described in section II. Section III explains the building blocks of the system. Simulation results are given in section IV. Section V is the conclusion of the paper, summarizing the simulation results.

II. TOP LEVEL CDR ARCHITECTURE

As shown in Figure 1, the CDR system consists of a Phase Locked Loop (PLL) based dual loop architecture which includes a phase detector, a phase-frequency detector, two charge pumps, a low-pass filter, a voltage controlled oscillator (VCO) and a feedback divider.

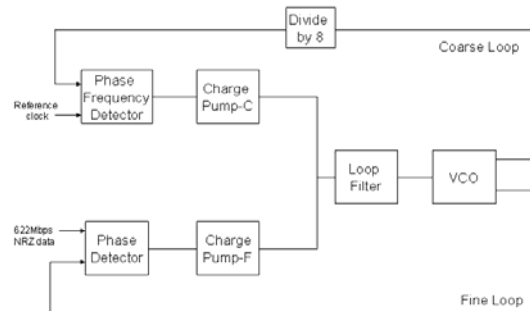


Fig. 1. CDR circuit top level architecture

Since SONET OC-12 jitter transfer specification requires a loop bandwidth of smaller than 500 kHz, the capture range of the PLL is limited. This problem is solved by using dual loop architecture. The two loops can be defined to be the coarse

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loop and the fine loop depending on their functionality. Following power up, only the coarse loop operates and the system functions as a frequency synthesizer to align the divided VCO clock with the reference clock of 78 MHz. After the lock is achieved, coarse loop stops and fine loop aligns the rising edge of the recovered clock to the middle of the data eye which is 622 Mbps NRZ (non return to zero) random data. Both loops are identical apart from the fact that phase/frequency detector of the coarse loop is replaced with Hogge phase detector in the fine loop. In terms of loop dynamics, the effect of feedback divider at the coarse loop is compensated by the ratio of the charge pump currents of the loops. The charge pump current of the coarse loop is approximately 8 times of the fine loop charge pump current. This enables coarse loop to tune the oscillation frequency in bigger steps and fine loop to tune in smaller steps. A second order passive low-pass filter is implemented as the loop filter where an off chip capacitor is needed due to its large value. The loop parameters and stability analysis results are represented in Table 1 and 2, respectively.

Due to the use of dual loop architecture, a lock detect circuitry is required to disable the coarse loop and enable the fine loop when the lock condition is achieved. The lock detector circuit asserts lock signal when a reasonable phase difference between reference clock and divided VCO clock is obtained. It means that a proper frequency alignment is already achieved. Hence, coarse loop is turned off, no longer affects control voltage, and fine loop is turned on in order to provide exact phase alignment such that the rising edge of the recovered clock is properly centered within the data bit interval.

A power down circuitry is implemented determining which of the loops to operate under desired conditions. It processes a global power down signal, lock signal and data loss signal to generate conditions that start/stop the coarse and fine loop. No loop operates when the global power down is active and there is no possible condition for both of them to operate at the same time.

TABLE I
LOOP PARAMETERS

Loop parameter	Value	Unit
K_{VCO} (VCO gain)	2.8 / 2	GHz/V
$I_{CP(\text{coarse})}$ (Coarse loop charge pump current)	40	μA
$I_{CP(\text{fine})}$ (Fine loop charge pump current)	5	μA
R (Loop filter resistance)	308	ohm
C_1 (Loop filter capacitor)	144.6	nF
C_2 (Loop filter capacitor)	723	pF
N (Divide Ratio of coarse loop)	8	--

TABLE II
STABILITY ANALYSIS RESULTS

Parameter	Value	Unit
ζ (Damping Ratio)	4.9	--
PM (Phase Margin)	65.8	$^\circ$
f_n (natural frequency)	35	kHz.
f_{-3dB} (Jitter transfer bandwidth)	479	kHz.
JP (Jitter peaking)	0.088	dB
JT (Jitter tolerance, 3 dB frequency)	236	kHz.

III. BUILDING BLOCKS

In general, “expensive” analog circuitry is avoided because of reduced voltage headroom. All the blocks except VCO are designed single ended not to increase total area and power consumption. Below is the summary of these structures of building blocks.

A. Phase/Frequency Detector (PFD) and Hogge Phase Detector

The PFD for the coarse loop is designed in a conventional way using two D-type flip-flops, one NAND gate. Also, two multiplexers at the output have been added to ensure that the circuit generates either an “up” pulse or a “down” pulse and both of them can not be at logic high at the same time. The designed PFD has a dead zone of around 90 ps.

The Hogge phase detector [6] of the fine loop compares the VCO clock with the incoming data stream and outputs two signals; “error” and “reference” that carry information about the alignment of VCO clock and data. The width of the reference pulses are always the same, but the width of the error pulses change according to the alignment of VCO clock. Hogge phase detector should be able to detect small phase differences accurately, because it directly affects the overall dead zone of the CDR and the static phase offset after lock. The set up and hold times of the flip flops are minimized for the PD to detect small differences.

B. Charge Pumps

A charge pump is consisted of two switched current sources that charge or discharge the loop filter according to its inputs. Figure 2 shows the conceptual implementation of continuous current paths in the charge pump. The idea is to have a continuous flowing current and to change only its direction when required rather than regenerating it. This method reduces the possible current peaking that occurs during the transitions. Also a unity gain amplifier is used to prevent charge sharing [7].

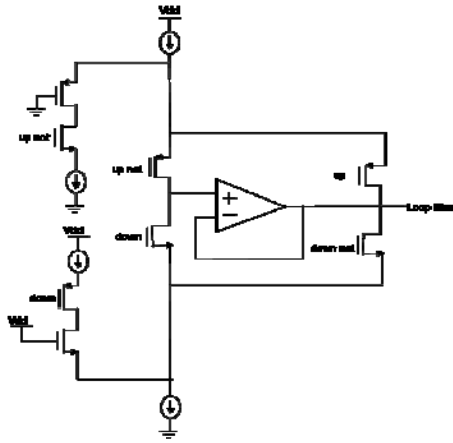


Fig. 2. Conceptual diagram of charge pump circuit

C. Loop Filter

It is a 2nd order passive loop filter with one external capacitance (144.6nF). Since satisfying jitter peaking constraint requires a large capacitor, an external capacitor is inevitable. The other capacitor (723pF) is implemented as MOS-Cap which approximately occupies an area of 50000 μm^2 . Since the depletion region in the NMOS transistor will not exist below the threshold value, a MOS-Cap will accurately act as a capacitor only when its gate voltage exceeds the threshold voltage. To increase the proper operation voltage range of the MOS-Cap, a low V_t transistor was used.

D. Voltage Controlled Oscillator (VCO)

VCO, which is common for the two loops, is a four stage ring oscillator designed differentially to provide better power supply noise rejection. The delay cell, described in [8], is implemented since it is suitable for low voltage operation and outputs rail-to-rail signal, therefore eliminating the need for a level shifter. The cross coupled transistors decrease the rise and fall time of the signal, reducing the jitter generation.

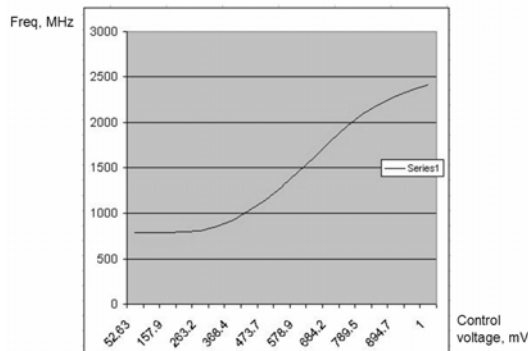


Fig. 3. VCO characteristics

Figure 3 shows the characteristic of the VCO. Its gain must be large enough to guarantee the linear operation for all possible process and temperature variations of the technology. In 90nm CMOS technology, it requires a center frequency of 1.22 GHz with a minimum gain of 2.8 GHz/V, hence it runs at

twice the operating data rate and the frequency is divided by 2 at the output of the VCO. This division also solves the duty cycle problem of the VCO. The power consumed in the VCO together with its buffer circuitry is around 500 μW in typical case. The simulation results representing eye-diagram shows a maximum jitter generation of 9psec.

E. Frequency Divider

CMOS D-type flip-flop cells are used to generate feedback dividers. It can be programmed so that the operating frequency of the CDR can be selected between 155 Mbps, 622 Mbps, and 1.2 Gbps. Although the circuit can correctly satisfy lock condition at all these three frequencies, the jitter transfer and jitter generation specifications are optimum for 622 Mbps.

F. Lock Detector

The use of dual loop architecture requires a circuitry that detects the condition of lock in order to disable the coarse loop and enable the fine loop when the lock condition is achieved. When coarse loop is locked, that is the divided VCO clock frequency and reference clock frequency are almost equal, the lock signal is asserted low. The circuit requires a phase difference of around 350 psec between the reference clock and the divided VCO clock to make sure that the loop is locked. Figure 4 shows the conceptual diagram of analog lock detector circuit.

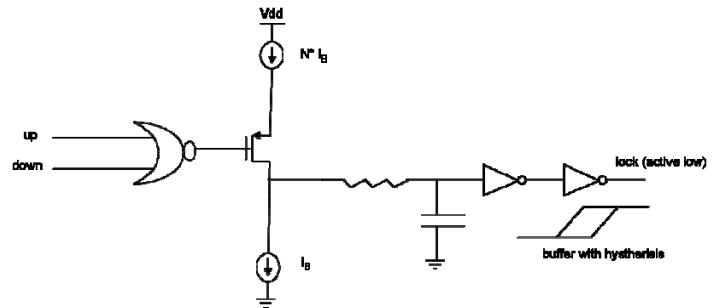


Fig. 4. Conceptual diagram of lock detector circuit

IV. SIMULATION RESULTS

All simulations are done using CADENCE Spectre simulation tool. Figure 5 shows the overall variation of the control voltage (with an initial voltage value) and the assertion of lock signal. The control voltage gradually decreases to slow down the clock signal, which shows that in the simulation clock is advanced with respect to the middle of the data bit period.

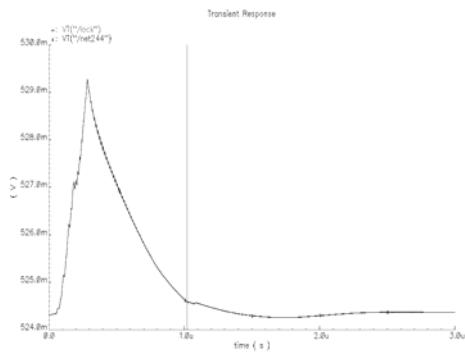


Fig. 5. Overall variation of control voltage and the assertion of lock signal

At lock, the rising edge of clock is aligned to the middle of the data bit period with only 20 psec. of phase offset. The offset is a direct result of mismatches in the circuit and inevitable. Figure 6 shows the simulated eye diagram of the recovered clock after lock. The generated jitter is around 1 psec. which is lower than the individual fine loop analysis. This is due to the self correcting capability of the CDR circuit and the analysis was made after lock was achieved.

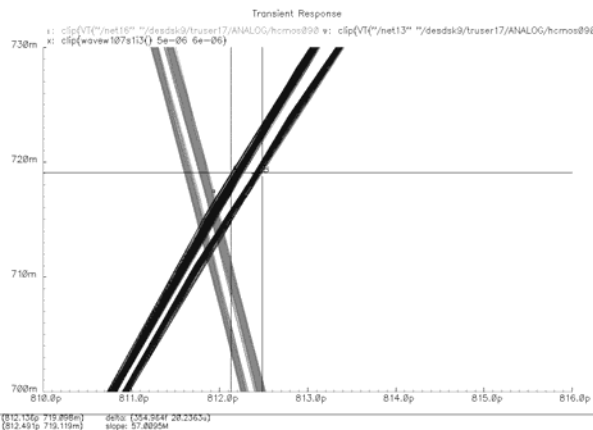


Fig. 6. Eye diagram of the recovered clock after lock showing jitter generation

V. CONCLUSIONS

A very low power CDR circuit was designed in 90-nm digital CMOS technology for multi-channel fiber-optic transceivers of SONET OC-12 applications. After lock, the circuit consumes an average power of only 3.2 mW at 622 Mbps. In terms of operating frequency, it can be programmed to comply with both OC-3 and OC-12 standards. It can also work at 1.2 Gbps as the highest frequency. There is a single supply of 1 V. The circuit has one external loop filter capacitance to satisfy jitter peaking requirement. The simulation results show that the maximum jitter peaking is 0.088 dB and the loop bandwidth of the loop is 475 kHz both of which meet and exceed the jitter transfer requirements of SONET OC-12. The generated jitter in the CDR does not exceed 1psec. corresponding to only $0.00063UI_{p-p}$. Figure 7 is the top level layout view of the overall circuit with the

dimensions of $408\mu\text{m} \times 322\mu\text{m}$. The layout is consistent with analog layout design rules and some special attention was given to the compactness since the interconnect capacitances have a considerable effect on the behavior of the circuit in deep sub-micron technologies.

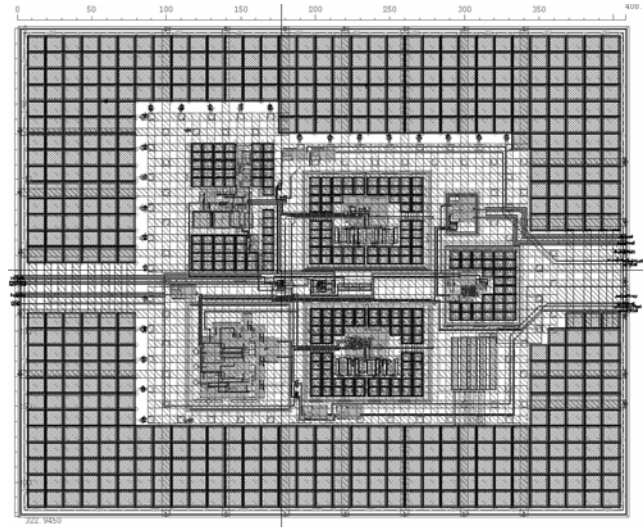


Fig. 7. Top level layout view of the overall circuit

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