Fully Integrated Hybrid Voltage Regulator for Low Voltage Applications

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Abstract of the Thesis

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A novel hybrid regulator topology is proposed to alleviate the weaknesses of existing hybrid topologies. Contrary to the dominant existing practice, a switched-capacitor converter and a resistorless LDO operate in a parallel fashion to supply current and regulate the output voltage. The proposed topology targets a fully integrated regulator without using any inductors and resistors. The primary emphasis is on maximizing power efficiency while maintaining sufficient regulation capability (with ripple voltage less than 10% of the output voltage) and power density. The first implementation of the proposed topology operates in a single frequency mode. Simulation results in 45 nm technology demonstrate a power efficiency of approximately 85% at 100 mA load current with an input and output voltage of, respectively, 1.15 V and 0.5 V. The worst case transient response time is under 20

ns when the load current varies from 65 mA to 130 mA. The worst case ripple is 22 mV while achieving a power density of 0.5 W/mm^2. This single-frequency hybrid voltage regulator is useful (due to its fast and continuous response and high power efficiency) when the output load current is relatively constant at a certain nominal value. However, the performance is degraded when the load current varies significantly beyond the nominal current since the current provided by switched-capacitor converter is constant. The second implementation of the proposed hybrid regulator topology partially alleviates this issue by employing two different frequencies depending on the load current. This design is also implemented in 45 nm technology. It is demonstrated that the power efficiency is maintained within 60% to 80% even though the load current varies by more than 100 mA. The power density remains the same (0.5 W/mm^2). The simulation results of the proposed topology are highly competitive with recent work on integrated voltage regulators.

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Based on the precious things that I learned from them, I hope I will be able to contribute to the society in the future. I would like to express my gratitude to them again.

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I am still in the course of learning. I always dream of a better day than the day before.

Chapter 1

Introduction

The significance of on-chip voltage conversion and regulation has increased in the past decade due to various reasons such as power management within multi-core ICs, multi-voltage designs, dynamic voltage frequency scaling, power integrity, and near-threshold operation [1–4]. For example, Intel has developed a fully integrated voltage regulator (FIVR) for the Haswell microarchitecture, allowing dynamically managed multiple power domains [5].

Near-threshold computing has also received significant attention due to enhanced energy efficiency, particularly for mobile SoCs [6]. Highly parallelized architectures based on near-threshold operation have been proposed as a possible solution to dark silicon [7]. Developing an integrated voltage regulator module with application to near-threshold operation is challenging due to low output voltages in the range of 0.5 V. The regulator should simultaneously satisfy high power

efficiency and power density (to minimize area overhead). Furthermore, the output ripple should be minimized since near-threshold circuits are highly sensitive to power supply variations (due to near-exponential dependence).

Linear low-dropout (LDO) regulators have been commonly used due to low cost and area efficiency. Unfortunately, LDO regulators suffer from low power efficiency (less than 60% in the majority of the cases) [8]. This issue is exacerbated for higher conversion ratios as needed in near-threshold computing since the output voltage is in the range of 0.5 V. Alternatively, switched-capacitor DC-DC converters enhance power efficiency, but typically have poor regulation capability, causing higher ripple voltage and long transient response time [1]. This limitation is critical for near-threshold operation due to high sensitivity to supply voltage. Finally, switching buck converters can achieve sufficiently high power efficiency and sufficient regulation capability, but require high-quality inductors (typically more than one due to multi-phase operation), significantly increasing the overall cost.

In existing approaches, a DC-DC switching converter is combined in series with an LDO, as shown in Fig. 1.1(a) [9, 10]. The switched-capacitor circuit functions as a converter without any regulation capability whereas the LDO regulates the output voltage without any conversion. Thus, the circuit enhances power efficiency since LDO works with a near-unity voltage conversion ratio. Regulation is also enhanced

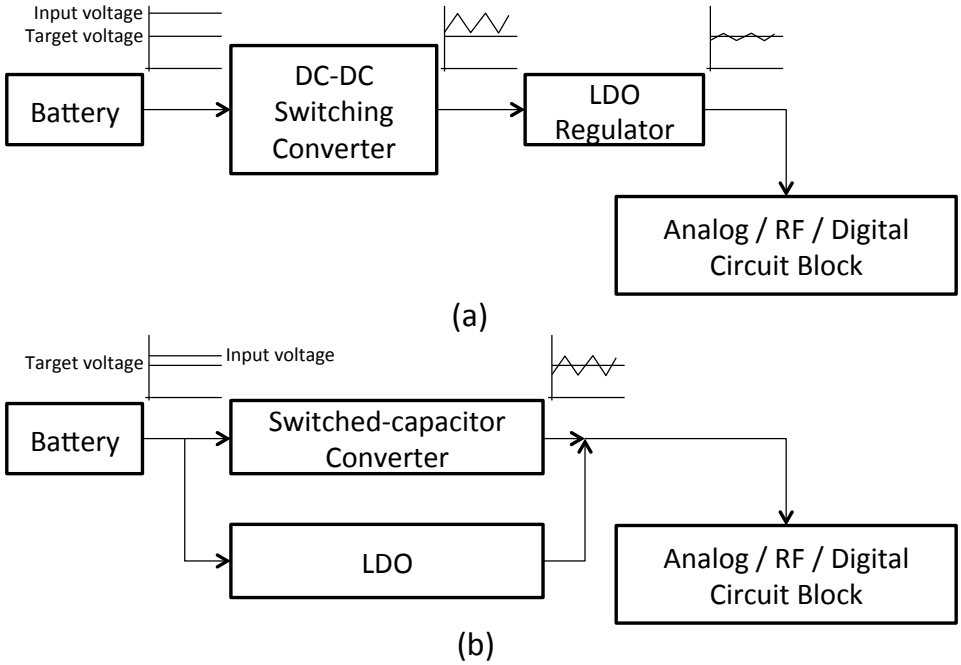

Figure 1.1: Conceptual block diagram of (a) a conventional hybrid regulator, (b) proposed hybrid regulator.

due to an LDO with fast transient response at the output. Feed-forward ripple cancellation has also been proposed to further improve the regulation process [9]. This topology, however, suffers in near-threshold operation with large output current and low output voltage due to three reasons:

- Power transistor of the LDO suffers from low $|V_{GS}|$ since the voltage conversion is achieved by the previous stage (switched-capacitor converter). This low input voltage makes it challenging to supply high current at the output.

- At high output current, the voltage drop across the power transistor (within an

LDO) becomes nonnegligible, requiring a higher input voltage at the LDO. Higher input voltage, however, degrades the power efficiency.

- The maximum output load current cannot be larger than the current supplied by the switched-capacitor converter due to the series connection. Thus, the DC-DC switching converter needs to be optimized for the maximum load current rather than the nominal load current.

These limitations are exacerbated and the power efficiency is further degraded with reduced output voltages, as in near-threshold computing. Thus, a new hybrid topology is proposed in this thesis where the switched-capacitor converter and LDO operate in a parallel fashion, as conceptually illustrated in Fig. 1.1(b). Two implementations are developed to ensure proper operation at low output voltages and outperform existing regulators. The first implementation operates at a single switching frequency of 482 MHz. This implementation achieves approximately 85% power efficiency while supplying 100 mA nominal output current at 0.5 V with a maximum ripple voltage of 22 mV. The second, enhanced implementation employs coarse frequency modulation depending upon the magnitude of the load current. The frequency modulation allows to vary the nominal output current (provided by the switched-capacitor converter) of the regulator. The second implementation has two power efficiency peaks, both higher than 80%. The first peak occurs

when the load is 30 mA at switching frequency of 100 MHz whereas the second peak occurs when the load is 80 mA at switching frequency of 400 MHz.

The rest of the thesis is organized as follows. The first implementation of the proposed hybrid voltage regulator and related simulation results are presented in Chapter 2. The improved version of the proposed topology with coarse frequency modulation and related simulation results are described in Chapter 3. Finally, conclusions and future works are discussed in Chapter 4.

Chapter 2

Proposed Topology

2.1 Proposed Hybrid Regulator

A simplified circuit schematic of the proposed hybrid regulator is shown in Fig. 2.1 [11]. The switched-capacitor converter and LDO operate in a parallel fashion where the source node of the power transistor within the LDO is connected to the primary DC input voltage V_{in}. Thus, this topology does not suffer from the aforementioned limitations since LDO has a relatively larger input voltage. The switched-capacitor circuit provides the nominal output current while converting the input voltage from 1.15 V to 0.5 V. At the nominal load current, LDO is turned off. Any variation at the output voltage is directly sensed by the error amplifier of the LDO and output voltage is regulated with a fast transient response.

Some of the important characteristics of the proposed topology are: 1) no resistors are used within the LDO to minimize power loss, 2) a static current minimization technique is developed to maximize power efficiency, 3) since the output voltage is directly sensed by the error amplifier, a small gain-bandwidth product is adopted, thereby preventing the output ripple from being amplified. These characteristics are described in the following subsections.

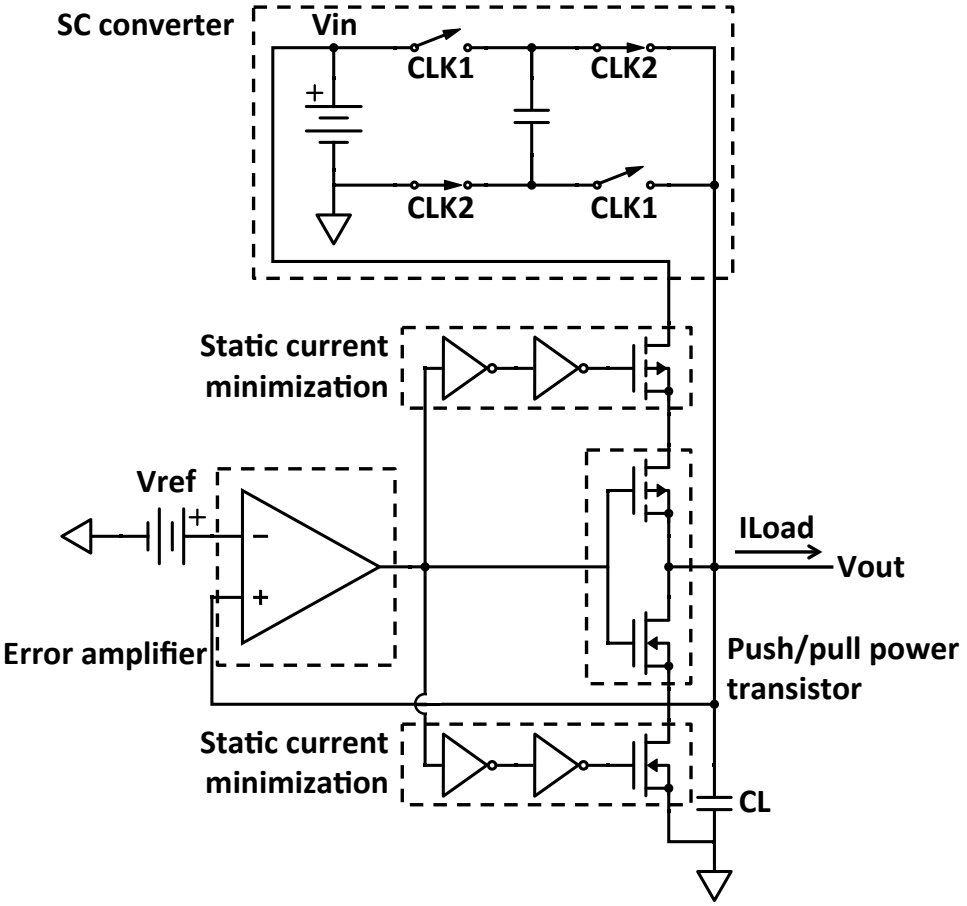

Figure 2.1: Proposed hybrid regulator consisting of an LDO (push/pull power transistors, error amplifier, and static current minimization) and switched-capacitor converter.

2.1.1 Switched-Capacitor DC-DC Converter

A switched-capacitor converter consists of several switches and capacitors to achieve voltage conversion. The topology shown in Fig. 2.1 achieves a conversion ratio of two, as required in this study. According to [12], the overall power loss can be expressed by

$$P_{loss} = P_{C_{fly}} + P_{R_{sw}} + P_{bott-cap} + P_{gate-cap}, \tag{2.1}$$

W_{sw}/L_{sw}	43×25 μm/50 nm
C_{fly}	1.5 nF
C_L	1.5 nF
Switching frequency	482 MHz

Table 2.1: Primary parameters of the switched-capacitor converter.

where $P_{C_{fly}}$, $P_{R_{sw}}$, $P_{bott-cap}$, and $P_{gate-cap}$ refer, respectively, to power loss due to flying capacitor, switch resistance, parasitic capacitance of flying capacitor, and that of the switches. $P_{C_{fly}}$ and $P_{R_{sw}}$ are

$$P_{R_{sw}} \propto I_L^2 \frac{R_{on}}{W_{sw}}, \quad P_{C_{fly}} \propto I_L^2 \frac{1}{C_{fly} f_{sw}}, \tag{2.2}$$

where I_L is the load current, R_{on} is the on-resistance of a single switch, W_{sw} is the width of a single switch, C_{fly} is the flying capacitance, and f_{sw} is the switching frequency. The shunt power loss due to fully-integrated flying capacitor $P_{bott-cap}$ and gate capacitance of the switches $P_{gate-cap}$ are

$$P_{bott-cap} \propto V_o^2 C_{bott} f_{sw}, \;\; P_{gate-cap} \propto V_{sw}^2 C_{gate} f_{sw}, \tag{2.3}$$

where C_{bott} is the sum of the parasitic capacitance from the top and bottom plates of the flying capacitor, V_{sw} is the clock voltage swing, and C_{gate} is the gate capacitance of the switches. Following these expressions, the switch size and flying capacitor are determined to maximize power efficiency [12, 13]. These parameters are listed in Table 2.1.

2.1.2 Proposed Resistorless LDO

Contrary to conventional LDOs, the proposed LDO does not contain any resistors to maximize power efficiency, as illustrated in Fig. 2.1. Instead, a PMOS push power transistor provides the additional current to the load whereas an NMOS pull

transistor reduces the output voltage. These power transistors are controlled by the output of the error amplifier. The error amplifier directly senses the output voltage and adjusts its output based on the difference between the reference voltage and output voltage. Two important design characteristics are the error amplifier and the static current minimization technique, as described in the following subsections.

2.1.2.1 Optimization of the Error Amplifier

In conventional LDOs, the output frequency spectrum is determined solely by the error amplifier within the LDO. Alternatively, in the proposed regulator, the high frequency components of the output frequency spectrum, as depicted in Fig. 2.2, are dominantly determined by the switched-capacitor converter since it operates in parallel with the LDO. As listed in Table 2.1, the switching frequency is 482 MHz. According to Fig. 2.2, the output voltage has a strong frequency component at this switching frequency, demonstrating the effect of switched-capacitor on the frequency spectrum. Thus, the ripple at the output voltage is primarily determined by the switched-capacitor. This behavior is important since the error amplifier directly senses the output voltage in the proposed approach. To prevent the error amplifier from amplifying output ripple, the gain-bandwidth product should be smaller than the switching frequency of the switched-capacitor circuit. Note, however, that a sufficiently small gain-bandwidth product slows down the circuit, increasing the response time. Considering this tradeoff, the gain-bandwidth product is determined as approximately 350 MHz.

2.1.2.2 Static Current Minimization

As opposed to conventional LDOs with single PMOS power transistor, the proposed LDO consists of both PMOS and NMOS power transistors to be able to increase

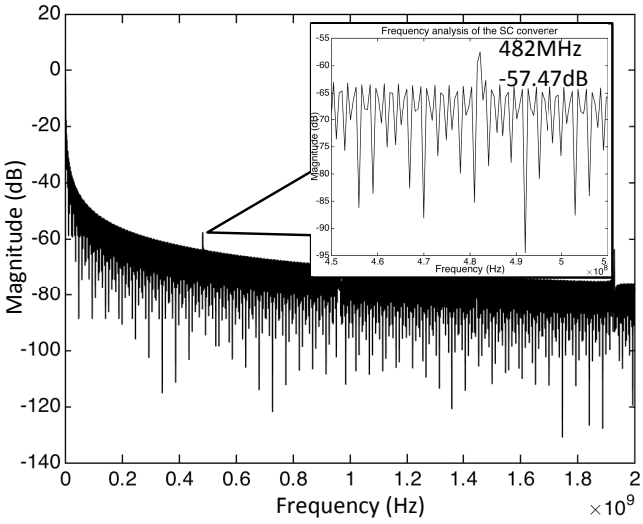

Figure 2.2: Frequency spectrum of the output voltage with 100 mA current.

and decrease the output voltage during regulation. Thus, according to the error amplifier output, both power transistors can be on, dissipating significant static current. This behavior should be prevented to maximize power efficiency. For this reason, a buffer with a different switching voltage is added before each power transistor, as illustrated in Fig. 2.1. The DC voltage characteristics of these buffers are shown in Fig. 2.3. As illustrated in this figure, the buffer preceding the PMOS power transistor has a much smaller switching voltage than the buffer preceding the NMOS power transistor. This difference in the switching voltage ensures that 1) either only PMOS power transistor is on, or 2) only NMOS power transistor is on, or 3) both power transistors are off. The difference in the switching voltages is determined to ensure that the situation when both transistors are on is avoided, thereby preventing the static current.

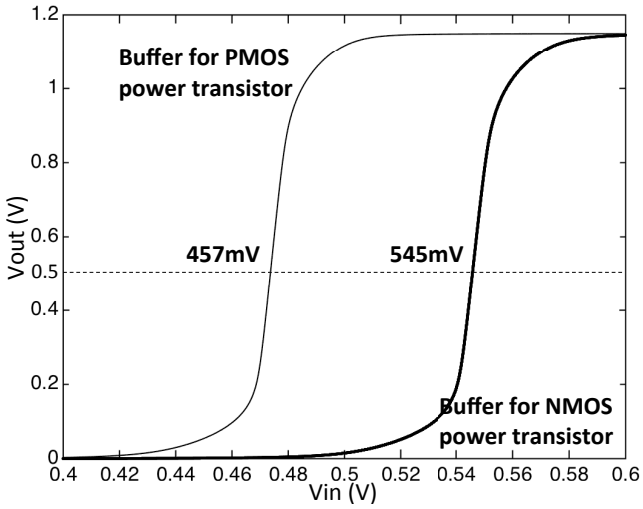

Figure 2.3: DC analysis of the buffers added to prevent static current.

2.2 Simulation Results

The proposed novel hybrid regulator is designed using a 45 nm CMOS technology with a capacitance density of 30 nF/mm^2. The input voltage is 1.15 V and the output voltage is 0.5 V which is slightly larger than the threshold voltage. The nominal load current is 100 mA, as supplied by the switched-capacitor converter. The total capacitance is 3 nF which approximately occupies 0.1 mm^2, thereby achieving approximately 0.5 W/mm^2. As recently demonstrated by [14], regulators for portable SoCs require this power density to ensure proper operation at reasonable cost.

The output voltage and error amplifier output are plotted in Fig. 2.4 when the load current varies from 65 mA to 130 mA. As illustrated in this figure, the output of the error amplifier is reduced as the load current increases. Thus, additional current is supplied by the PMOS power transistor. Output voltage remains approximately at 0.5 V with a maximum ripple of 22 mV.

The power efficiency is plotted in Fig. 2.5 as a function of load current. At

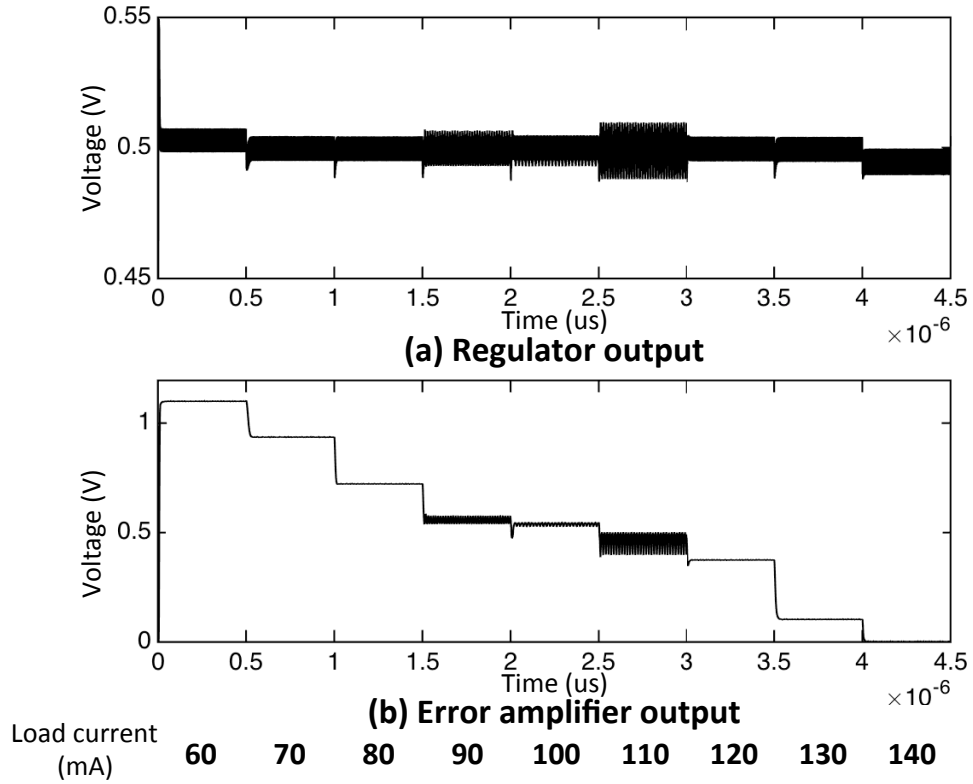

Figure 2.4: Simulation results as the load current abruptly changes from 60 to 140 mA with a step size of 10 mA: (a) output voltage of the regulator, (b) output voltage of the error amplifier.

the nominal load of 100 mA, the regulator achieves approximately 85% power efficiency. Note that the power efficiency is maintained above 70% across a relatively broad range of load current, from approximately 82 mA to 130 mA.

Finally, the transient response of the proposed regulator is depicted in Fig. 2.6. When the load current changes from 65 mA to 130 mA, the regulator requires approximately 18 ns to regulate the output voltage back to 0.5 V. Alternatively, when the load current changes from 130 mA to 65 mA, the regulator responds quicker with a response time of 10 ns. The maximum overshoot and undershoot are less than 50 mV in both cases.

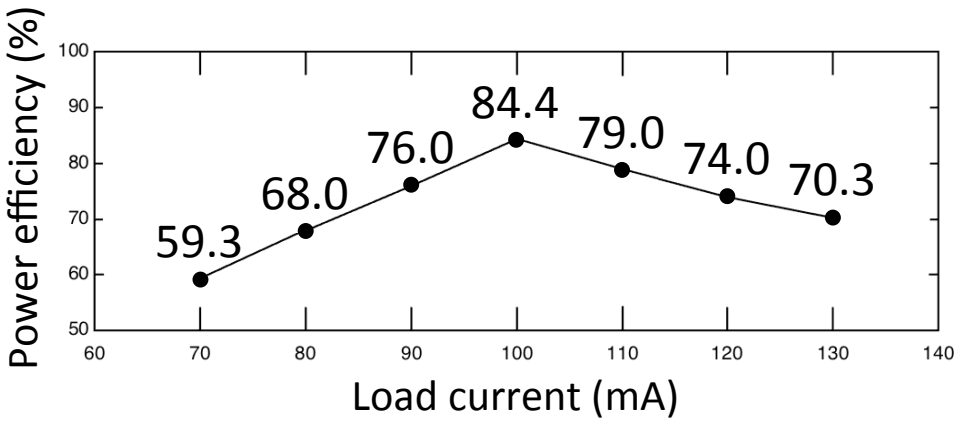

Figure 2.5: Power efficiency of the proposed regulator.

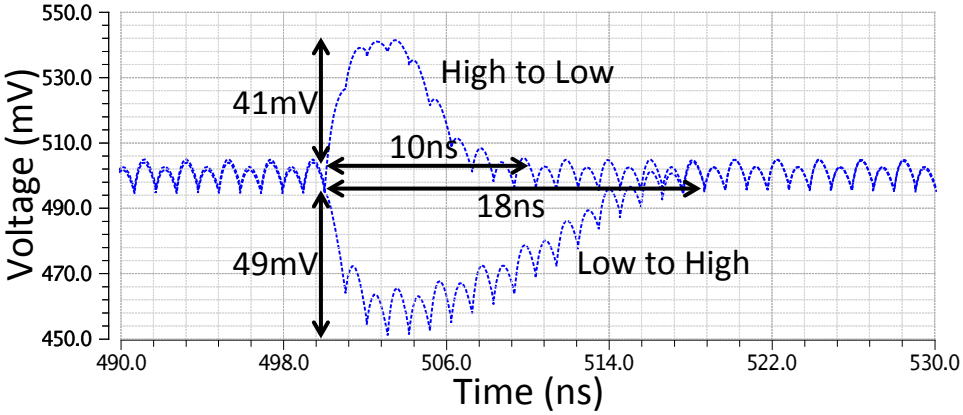

Figure 2.6: Transient response of the proposed regulator when the load current abruptly changes.

The proposed regulator is compared with several recent existing works, developed for similar applications. The comparison results are listed in Table 2.2. According to this table, at comparable current density, this work outperforms other works in both power efficiency and output ripple. Specifically, the output ripple is reduced by more than 60%, enabling a more robust near-threshold operation. A reasonable transient response time is also achieved.

Reference	H.-P Le 2013 [15]	R. Jain 2014 [16]	M. Abdelfattah 2015 [17]	This work
Technology	65 nm	22 nm trigate	45 nm SOI	45 nm
Input voltage	3-4V	1.23V	1.15V	1.15V
Output voltage	1V	0.45-1V @88mA	0.5V @5-125mA	0.5V @65-130mA
Power efficiency	73%	70%@0.55V 84%@1.1V	74-80% @5-125mA	84.4% @100mA
Response time	N/A	3-5ns	3-95ns	$<$20ns
Current density	0.19 A/mm^2	0.88 A/mm^2	1.25 A/mm^2	1 A/mm^2
Ripple voltage	N/A	60mV	62mV	Max:22 mV Min:9 mV

Table 2.2: Comparison of the proposed regulator with existing work.

Chapter 3

Enhancements to the Proposed Topology

3.1 Improved Hybrid Regulator

The enhanced version (second implementation) of the hybrid regulator is depicted in Fig. 3.1. This hybrid regulator uses the same switched-capacitor DC-DC converter topology, as described in Chapter 2. Nonoverlapping clock signals are used to avoid short circuit power loss during transition [13] [18]. Size of transistors and flying capacitor are optimized for 100 MHz and 400 MHz frequencies, respectively, for 30 mA and 80 mA load currents. Flip-flop based frequency divider is used to obtain the low frequency clock signal [19]. Some of the design parameters are listed in Table 3.1. The overall operation of this regulator is similar to that of the first implementation. Output variation is sensed and the variation is compensated by modulating the LDO current. In addition to modulating LDO current, this second implementation also employs frequency modulation for coarse regulation of the output voltage. One of the output voltages of error amplifiers is compared with one of the Schmitt trigger switching threshold voltages. When this output voltage

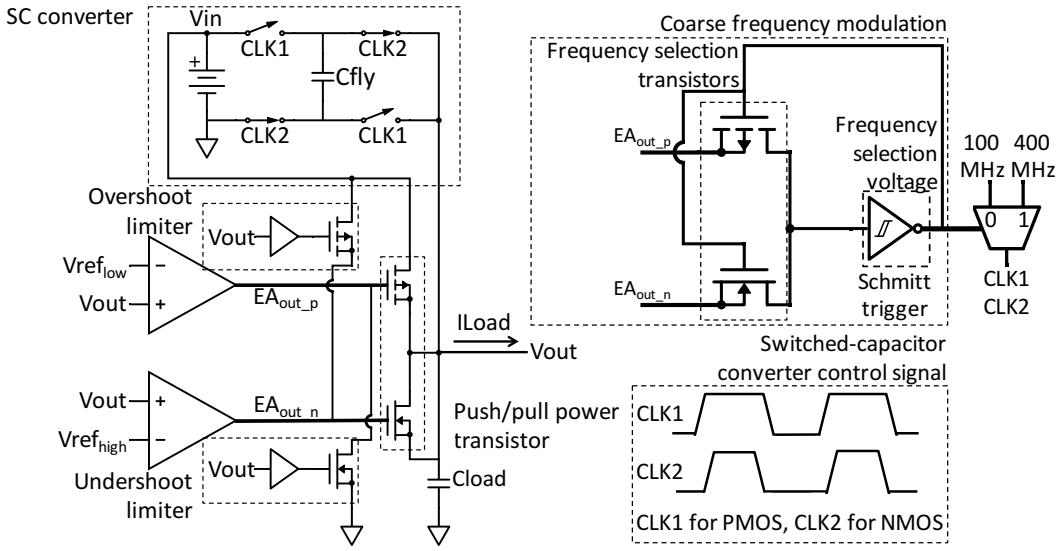

Figure 3.1: Enhanced hybrid regulator.

crosses the Schmitt trigger switching threshold voltage, the frequency modulation structure changes the frequency of the switched-capacitor converter. Frequency modulation introduces some delay which causes overshoot or undershoot at the output node when the load current exhibits a significant change. To avoid these over/undershoots, an additional structure is proposed. When the over/undershoot at the output is more than the tolerable limit, the additional structure is activated and the current through the push or pull power transistor is increased so that the regulator quickly regulates the output voltage. This structure is referred to as the over/undershoot limiter in Fig. 3.1. Two primary characteristics that enhance the first implementation are: 1) coarse frequency modulation, 2) over/undershoot limiters. These enhancements are described more in detail in the following subsections.

W_{sw}/L_{sw}	100×25 μm/50 nm
C_{fly}	0.85 nF
C_L	2.15 nF
Switching frequency	400 MHz & 100 MHz

Table 3.1: Primary parameters of the switched-capacitor converter.

3.1.1 Coarse Frequency Modulation

There are various previous studies on switched-capacitor converters with voltage regulation [20]. Most of these studies use fine frequency modulation (small step size) for voltage regulation [21], or flying capacitor modulation in addition to frequency modulation [17, 22]. These approaches require a large number of switching frequencies to enhance regulation efficiency. Furthermore, the optimum set of parameters (flying capacitance, switch size, and switching frequency) is different depending upon the output load current. Thus, different values are needed to optimize output ripple and power efficiency at each load current [21]. To alleviate these limitations, in this work, only two optimized switching frequencies are used as coarse frequency modulation and LDO plays a role in fine voltage regulation between these two frequencies. The coarse frequency modulation depicted in Fig. 3.1 consists of reference voltage selection and Schmitt trigger, as described in the following subsections.

3.1.1.1 Reference Voltage Selection

Coarse frequency modulation circuitry compares the output voltages of the error amplifiers. Note that since the operation of the NMOS and PMOS power transistors does not overlap, two reference voltages are required, Vref_{low} and Vref_{high}. Specifically, there are two possible scenarios: 1) load current changes from low to high and therefore switching frequency also changes from low to high, as shown in

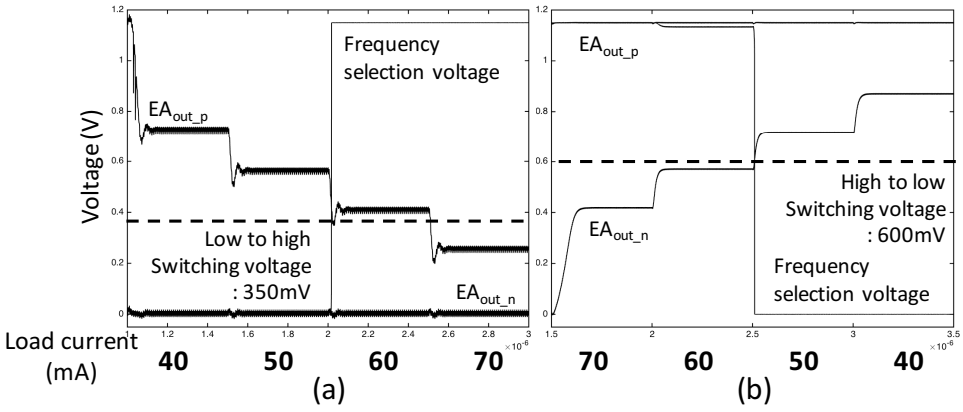

Figure 3.2: Important voltages as a function of load current, illustrating the behavior of the coarse frequency modulation.

Fig. 3.2(a), 2) load current changes from high to low and therefore switching frequency also changes from high to low, as shown in Fig. 3.2(b). In the first scenario, when the load current is higher than the nominal current (30 mA in this case) and continues to increase, PMOS power transistor plays the primary role in providing the supplementary current to the output node. In the mean time, the NMOS power transistor remains off since EAout$_n$ is at logic low. Thus, the output of the error amplifier for NMOS power transistor (EAout$_n$) cannot act as a reference voltage. Consequently, the input of the PMOS power transistor should be selected as the reference voltage. To achieve this process, the previous frequency selection voltage is directly connected to the gates of the frequency selection transistors, a pair of NMOS and PMOS transistors, as depicted in Fig. 3.1 by the coarse frequency modulation part. For instance, when the frequency selection voltage is at logic low, only the PMOS frequency selection transistor is turned on, so that the PMOS power transistor input voltage is used for comparison.

3.1.1.2 Schmitt Trigger

Frequency modulation circuitry consists of a Schmitt trigger to obtain different switching voltages depending on whether the load current increases or decreases. Hysteresis characteristic of Schmitt trigger is helpful to choose a different specific load current at which the frequency changes, depending upon whether the load current is rising or falling. This characteristic maximizes the overall power efficiency with consideration of the nominal currents. Furthermore, this characteristic is also helpful for the stability of the regulator. Output voltage of the error amplifiers exhibits a certain amount of ripple, which can be reduced by decreasing the response time of the LDO [1]. Note that in this implementation with two switching frequencies, most of the parameters are optimized for the low frequency (100 MHz). Thus, the response time of the LDO at higher frequencies can be degraded. To alleviate this issue, the response time of the LDO should be as short as possible without sacrificing the output voltage, particularly at the low switching frequency. However, if the response time is too short, the large ripple at the output of the error amplifier can make the LDO unstable. To avoid this condition, there should be enough margin between the two switching voltages of the Schmitt trigger. Output voltages for both stable and unstable regulator are depicted in Fig. 3.3. In Fig. 3.3(a), there is 20 mV voltage gap between two switching voltages of the Schmitt trigger with hysteresis whereas in Fig. 3.3(b), the gap is 250 mV. In the first case, the regulator is unstable with a ripple voltage of 122 mV whereas in the second case, the ripple is only 50 mV and the regulator is stable. Implementation of Schmitt trigger topology is based on [23].

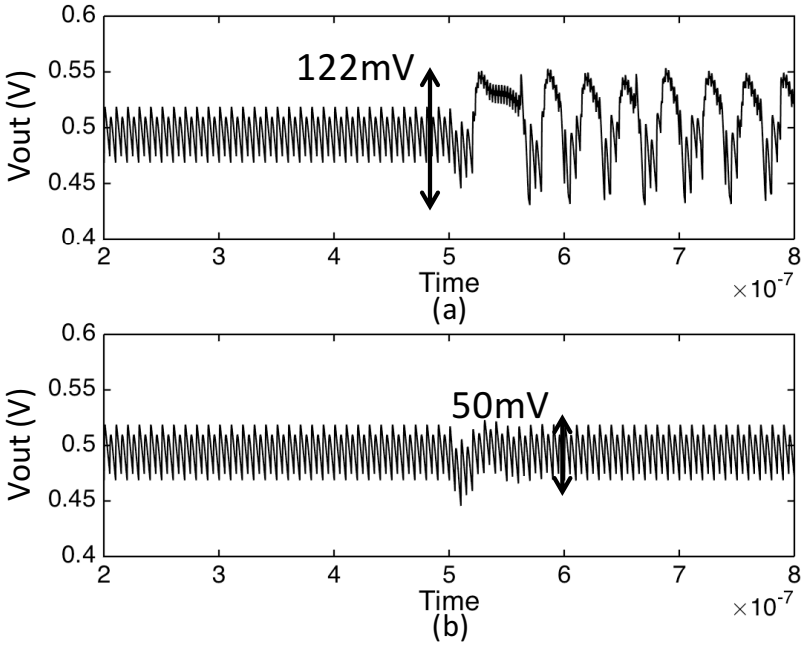

Figure 3.3: Regulator output voltage: (a) small voltage gap between the switching voltages in Schmitt trigger, (b) larger voltage gap between the switching voltages in Schmitt trigger.

3.1.2 Enhancements to LDO

As depicted in Fig. 3.1, the enhanced LDO consists of three parts: 1) error amplifier, 2) power transistor and 3) over/undershoot limiter. Contrary to the first implementation, this regulator does not have the extra static current minimization circuitry. Instead, two error amplifiers with different reference voltages are in charge of the short circuit current minimization by ensuring that either PMOS or NMOS power transistor is on at a time. Another difference from the first implementation described in Chapter 2 is the over/undershoot limiter. Since the enhanced topology utilizes frequency modulation (between 100 MHz and 400 MHz) for coarse regulation, the output exhibits large over/undershoot when the frequency changes. Furthermore, since the frequency modulation is determined by the output of the error amplifiers,

it is relatively more challenging to react in a sufficiently fast manner. To alleviate these over/undershoots, small PMOS and NMOS transistors are connected to the input of the PMOS and NMOS power transistors, respectively, as shown in Fig. 3.1. These additional transistors help the power transistors to quickly supply full current to the output or drain full current from the output. Note that these transistors are activated only when the buffers (at the input of the transistors) sense a large output voltage variation (indicating that the frequency is modulated from 100 MHz to 400 MHz or vice versa). Similar to the static current minimization described in Chapter 2, each buffer has different switching voltage.

3.2 Simulation Results

The second implementation of the proposed novel hybrid regulator is also designed using a 45 nm CMOS technology with a capacitance density of 30 nF/mm^2. The input voltage is 1.15 V and the output voltage is 0.5 V. The nominal load current for 0.5 V output voltage is 30 mA at 100 MHz switching frequency and 80 mA at 400 MHz switching frequency, as decided by the switched-capacitor converter. The ovarall capacitance is 3 nF which approximately occupies 0.1 mm^2 in this 45 nm technology, thereby achieving more than 0.5 W/mm^2 as the highest power density. Note that all of the capacitors are implemented as MOS-CAP in this technology.

The output voltage and error amplifier output are plotted in Fig. 3.4 when the load current varies from 10 mA to 120 mA. The output voltage of the error amplifier EAout$_p$ (input of the PMOS power transistor) first decreases as the load current increases to supply more current. Once the voltage reaches a certain point, 350 mV in this case, the switching frequency of the switched-capacitor converter changes from 100 MHz to 400 MHz. At this higher switching frequency, the LDO structure

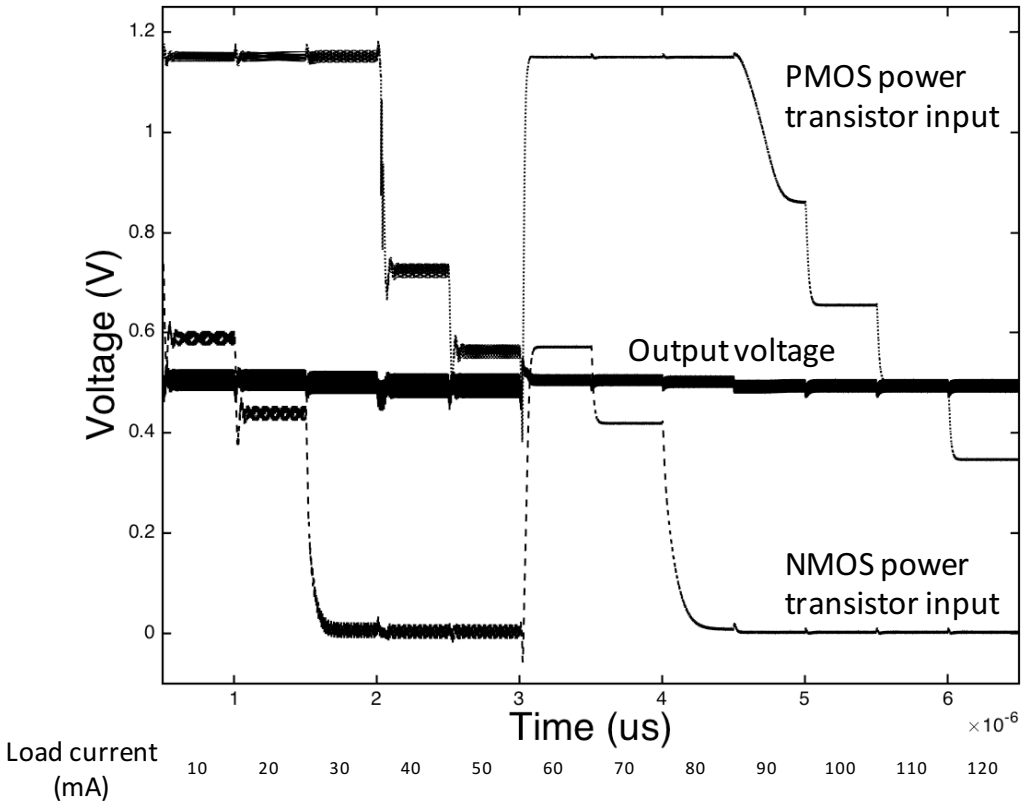

Figure 3.4: Simulation results as the load current changes from 10 to 120 mA with a step size of 10 mA, Once the input voltage of the PMOS power transistor falls to 350 mV, the switching frequency of the switched-capacitor converter changes from 100 MHz to 400 MHz. The output voltage remains approximately constant with a ripple voltage of 50 mV.

readjusts the amount of auxiliary current. This process enables the output voltage to remain approximately constant at 0.5 V with a maximum ripple of 50 mV.

The power efficiency is plotted in Fig. 3.5 as a function of load current. At the nominal load currents of 30 mA (at 100 MHz switching frequency) and 80 mA (at 400 MHz switching frequency), the regulator achieves approximately 80% maximum power efficiency. The efficiency is maintained more than 60% in a wide range of load current, from 20 mA to 120 mA and more than 70% in the range of

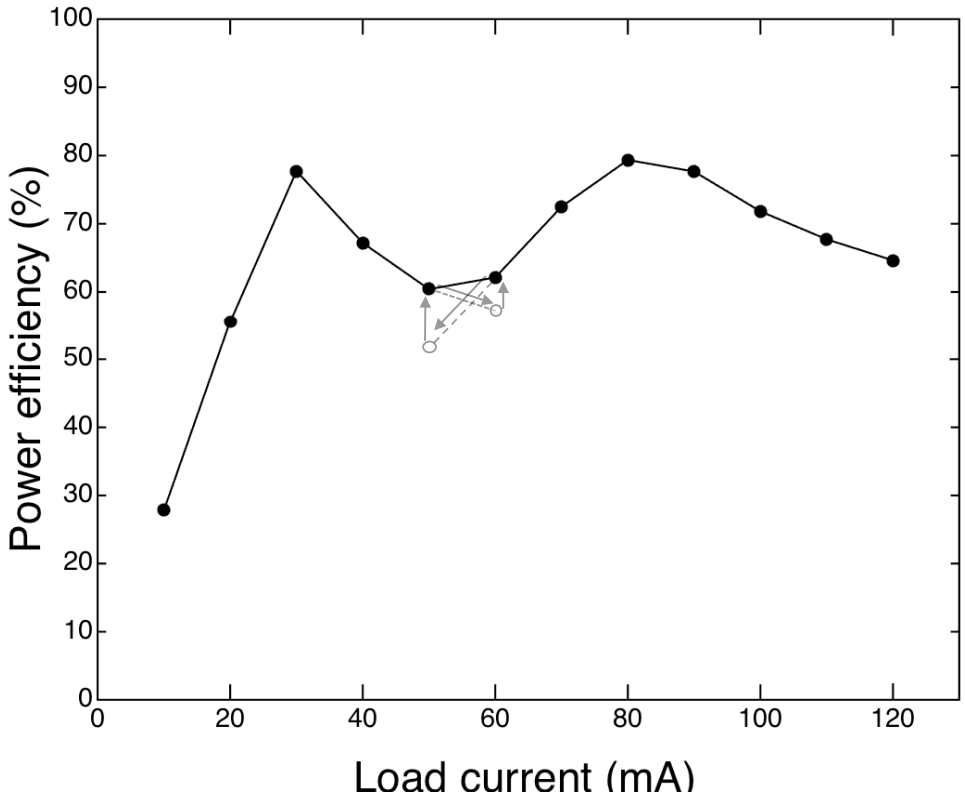

Figure 3.5: Power efficiency of the proposed regulator.

25 mA to 40 mA and 65 mA to 100 mA. The overall power efficiency exhibits a tradeoff with the range of the load current.

Finally, the transient response of the proposed regulator is depicted in Fig. 3.6. When the load current instantly changes from 110 mA to 10 mA, the regulator requires approximately 40 ns to regulate the output voltage back to 0.5 V. Alternatively, when the load current changes from 10 mA to 110 mA, the regulator responds quicker within 13 ns. The maximum overshoot is 70 mV and undershoot is less than 110 mV thanks to the over/undershoot limiter. The primary performance characteristics of the proposed regulator are compared with recent existing work in Table 3.2. As listed in this table, the second implementation described in this

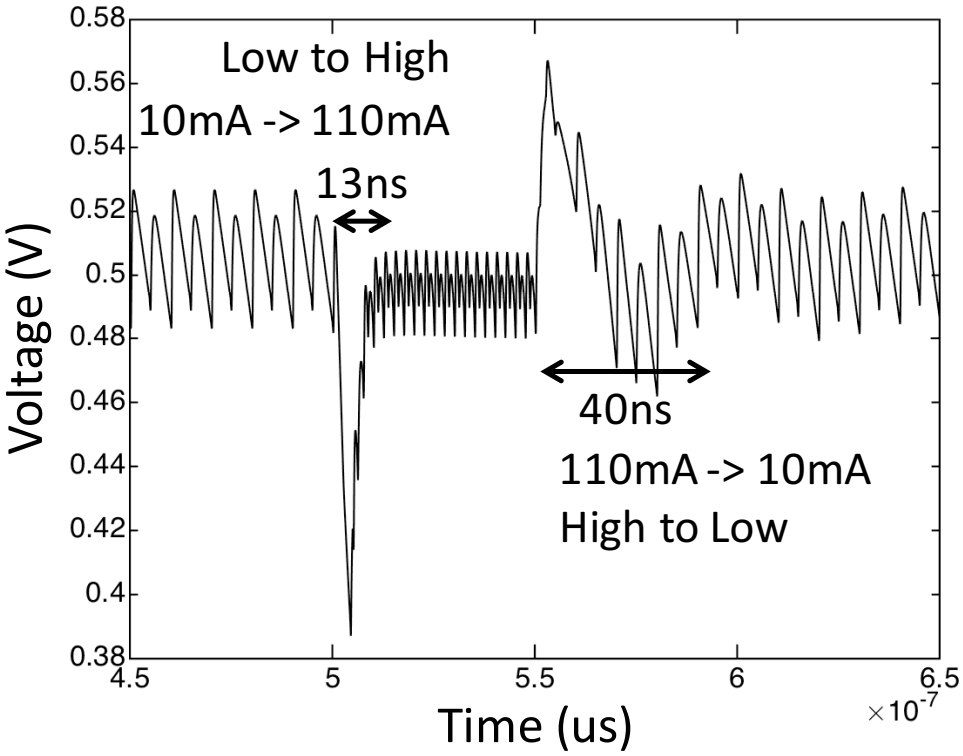

Figure 3.6: Transient response of the proposed regulator when the load current abruptly changes.

chapter significantly enhances the load current range at the expense of slight degradation in efficiency, response time, and ripple voltage. As compared to previous work, the proposed regulator achieves lower ripple voltage and faster response time for a wide range of load current.

Reference	H.-P Le 2013 [15]	R. Jain 2014 [16]	M. Abdelfattah 2015 [17]	First implementation	Second implementation
Technology	65 nm	22 nm trigate	45 nm SOI	45 nm	45 nm
Input voltage	3-4V	1.23V	1.15V	1.15V	1.15V
Output voltage	1V	0.45-1V @88mA	0.5V @5-125mA	0.5V @65-130mA	0.5V @0-130mA
Power efficiency	73%	70%@0.55V 84%@1.1V	74-80% @5-125mA	84.4% @100mA	60-80% @20-120mA
Response time	N/A	3-5ns	3-95ns	<20ns	<40ns
Current density	0.19 A/mm^2	0.88 A/mm^2	1.25 A/mm^2	1 A/mm^2	1 A/mm^2
Ripple voltage	N/A	60mV	62mV	Max:22 mV Min:9 mV	<50mV

Table 3.2: Comparison of the proposed regulator with existing work.

Chapter 4

Conclusion and Future Work

A novel hybrid regulator topology has been proposed for near-threshold computing in portable SoCs. Contrary to existing approaches, a switched-capacitor converter and an LDO operate in a parallel connection to convert and regulate the output voltage. The proposed implementations do not contain any resistors to minimize power loss, particularly within LDO. Several techniques have been introduced to maximize power efficiency while keeping voltage ripple sufficiently small. The proposed regulator is compared with several recent existing works, developed for similar applications. Specifically, at comparable current density, this work outperforms existing works in both power efficiency and output ripple voltage. A reasonable transient response time and over/undershoot are also achieved. Furthermore, the frequency modulation significantly increases the range of load current with slight degradation in power efficiency. Simulation results in 45 nm technology demonstrate that the proposed regulator outperforms existing approaches in primary design objectives.

To further enhance the power efficiency of the proposed topology, additional switching frequencies (more than two) can be added for coarse regulation. In the second implementation described in Chapter 3, the regulator operates at two switch-

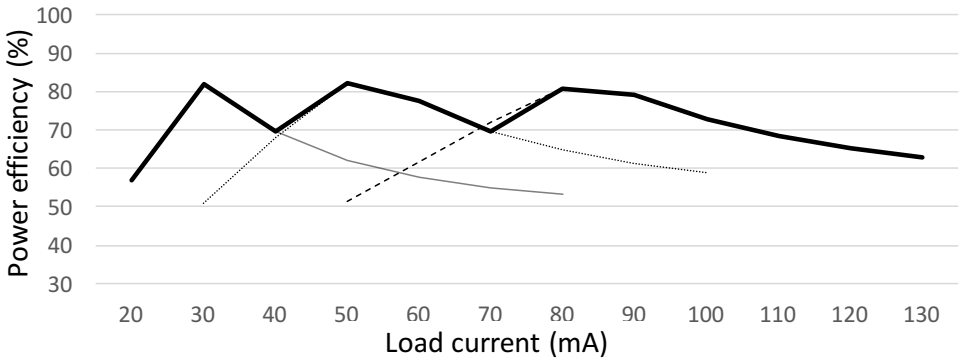

Figure 4.1: Increase in power efficiency when an additional switching frequency of 200 MHz is added for a load current of 60 mA.

ing frequencies of 100 MHz (optimized for 30 mA of load current) and 400 MHz (optimized for 80 mA of load current). If an additional switching frequency of 200 MHz is introduced for 60 mA of load current, the power efficiency increases (above 70%) for a larger range of load current, as illustrated in Fig. 4.1. However, as the number of switching frequencies increases, the complexity of the circuit also increases. Thus, it is important to determine the optimum number of switching frequencies based on the required design objectives.

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