Reducing Delay Uncertainty in Deeply Scaled Integrated Circuits Using Interdependent Timing Constraints

Emre Salman and Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627 USA
[salman,friedman]@ece.rochester.edu

ABSTRACT

Interdependent setup-hold times are exploited during the *design process* to reduce *delay uncertainty*. Considering this interdependence only during static timing analysis (STA) is insufficient to fully exploit the capabilities offered by interdependence. This result is due to the strong dependence of STA on the specific circuit, cell library, and operating frequency. Interdependence is evaluated in this paper for several technologies to determine the overall reduction in delay uncertainty rather than improvements in STA. The increasing efficacy of interdependence in deeply scaled technologies is also demonstrated by investigating the effect of technology scaling on interdependent timing constraints.

1. INTRODUCTION

Cell library characterization is a critical step in static timing analyses (STA) of large scale integrated circuits [1, 2]. Since an STA tool relies on the data described in these libraries to analyze the timing characteristics of a circuit, the overall accuracy of STA is strongly dependent upon the accuracy of cell library characterization.

The setup and hold times, *i.e.*, timing constraints, of a sequential cell play an important role in the timing analysis process since these timing constraints are used to determine whether a circuit can properly operate at the required clock frequency. Previous work has shown that the setup-hold times and CLK-to-Q delay of a sequential cell are *interdependent* [3, 4]. An *independent* characterization process may produce either optimistic or overly pessimistic STA results. Both cases should be avoided as the optimistic case can cause a circuit to fail whereas the pessimistic case unnecessarily degrades circuit speed.

One of the challenges in interdependent characterization of timing constraints is computational complexity since each sequential cell in a library should be extensively simulated to obtain the *CLK-to-Q delay surface* [3]. The computational efficiency of interdependent setup-hold time characterization has been improved through state transition equations [5, 6]. Interdependent setup-hold times have also been exploited in statistical static timing analysis processes [7].

While the need for interdependent characterization and using these interdependent timing constraints within the STA process have been well understood [3–7], the significance of interdependence has not been investigated in deeply scaled technologies. A disadvantage of relying only on STA is the inability to accurately evaluate the significance of interdependence. Specifically, the results presented in [3] strongly depend upon the specific circuit and clock frequency. For example, while interdependence can significantly reduce timing violations in one circuit, interdependence may not be as efficient in another circuit with the same technology, producing inconsistent results. A different approach is proposed in this paper where the ability of the interdependence *to tolerate variations and reduce delay uncertainty* is investigated rather than improving timing analysis. This approach provides a more complete understanding of the efficacy of interdependence. Furthermore, the evolution of interdependence with process technology is also investigated to determine the effects of scaling on these interdependent timing constraints.

The rest of the paper is organized as follows. Background material reviewing the timing characteristics of a circuit and setup-hold interdependence is provided in Section 2. The problem is formulated in Section 3. A procedure to reduce delay uncertainty and compensate for variations is described in Section 4. A case study is presented in Section 5 to evaluate the significance of setup-hold interdependence to compensate for power supply variations for four technology generations. Finally, the paper is concluded in Section 6.

2. BACKGROUND

The timing characteristics of synchronous circuits are reviewed in Section 2.1. Interdependent setup-hold times are summarized in Section 2.2.

2.1 Timing Characteristics of Synchronous Circuits

A simple synchronous digital circuit consisting of two sequentially-adjacent registers with a combinational circuit between these registers is shown in Fig. 1. Two inequalities should be satisfied for this circuit to function properly. Referring to Fig. 1, the first inequality is

$$T_{Cf} + T_{CP} \geq T_{Ci} + T_D + T_S, \tag{1}$$

where T_{Ci} and T_{Cf} are the delay for the clock signals to arrive, respectively, at the *initial* and *final* registers. Note that T_{Ci} and T_{Cf} are also referred to as, respectively, the delay of the clock launch path and clock capture path. T_{CP} is the clock period, T_D is the data path delay consisting of the clock-to-Q delay of the initial register, logic delay of the combinational circuit, and the interconnect delay.

This research is supported in part by the Semiconductor Research Corporation under Contract No. 2004-TJ-1207, the National Science Foundation under Contract No. CCF-0541206, grants from the New York State Office of Science, Technology & Academic Research to the Center for Advanced Technology in Electronic Imaging Systems, and by grants from Intel Corporation, Eastman Kodak Company, and Freescale Semiconductor Corporation.

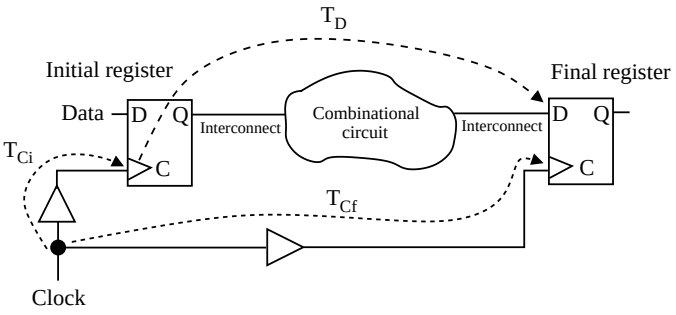
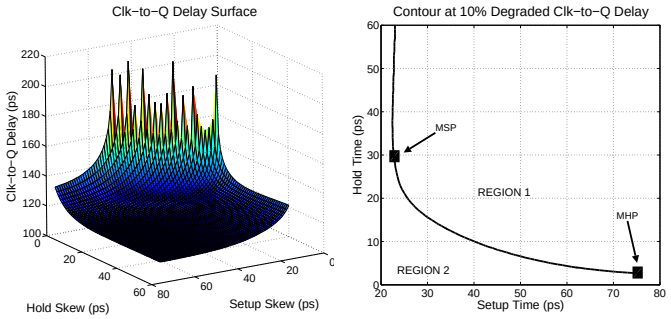


Figure 1: Simple synchronous circuit consisting of a combinational logic and two registers.



(a) (b)

Figure 2: Interdependent setup-hold time characterization: (a) CLK-to-Q delay surface as a function of independently varying setup skew and hold skew, (b) The contour at 10% degraded CLK-to-Q delay.

T_S is the setup time of the final register. Note that (1) determines the maximum speed of the circuit, making this inequality important for the critical paths within a circuit.

The second inequality that needs to be satisfied is

$$T_{Ci} + T_D \geq T_{Cf} + T_H, \tag{2}$$

where T_H is the hold time of the final register. This inequality guarantees that no race condition exists, *i.e.*, the data is not latched within the final register during the same clock edge. Note that (2) is relatively more important for those timing paths where the data path delay is sufficiently small, such as a shift register or counter.

2.2 Interdependent Setup-Hold Times

Existing approaches to characterize the timing constraints of a register, *i.e.*, setup and hold times in (1) and (2), assume these timing constraints are independent [8]. This independent characterization produces overly pessimistic results since the setup-hold times are, in reality, interdependent [3]. An example of an interdependent setup-hold contour curve obtained from a clock-to-Q delay surface at a constant delay is illustrated in Fig. 2 [4]. In Fig. 2(a), the CLK-to-Q delay is obtained as a function of independently varying setup skew and hold skews. Those setup and hold skews corresponding to a specific per cent degradation in CLK-to-Q delay are extracted from this surface, representing a contour curve. Each (setup, hold) pair on this contour curve shown in Fig. 2(b) is a valid pair for the register. Multiple timing constraints therefore exist rather than a single setup and hold time. As indicated in Fig. 2(b), a small setup time can be obtained at the expense of a large hold time. Similarly,

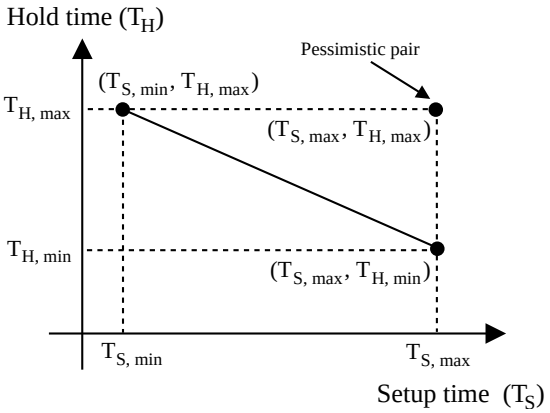


Figure 3: Linear approximation of the contour curve using two pairs: ($T_{S,min}$, $T_{H,max}$) and ($T_{S,max}$, $T_{H,min}$).

a small hold time can be obtained at the expense of a large setup time. For example, *minimum setup pair* (*MSP*) and *minimum hold pair* (*MHP*) refer, respectively, to a pair on the contour with the minimum setup time and minimum hold time. Also note that any pair in region 1 is also valid with additional pessimism, whereas any pair in region 2 is invalid, as the pairs in this region are optimistic.

Previous work has primarily focused on the timing analysis [3,4, 7] and characterization aspects of interdependence [5,6]. Considering only STA results, however, is insufficient to fully understand the capabilities of interdependence. Interdependent setup-hold times not only reduce pessimism in timing analysis, but also provide an opportunity to improve the tolerance of a circuit to process and environmental variations. Investigating interdependence from this perspective enhances the capability of interdependent timing constraints in reducing delay uncertainty. Furthermore, the dependence of interdependence on technology is also investigated, demonstrating the increasing significance of interdependence in deeply scaled technologies.

3. PROBLEM FORMULATION

The contour curve illustrated in Fig. 2(b) can be approximated as a linear line using two critical pairs: *MSP* and *MHP*. Note that this approximation is valid since any point above the curve, *i.e.*, in region 1, is a valid pair with some pessimism. An approximation of the contour using two critical pairs is illustrated in Fig. 3 where the pairs *MSP* and *MHP* are represented, respectively, as ($T_{S,min}$, $T_{H,max}$) and ($T_{S,max}$, $T_{H,min}$).

According to (1) and (2) and referring to Fig. 1, the delay of the data path should satisfy

$$T_{Cf} + T_H - T_{Ci} \leq T_D, \tag{3}$$

$$T_D \leq T_{Cf} + T_{CP} - (T_{Ci} + T_S), \tag{4}$$

where (3) and (4) determine, respectively, the lower and upper bounds of the data path delay.

Characterization of the setup and hold times affects the design process by constraining the data path delay T_D. The allowable range of T_D is minimized if the pessimistic pair ($T_{S,max}$, $T_{H,max}$) is used, causing the circuit to be overdesigned. Which specific (setup, hold) pair should be chosen to design the circuit is unclear even if the interdependence is known since multiple valid pairs are available. For example, if the pair ($T_{S,min}$, $T_{H,max}$) is used, the

lower bound constraint of the data path delay is difficult to satisfy since the hold time is large. Hence, the data path delay should be increased by inserting additional stages, dissipating unnecessary power. Alternatively, if the pair ($T_{S,max}$, $T_{H,min}$) is used, the upper bound constraint on the data path delay is difficult to satisfy since the setup time is large. Consequently, the data path delay should be lowered by inserting an additional register to satisfy the target frequency, also causing unnecessary power consumption. Furthermore, both pairs ($T_{S,min}$, $T_{H,max}$) and ($T_{S,max}$, $T_{H,min}$) exhibit low tolerance to process and environmental variations since the range of valid setup times $T_{S,max} - T_{S,min}$ and hold times $T_{H,max} - T_{H,min}$ is not exploited.

It is therefore important to determine the appropriate (setup time, hold time) pair during the design process that lowers power consumption, satisfies the required delay, and increases the robustness of the circuit to achieve a higher tolerance to process and environmental variations. This procedure exploits interdependence to reduce delay uncertainty, as described in the following section.

4. REDUCING DELAY UNCERTAINTY

A procedure to reduce delay uncertainty and compensate for variations is described in Section 4.1. The amount of compensation achieved by the proposed technique is determined in Section 4.2.

4.1 Procedure to Reduce Delay Uncertainty

For a critical path, an increase in the delay of a data path ΔT_D due to variations causes the frequency to be decreased to satisfy (4). This increase in the data path delay produces additional slack in (3), *i.e.*, hold skew. This additional slack in the hold skew can be exploited to increase the hold time in (3) by ΔT_{Hold} where $\Delta T_{Hold} = \Delta T_D$. An increase in the hold time enables a decrease in the setup time by $\Delta T_S = f^{-1}(\Delta T_H)$ due to the interdependence, as illustrated in Fig 3. The effect of the variation, *i.e.*, the decrease in frequency, can therefore be compensated by exploiting a lower setup time.

Similarly, for a timing path sensitive to a race condition, referred to as a *short path*, a decrease in the delay of the data path by ΔT_D can cause a hold time violation. Since the delay of the data path is reduced, any additional slack in (4), *i.e.*, setup skew, can be exploited by increasing the setup time by ΔT_S where $\Delta T_S = \Delta T_D$. An increase in the setup time supports a decrease in the hold time by $\Delta T_H = f(\Delta T_S)$, potentially resolving the violation. The delay uncertainty due to a variation is therefore reduced by exploiting interdependent setup-hold times. This procedure is summarized in the flowchart depicted in Fig. 4.

Note that the variation in the delay of the clock launch path ΔT_{Ci} and clock capture path ΔT_{Cf} is assumed in this approach to be equal. For those cases where this assumption is not accurate, the variation in the delay of the clock path may either enhance or degrade the delay uncertainty depending upon the sign of $\Delta T_{Cf} - \Delta T_{Ci}$, as described in the following section.

4.2 Amount of Compensation

The compensation in delay variation (or the reduction in delay uncertainty) is dependent upon three primary factors: (a) the range of the valid setup times $T_{S,r}$ and hold times $T_{H,r}$, (b) the specific (setup, hold) pair used in (3) and (4) to determine the data path delay, and (c) the effect of the variations on the clock launch and capture paths, *i.e.*, the clock distribution network.

If a register has a greater range of valid setup times and hold times, this register is more effective in reducing delay uncertainty. Note however that this type of register may exhibit other tradeoffs such as higher power consumption and CLK-to-Q delay.

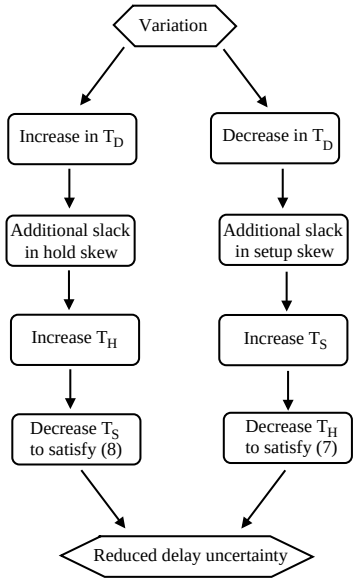


Figure 4: Flow diagram to reduce delay uncertainty by exploiting interdependent setup-hold times.

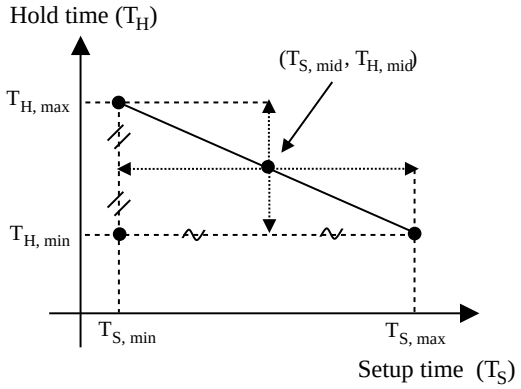


Figure 5: A data path designed at the pair $(T_{S,mid}, T_{H,mid})$ achieves the highest tolerance to variations.

As described in Section 3, the specific (setup, hold) pair used to determine the data path delay can lower the power consumption while satisfying the target frequency and achieving a higher tolerance to variations. The middle point of the setup-hold line ($T_{S,mid}$, $T_{H,mid}$) results in a highest tolerance since the setup and hold times exhibit the maximum flexibility to variations, as illustrated in Fig. 5. Note that in this case, the data path should be designed to ensure that the delay of the data path satisfies both (3) and (4), specifically when the setup time and hold time are, respectively, $T_{S,mid}$ and $T_{H,mid}$. This technique is analogous to clock skew optimization techniques proposed in the mid 90's where the circuit is designed at the middle of the clock skew range among possible skew values (referred to as the permissible range) to maximize the tolerance of a circuit to variations [9, 10].

The amount of variation tolerated by this methodology is also dependent upon the variation in the delay of the clock launch path ΔT_{Ci} and clock capture path ΔT_{Cf}. Specifically, if $\Delta T_{Ci} = \Delta T_{Cf}$, *i.e.*, constant clock skew, these variations compensate, maintaining the validity of the proposed algorithm. In this case, the variation in the delay of the clock paths does not affect the amount of tolerance.

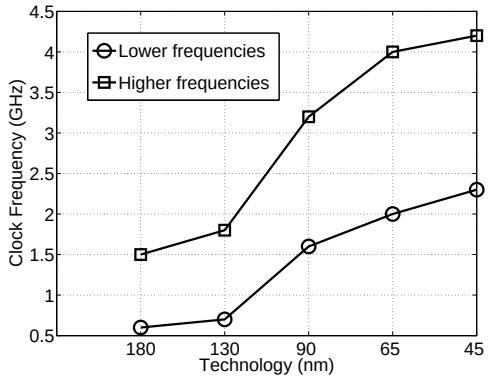


Figure 6: Target clock frequency for each technology node. Higher frequencies represent the upper bound of the frequency while the lower frequencies represent the lower bound of the frequency.

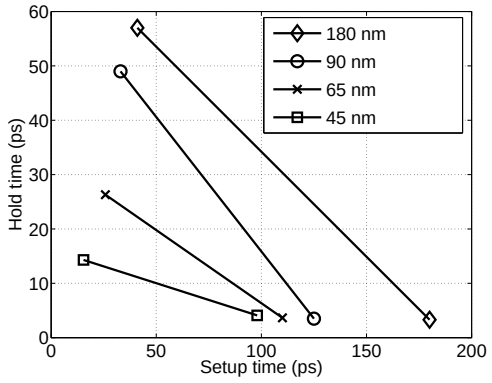


Figure 7: Interdependent setup-hold time characteristics for four technologies.

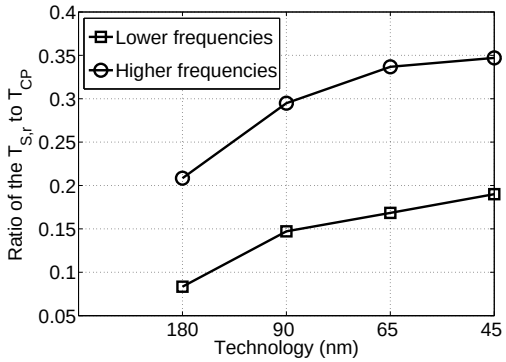


Figure 8: Ratio of the range of valid setup times $T_{S,r}$ to the clock period T_{CP}.

If however $\Delta T_{Ci} > \Delta T_{Cf}$, less variation can be tolerated by a critical path since the delay of the clock launch path is increased, delaying the data signal from leaving the register. For a short path, however, additional variation can be tolerated.

Alternatively, if $\Delta T_{Cf} > \Delta T_{Ci}$, additional variation can be tolerated for a critical path since the clock launch path is relatively faster than the clock capture path. For a short path, however, less variation can be tolerated.

5. CASE STUDY

The efficacy of setup-hold time interdependence to compensate power supply variations is evaluated in this section. Note that power supply noise is considered here as an example to demonstrate the significance and utility of the setup-hold interdependence. Other factors that introduce delay uncertainty such as process and temperature variations can also be considered to evaluate the significance of setup-hold interdependence.

Four CMOS technology generations are considered: 180 nm, 90 nm, 65 nm, and 45 nm. An industrial model is used for the 180 nm, 90 nm, and 65 nm CMOS technologies. For the 45 nm CMOS technology, a predictive model is used [11]. Two clock frequencies are considered for each technology based on the data published in [12], as illustrated in Fig. 6. Higher frequencies represent the upper bound on the frequency while the lower frequencies represent the lower bound on the frequency.

The interdependent setup-hold time characteristics for each technology is described in Section 5.1. The dependence of these characteristics on process technology is also discussed. The variation in the delay caused by the power noise is quantified as a function of technology in Section 5.2. Finally, the efficacy of setup-hold time interdependence in tolerating this delay variation is evaluated in Section 5.3.

5.1 Interdependent T_S vs T_H Relationship

A master-slave type, rising edge triggered register is used to illustrate the T_S vs. T_H relationship for each technology node. The register has been simulated to obtain the critical setup-hold pairs, where the signal transition times are assumed to be 10% of the clock period. The T_S vs. T_H relationship for each technology is illustrated in Fig. 7. Each line can be represented as

$$\text{180 nm: } T_H = -0.386T_S + 72.839 \text{ for } 41 \leq T_S \leq 180, \quad (5)$$

$$\text{90 nm: } T_H = -0.494T_S + 65.32 \text{ for } 33 \leq T_S \leq 125, \quad (6)$$

$$\text{65 nm: } T_H = -0.269T_S + 33.255 \text{ for } 25.8 \leq T_S \leq 110, \quad (7)$$

$$\text{45 nm: } T_H = -0.123T_S + 16.202 \text{ for } 15.4 \leq T_S \leq 98, \quad (8)$$

where each range is in picoseconds. The range of valid setup times $T_{S,r} = T_{S,max} - T_{S,min}$ and range of valid hold times $T_{H,r} = T_{H,max} - T_{H,min}$ scale with technology, as shown in Fig. 7. These critical points, CLK-to-Q delay of the register, and power supply voltage are listed in Table 1 for each CMOS technology.

Note the behavior of $T_{S,r} = T_{S,max} - T_{S,min}$ (range of valid setup times) as a function of technology. The ratio of the range of valid setup times to the clock period ($T_{S,r}/T_{CP}$) increases as the technology advances, as illustrated in Fig. 8. Specifically, for the 45 nm CMOS technology, the range of valid setup times is approximately 20% of the clock period at lower frequencies. At higher frequencies, this ratio increases to 35%. The interdependence of the setup-hold times is therefore more able to tolerate variations in deep submicrometer technologies, where the difference between the maximum and minimum setup time is a significant fraction of the clock period.

5.2 Delay Variation due to Power Noise

The effect of power supply variations, *i.e.*, power noise, on delay

Table 1: Power supply voltage, clock-to-Q delay, and critical points $T_{S,min}$, $T_{H,max}$, $T_{S,max}$, $T_{H,min}$, $T_{S,r}$, and $T_{H,r}$ for each technology.

CMOS Technology	V_{DD} (V)	Clock-to-Q delay (ps)	$T_{S,min}$ (ps)	$T_{H,max}$ (ps)	$T_{S,max}$ (ps)	$T_{H,min}$ (ps)	$T_{S,r}$ (ps)	$T_{H,r}$ (ps)
180 nm	1.8	172	41	57	180	3.3	139	53.7
90 nm	1.2	86.4	33	49	125	3.5	92	45.5
65 nm	1.1	57	25.8	26.3	110	3.6	84.2	22.7
45 nm	1.0	29.8	15.4	14.3	98	4.1	82.6	10.2

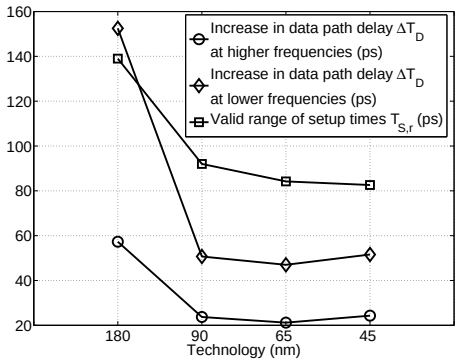


Figure 9: Comparison of the increase in the delay of a critical data path with $T_{S,r}$ to evaluate the efficacy of exploiting the interdependence relationship.

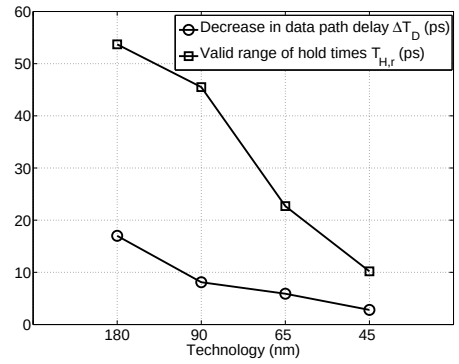


Figure 10: Comparison of the decrease in the delay of a short path with $T_{H,r}$ to evaluate the efficacy of exploiting the interdependence relationship.

is evaluated in this section. These variations are compared with the range of valid setup times $T_{S,r}$ and hold times $T_{H,r}$, thereby determining the ability to exploit this interdependence to reduce delay uncertainty. The clock period corresponding to each technology is determined from Fig. 6. A critical path is designed for each technology to evaluate the efficacy of exploiting the interdependence relationship in compensating for a drop in the power supply voltage. Identical inverters are used in the combinational circuit. A specific number of inverters is inserted between the initial and final register until the delay of a data path satisfies (4).

A short path can also be generated by abutting the registers. This short path is designed to evaluate the efficacy of exploiting the interdependence relationship in compensating for an increase in the power supply voltage since an increase in V_{DD} reduces the delay of the data path.

These long and short paths are simulated with SPICE, where the power supply voltage is varied by 10%. Specifically, for a long path, the power supply is decreased by 10% while for a short path, the power supply is increased by 10%. The corresponding variation in the delay of the data path is determined by SPICE simulations for each technology. These variations are compared with the range of valid setup times $T_{S,r}$ and hold times $T_{H,r}$, respectively, in Figs. 9 and 10 to evaluate the efficacy of exploiting the interdependence relationship, as described in the following section.

5.3 Compensation of Delay Variations

As illustrated in Fig. 9, the interdependence relationship can be used to compensate for delay variations since the range of valid setup times is higher than the increase in the data path delay except for the 180 nm CMOS technology operating at 600 MHz. At this frequency, the delay of the data path is relatively large, causing a higher absolute variation in the delay.

Note that the difference between the range of valid setup times and variation in delay is larger at higher frequencies since the delay of the data path is lower for these frequencies. Exploiting the interdependence relationship is therefore more effective in reducing the delay uncertainty of a critical path operating at higher frequencies. Also note that the absolute variation in delay due to power supply noise somewhat saturates beyond the 130 nm technology node. This behavior is primarily due to the use of multicore processors where the increase in clock frequency is relatively low, as illustrated in Fig. 6.

For a short path, the range of valid hold times is larger than the decrease in data path delay for each technology, as illustrated in Fig. 10. The difference between these two values, however, decreases for more deeply scaled technologies. For a short path, therefore, the interdependence relationship is more effective in reducing delay uncertainty in older technologies. This behavior is due to the significant decrease in the range of valid hold times with scaled technologies.

The procedure described in Section 4 has been performed on both long and short data paths. Note that these data paths are designed at the middle point $(T_{S,mid},\ T_{H,mid})$ of the interdependent setup-hold line. For example, for the 90 nm CMOS circuit operating at 3.2 GHz, the delay of the worst case data path increases by 23.7 ps due to a drop in power supply voltage. The hold time of 26.3 ps is increased by 23.7 ps to 50 ps. Since 50 ps is larger than the maximum hold time at this technology, the hold time is increased to 49 ps. An increase in the hold time enables a decrease in the setup time from 79 ps to 33 ps, tolerating 46 ps of delay uncertainty. Note that this delay uncertainty is larger than the initial variation of 23.7 ps, achieving about 100% delay compensation in the critical path.

Similarly, for a short path, the decrease in the delay of the data

Table 2: Compensation of delay uncertainty caused by power noise for a critical data path.

Technology (nm)	Critical data path				
	(T_{S1}, T_{H1}) (ps)	Frequency (GHz)	ΔT_D (ps)	(T_{S2}, T_{H2}) (ps)	Compensation (%)
180 nm	(110.5, 30.2)	1.5	57.3	(41,57)	100
		0.6	152.5	(41, 57)	45.6
90 nm	(79, 26.3)	3.2	23.7	(33,49)	100
		1.6	50.7	(33, 49)	90.7
65 nm	(67.9, 14.9)	4	21.2	(25.8, 26.3)	100
		2	47	(25.8, 26.3)	89.5
45 nm	(56.7, 9.2)	4.2	24.3	(15.4, 14.3)	100
		2.3	51.6	(15.4, 14.3)	80.1

Table 3: Compensation of delay uncertainty caused by power noise for a short path.

Technology (nm)	Short path			
	(T_{S1}, T_{H1}) (ps)	ΔT_D (ps)	(T_{S2}, T_{H2}) (ps)	Compensation (%)
180 nm	(110.5, 30.2)	17	(127.5, 7.1)	41.8
90 nm	(79, 26.3)	8.1	(87.1, 22.3)	50
65 nm	(67.9, 14.9)	5.9	(73.8, 13.4)	26.2
45 nm	(56.7, 9.2)	2.8	(59.5, 8.9)	10.7

path is 8.1 ps. The setup time can therefore be increased from 79 ps to 87.1 ps. The corresponding hold time is therefore reduced from 26.3 ps to 22.3 ps, as determined by (6), tolerating 4 ps of delay uncertainty. Since the variation in the delay of the data path is 8.1 ps, interdependence can compensate approximately 50% of the delay uncertainty of a short path. The results of this procedure for other technology nodes are listed in Tables 2 and 3 for, respectively, a worst case data path and a short path.

As listed in Table 2, delay uncertainty caused by power supply noise in a critical data path can be compensated by up to 100% at higher frequencies. At lower frequencies, more than 80% compensation is achieved in the more deeply scaled technologies. Alternatively, as listed in Table 3, for a short path, the compensation is lower due to the relatively smaller slope of the function $T_H = f(T_S)$ as compared to $T_S = f^{-1}(T_H)$, as illustrated in Fig. 7.

6. CONCLUSIONS

The efficacy of interdependence in reducing delay uncertainty is investigated for four CMOS technologies. The proposed approach provides enhanced understanding of the capabilities provided by setup-hold interdependence, thereby overcoming the limitations of only considering STA. A case study is presented where the efficacy of setup-hold interdependence in reducing delay uncertainty due to power supply noise is demonstrated.

7. REFERENCES

[1] D. Patel, "CHARMS: Characterization and Modeling System for Accurate Delay Prediction of ASIC Designs," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 9.5.1 - 9.5.6, May 1990.

[2] R. W. Phelps, "Advanced Library Characterization for High-Performance ASIC," *Proceedings of the IEEE International ASIC Conference*, pp. 15-3.1 - 15-3.4, September 1991.

[3] E. Salman, A. Dasdan, F. Taraporevala, K. Kucukcakar, and E. G. Friedman, "Exploiting Setup-Hold Time Interdependence in Static Timing Analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 6, pp. 1114–1125, June 2007.

[4] E. Salman, A. Dasdan, F. Taraporevala, K. Kucukcakar, and E. G. Friedman, "Pessimism Reduction in Static Timing Analysis Using Interdependent Setup-Hold Times," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 159–164, March 2006.

[5] S. Srivastava and J. Roychowdhury, "Independent and Interdependent Latch Setup/Hold Time Characterization via Newton-Raphson Solution and Euler Curve Tracking of State-Transition Equations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 27, No. 5, pp. 817–830, May 2008.

[6] S. Srivastava and J. Roychowdhury, "Interdependent Latch Setup/Hold Time Characterization via Euler-Newton Curve Tracing on State-Transition Equations," *Proceedings of the IEEE/ACM Design Automation Conference*, pp. 136–141, June 2001.

[7] S. Hatami, H. Abrishami, and M. Pedram, "Statistical Timing Analysis of Flip-Flops Considering Codependent Setup and Hold Times," *Proceedings of the IEEE/ACM Great Lakes Symposium on VLSI*, pp. 101–106, May 2008.

[8] V. Stojanovic and V. Oklobdzija, "Comparative Analysis of Master-Slave Latches and Flip-Flops for High-Performance and Low-Power Systems," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 4, pp. 536-548, April 1999.

[9] J. L. Neves and E. G. Friedman, "Optimal Clock Skew Scheduling Tolerant to Process Variations," *Proceedings of the IEEE/ACM Design Automation Conference*, pp. 623–628, June 1996.

[10] J. L. Neves and E. G. Friedman, "Design Methodology for Synthesizing Clock Distribution Networks Exploiting Non-Zero Clock Skew," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 4, No. 2, pp. 286–291, June 1996.

[11] "Predictive Technology Model (PTM)." [Online]. Available: http://www.eas.asu.edu/ ptm.

[12] IEEE Circuits and Systems Society, *Proceedings of the IEEE International Solid-State Circuits Conference*.