EFFECTIVE DISTANCE CALCULATIONS FOR
ON-CHIP DECOUPLING CAPACITORS IN
3-D INTEGRATED CIRCUITS

A Thesis Presented

by

Sateja Sunil Mungi

to

The Graduate School

in Partial Fulfillment of the

Requirements

for the Degree of

Master of Science

in

Electrical Engineering

Stony Brook University

May 2013

Stony Brook University

The Graduate School

Sateja Sunil Mungi

We, the thesis committee for the above candidate for the
Master of Science degree, hereby recommend
acceptance of this thesis.

Dr. Emre Salman - Thesis Advisor
Assistant Professor, Electrical and Computer Engineering Department

Dr. Milutin Stanacevic - Second Reader
Associate Professor, Electrical and Computer Engineering Department

This thesis is accepted by the Graduate School

Charles Taber
Interim Dean of the Graduate School

Abstract of the Thesis

Effective Distance Calculations for On-chip Decoupling Capacitors

In 3-D Integrated Circuits

by

Sateja Sunil Mungi

Master of Science

in

Electrical Engineering

Stony Brook University

2013

On-chip decoupling capacitors alleviate power supply noise at switching nodes
by supplying charge during switching activity. Concept of effective distance for
decoupling capacitors with a proposed ramp current model is presented. A closed-
form expression is derived for effective distance using the proposed model. Pro-
posed model is verified with SPICE simulations and shown to be more accurate than
the existing load current model. Analytical results are obtained for 2-D and 3-D ICs
with the proposed load current model to highlight the effect of different circuit pa-
rameters on effective distance. In 3-D ICs, effect of via-last and via-first/via-middle
TSV types is analyzed by modeling electrical characteristics of these TSVs. Elec-
trical models of via-last and via-first/via-middle TSVs are used to obtain analytical
results for effective distance. Via-last TSVs are shown to be superior than via-

first/via-middle TSVs since via-last TSVs do not rely on metal via stacks to ensure interplane communication. Via-last TSVs require, on average, 7.81% less decoupling capacitance than via-middle TSVs. Effect of number of TSVs, types of TSVs, resistance between decoupling capacitor and load, number of planes, resistance of alternative current path (only for via-first/via-middle TSVs) on effective distance is investigated. These results corroborate the concept of effective distance in 2-D and 3-D ICs which allows use of non-adjacent decoupling capacitors for switching loads. Due to vertical integration in 3-D ICs, effective distance permits the use of a properly sized decoupling capacitor located in one plane for a switching load located within a limited distance in another plane. This advantage leads to die area saving, less layout effort, reduced cost and time to market.

To my dear mother,
Swati Mungi
and
my dear husband,
Aditya Nirkhe.

Table of Contents

List of Figures

List of Tables

ACKNOWLEDGEMENTS

The journey of Masters degree has been full of experiences and learnings at Stony Brook University. I would like to thank everyone including faculty members, university staff and my friends who have been a part of it.

I wish to express my sincere thanks and gratitude towards my thesis advisor Dr. Emre Salman. He has always been there to guide, advice, and patiently answer even the simplest of the questions. His constant inspiration and valuable feedback enabled me stay focused on research. This research work would not have been possible without him as an advisor.

I would like to thank Dr. Milutin Stanacevic, second reader for the thesis for taking time to review and for making valuable suggestions.

I would also thank all fellow students at NanoCAS lab including Zhihua Gan, Hailang Wang, Ph.D candidates, and Peirong Ji. You have always been helpful when it came to discussing technical details, and solving queries related to different software issues.

I wish to take this opportunity to thank my husband, Aditya Nirkhe for his love, continuous support and encouragement. My mother who has been a great teacher for me, is the source of motivation and inspiration. I would like to thank my Mother, Mother-in-law, Sister and Brother-in-law for their encouragement and love.

Thank you.

Chapter 1

Introduction

Continuous feature-size scaling has brought several challenges that need to be alleviated using various creative and ingenious solutions. As we approach 14 nm technology node, and continue to scale down to 9 nm regime in the near future, a new trend of More-than-Moore is gaining popularity [1]. It refers to integration of a heterogeneous system in the same package using technologies such as system-in-package (SiP) and package-on-package (PoP) [2]. One key technology that allows heterogeneous integration of systems is three-dimensional (3-D) integration yielding 3-D ICs [3]. Figure 1.1 shows one such 3-D IC with different dies stacked together to act as a complete system. Term 3-D technology broadly refers to the family of technologies united by a common feature of vertical integration. These technologies include 3-D packaging, transistor build-up 3-D technology, and wafer-level 3-D integration compatible with back-end-of-line (BEOL) and front-end-of-line (FEOL) processes [2].

   3-D integration is an emerging technology that forms highly integrated systems by using a variety of materials and fabrication technologies to offer reduced power, higher integration density, reduced form factor, multi-functionality, high data bandwidth, high performance, increased yield and reliability at a reduced cost [2]. Expanded use of 3-D integration by allowing vertical stacking of dies is one of the promising solutions to continue achieving scaling advantages offered by Moore's
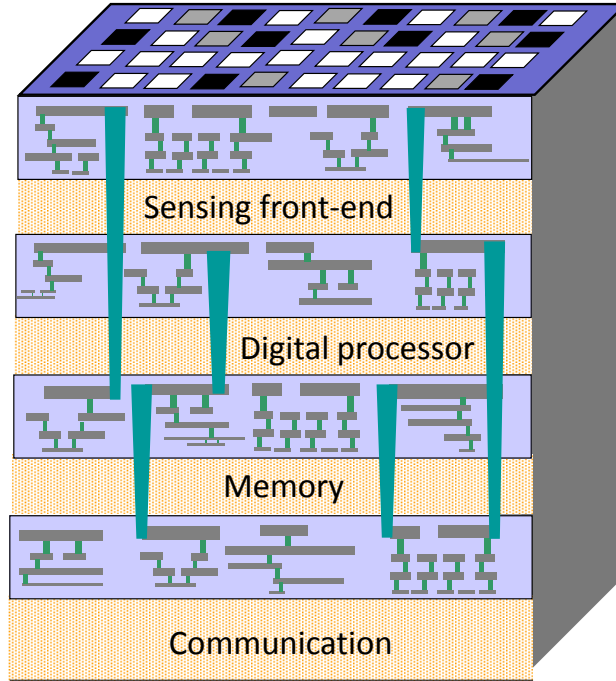
Figure 1.1: **Illustration of 3-D integration - vertical stacking of heterogenous planes**

law [1], [4].

Through silicon vias (TSVs) are the most important aspect of wafer level 3-D integration technology which penetrate through silicon substrate carrying power, ground, clock, and data signals from one plane to the other [2, 5]. TSVs exhibit different voltage drops and influence the noise behavior due to different fabrication processes and material properties. They act as vertical interconnect between different planes of dies conducting electrical signals and heat, and providing mechanical support to hold these dies in place. Figure 1.2 highlights the importance of TSVs in 3-D integration.

Similar to 2-D ICs, 3-D ICs face the challenge of efficient power delivery. There have been different topologies for on-chip power distribution networks that trade interconnect resources with resistive and inductive drop along the network, thereby affecting the overall reliability [7, 8]. Despite the several improvements in the design process of power distribution networks, they have important issues to over-
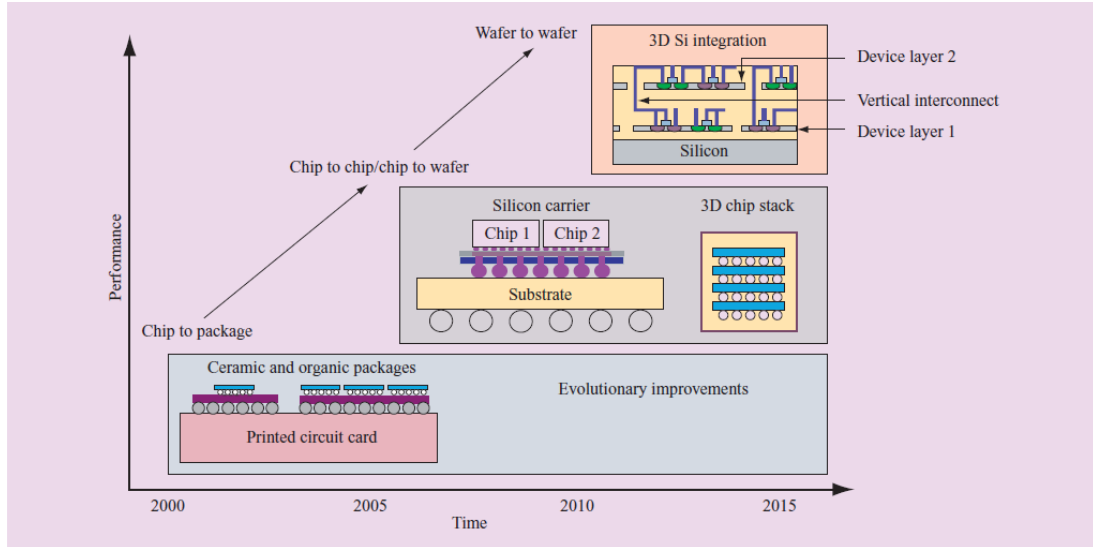
Figure 1.2: **3-D technology roadmap highlights the importance of TSVs which are marked as *Vertical Interconnect* providing electrical, thermal connectivity, and bonding between two device layers [6].**

come. Ongoing device and interconnect scaling adds to non-idealities and leads to increase in *IR* drop along the network. Reduced supply voltages, higher power density, large amount of simultaneously switching on-chip circuits, increasing coupling noise, and ever-increasing performance demand make the process of on-chip power distribution more challenging. To alleviate some of these issues, decoupling capacitors are used.

Decoupling capacitors have been used for decades to limit the power supply noise and improve signal/power integrity. Decoupling capacitors act as energy reservoir and provide charge to load circuit when the load circuit switches instantaneously. Hierarchical placement of decoupling capacitors on board level, package level, and chip level has been an effective solution to alleviate the strong trade-off between size and charge storage capacity of capacitors [7]. While acting as intermediate charge storages, decoupling capacitors also lead to parallel resonance with the upstream circuit which might increase impedance beyond the target impedance [7,8]. Furthermore, large on-chip decoupling capacitors occupy significant

3

chip area. These undesired features make it critical to size and place the decoupling capacitors as accurately as possible when deployed on-chip.

The topic of on-chip decoupling capacitance estimation and placement has been studied in detail. On-chip decoupling capacitance has been estimated in time and frequency domains [9]. Another algorithmic approach for sizing and placement of decoupling capacitors in [10] restricts decoupling capacitor placement in a row of standard cell. A floorplanning approach by [11] underestimates the decoupling capacitor budget when decoupling capacitor is not close, but at a certain distance from load. In [12], Popovich *et al.* have introduced effective radii based on target impedance, considering first or second dominant droop. Effective radii impose a restriction to place decoupling capacitors sufficiently close to switching load and power supply. Effective radius calculated by considering charge time, however, is not a closed-form equation. Another work by Wong *et al.* [13] uses network flow based algorithmic approach to improve effective distance calculation. However, only a pulse current model for load current is considered.

In 2-D integrated circuits, there exists a relationship between distance of load from decoupling capacitance and *IR* drop at the switching load as stated in [12], [13]. This relationship is essentially derived and validated when load and decoupling capacitance are in the same plane. For vertical integration in 3-D ICs, this relationship should be extended for non-planar distance between load and decoupling capacitor when both of them are not located in the same plane. Thus, vertical integration allows possible use of decoupling capacitors located in one plane for a load in adjacent plane.

In order to calculate the amount of decoupling capacitance required for a switching load, load current profile is studied and modeled. Effective distance is calculated on the basis of this current model. In [13], a basic model of current pulse has been assumed to derive effective distance. However, from observations, a model where current rises linearly to a peak value (such as a ramp signal) is more practical for on-chip load currents.

This work focuses on two aspects of decoupling capacitors: 1) improving load current model from a pulse to ramp current to derive improved effective distance,

2) extending effective distance from 2-D to 3-D ICs, evaluating different TSV technologies, and their influence on effective distance. These two aspects target at using optimal amount of decoupling capacitance for reducing power supply noise.

The rest of the thesis is organized as follows. Characteristics of prominent TSV types, their structures, on-chip power delivery and on-chip decoupling capacitors are described in Chapter 2. Chapter 3 explains the improved effective distance for 2-D integrated circuits using proposed ramp current model. Existing and proposed effective distance models are also compared in this chapter. Chapter 4 has models for 3-D integrated circuits and details about the results obtained by considering different TSV types, number of TSVs, and effect of these parameters on effective distance. Chapter 5 concludes the thesis.

Chapter 2

Background

TSVs are essential for electrical, thermal, and structural connectivity in wafer-level 3-D integration. In this chapter, TSV technologies and their physical and electrical characteristics are discussed. General on-chip power delivery and role of decoupling capacitors for efficient power distribution are also described.

2.1   TSV based 3-D integration

TSVs typically have high aspect ratio and are partially or completely filled with metallic substance for electrical and thermal conductivity. There have been numerous approaches to fabricate TSVs as mentioned in [6], [14], [15], [16], [17]. These approaches list a variety of filling materials such as copper, composite fill of copper and ceramic [6], tungsten, doped polysilicon [18], use of different physical structures such as cylindrical, tapered [19] and annular [18]. Also, depending upon the sequence of TSV formation, *i.e.* before FEOL, between FEOL and BEOL, and after BEOL, the process temperature which TSV material has to withstand, varies. Thus, TSV filling material employed in TSVs fabricated at different stages needs to possess certain thermal and mechanical properties. Depending on all of these factors mentioned above, there are primarily three types of TSVs: 1) *via-first*, 2) *via-middle*, and 3) *via-last*. Some important characteristics of these TSV types

Parameter	Via-first	Via-middle	Via-last
Filling material	Doped polysilicon	Tungsten/Copper	Copper
Structure	Cylindrical	Annular and conical/Cylindrical	Cylindrical
Aspect ratio AR	2.5:1	15:1-22:1	6:1
Diameter W	4 μm	4 μm to 2.66 μm	10 μm
Height H	10 μm	60 μm	60 μm
Pitch P	8 μm	8 μm to 9.34 μm	20 μm
Processing temperature	High	Average	Low
Formation	Before FEOL	Before BEOL	After BEOL
Landing metal	M_1	M_1	M_{Top}
Take-off metal	M_{Top}	M_{Top}	M_{Top}

Table 2.1: Characteristics of via-first, via-middle, and via-last TSVs [14], [15], [16], [18], [20], [21], [22], [23], [24], [25], [26]

are listed in Table 2.1. Figures 2.1(a) and (b) show representation of via-first/via-middle TSVs and via-last TSVs respectively. These TSV types are summarized in the following subsections.
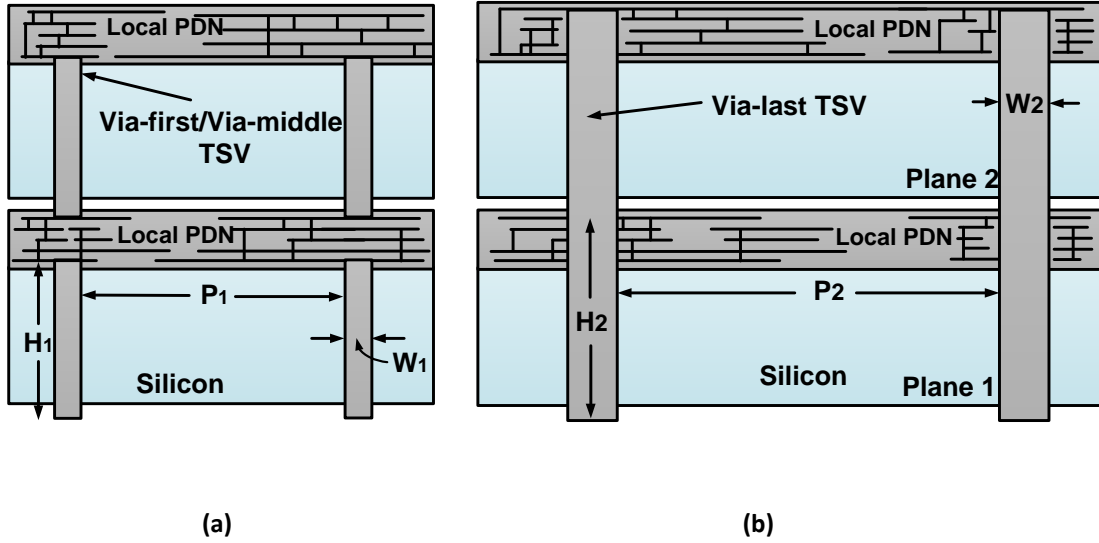
Figure 2.1: **Primary TSV technologies: (a) via-first/via-middle, (b) via-last [19]**

7

2.1.1 Via-first/Via-middle TSV

Despite the fabrication differences (such as via-first TSVs are formed before FEOL process, and via-middle TSVs are formed between FEOL and BEOL), there is a major common characteristic. Both via-first and via-middle TSVs connect the top-most metal layer and first metal layer within a plane. Thus, via-first and via-middle TSVs, from their electrical model view, are considered equivalent in this work. These two TSV types have comparable physical dimensions such as aspect ratio, height, width and pitch. Despite the difference in the resistivity of filling material in via-first and via-middle TSVs, they yield the same electrical model. Also note that, via-first and via-middle TSVs have alternative current paths to the devices, as shown in Figure 2.2(a).
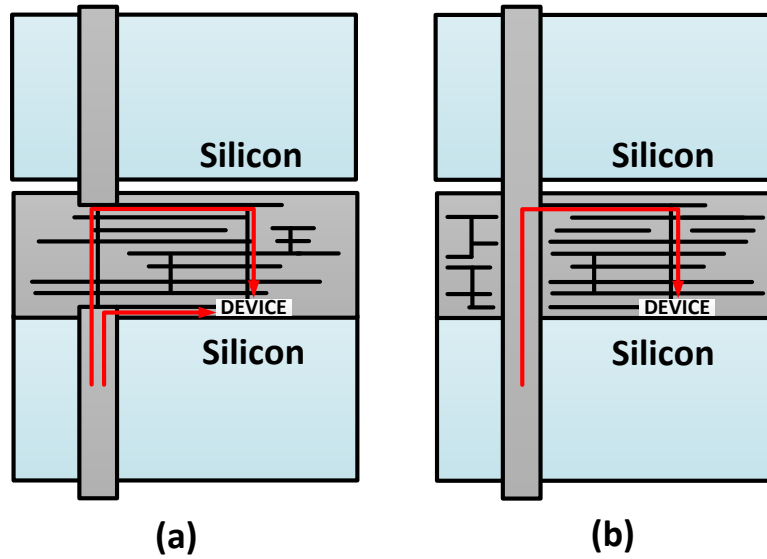
Figure 2.2: **(a) Alternative current paths in via-first/via-middle scheme, (b) only one electrical path for via-last TSV scheme [19].**

2.1.2 Via-last TSV

Via-last TSVs are fabricated after back-end-of-line (BEOL) process. Thus, they have to withstand less fabrication temperature, and have copper filling which gives the least resistance. However, via-last TSVs have higher inductance due to large physical dimensions. In this work, only resistive behavior is considered due to specific interest in effectiveness of decoupling capacitor affected by resistance. As shown in Figure 2.2(b), via-last TSVs do not have alternative current paths through the first metal layer.

2.2 Power Delivery in Integrated Circuits

Performance, size, and cost of any integrated circuit is greatly influenced by the power distribution system comprising of interconnect network and decoupling capacitors used at the board, package and chip levels [7]. Power distribution system is designed hierarchically due to the fact that power flows from outer level (PCB) to inner level (chip) of the system. Also, system design flow makes the specific power requirements clearer as the design progresses from coarse to fine level. In general, a power distribution system should satisfy impedance characteristics and power supply noise at each level. This requires the use of decoupling capacitors in a similar hierarchical fashion. A simple electrical model of a power distribution system is shown in Figure 2.3.

2.2.1 On-chip Power Distribution Networks

As there is a large number of non-uniformly switching circuits within a die, on-chip power distribution network (PDN) experiences significant variation in power dissipation across the chip area. This causes the voltage appearing across power and ground lines at different locations of the network to be non-uniform. This fact requires an on-chip power distribution network to be modeled as a two-dimensional mesh [7]. There are different topologies for on-chip power distribution networks
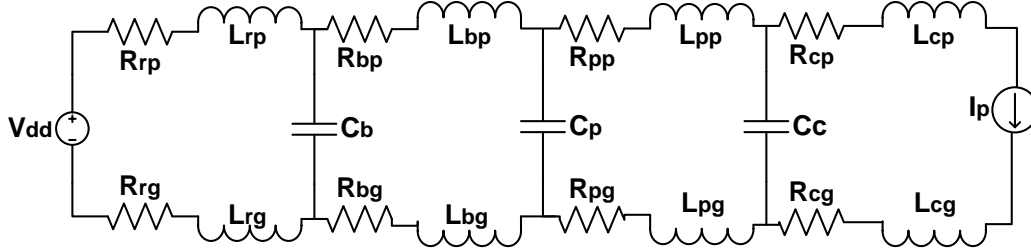
Figure 2.3: **Power distribution network with hierarchical placement of decoupling capacitors** C_b, C_p, C_c **at board, package, and chip level respectively [7]. Subscript** p **denotes parameters along power network and subscript** g **denotes the same along ground network.** R_r **and** L_r **are resistance and inductance at regulator level,** R_b **and** L_b **at board level,** R_p **and** L_p **at package level, and** R_c **and** L_c **at chip level.**

such as routed, mesh, grid structured, power and ground planes, and cascaded power/ground rings [1]. These styles can be classified into irregular and regular structures and play a major role in determining power integrity, power distribution resources, cost and effort required for the design of power distribution network, and the robustness of the on-chip circuit.
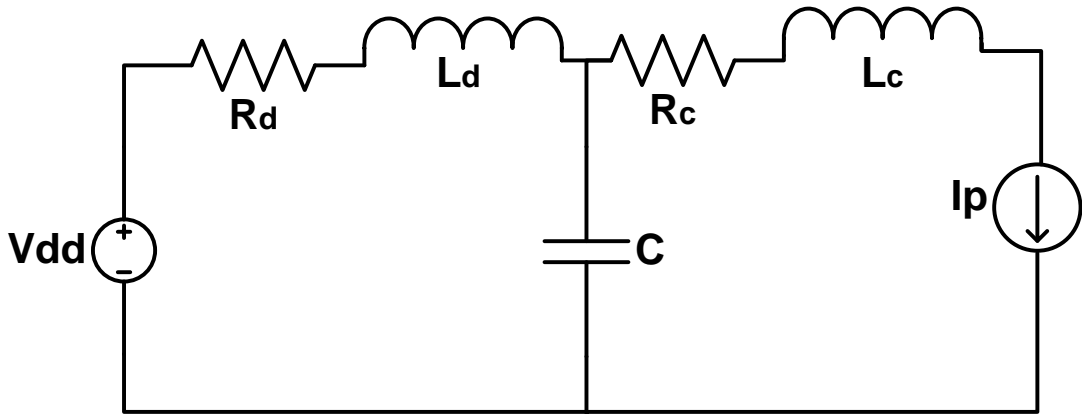
Figure 2.4: **Model of an on-chip power distribution network with decoupling capacitor** C

10

2.3 On-chip Decoupling Capacitance

Figure 2.4 shows a model of an on-chip power distribution network with decoupling capacitor C. Here, R_d and L_d are, respectively, the resistance and inductance between voltage source and decoupling capacitor. R_c and L_c are, respectively, the resistance and inductance between load and decoupling capacitor. Switching block (or load) is represented by current source. C is the on-chip decoupling capacitance that partially supplies current to load during switching to reduce power supply noise.

Decoupling capacitors are an integral part of a power distribution network. They are used to reduce power supply noise by acting as charge reservoirs. On-chip decoupling capacitors have traditionally been allocated into the white space available on die based on an unsystematic or *ad hoc* approach [10], [11].

This approach can place decoupling capacitor and switching block far apart which causes the decoupling capacitor to be ineffective. To make decoupling capacitors effective, they are forced to be over-sized. Else, it leads to an increase in power supply noise and degradation in power/signal integrity. A larger decoupling capacitance occupies more chip area. It also results in higher leakage power, reduced reliability, and higher cost [7]. Thus, decoupling capacitors should be placed sufficiently close to the load to have small and optimal values.

On the other hand, if a switching block is allowed to use a decoupling capacitor located nearby or only within the same row of a standard cell, this restriction creates another issue. On-chip decoupling capacitors are allocated to the white space after the layout is completed. Thus, if the nearby decoupling capacitor is not sufficient, this method would require creation of new white space adjacent to the block, which leads to modification of the entire layout. Moreover, effort spent for laying out those blocks is also sacrificed. If there is available white space that is located within a specific distance from the block (which is not necessarily adjacent to the block), it can be allocated to a decoupling capacitor for that block. Thus, by precise calculation of decoupling capacitance and its effective distance, rework effort for layout, wasted white space on-chip, cost, and additional time-to-market is avoided. This

work tries to highlight that a decoupling capacitor sized properly is effective even when it is physically located at a certain distance. This characteristic is important to exploit non-adjacent decoupling capacitance.

In 3-D ICs, a decoupling capacitor located in one plane can be useful for switching load in another plane if decoupling capacitor is large and sufficiently close. It would account for significant chip area saving where one die (plane) has sparsely distributed circuit and the other die (another plane) has densely packed circuits and cannot afford to undergo layout modification. Next chapter discusses sizing of decoupling capacitance and its maximum allowed distance from load, and effects of circuit parameters on these two criteria.

Chapter 3

Effective Distance for Decoupling Capacitors in 2-D ICs

In order to quantify effective distance and better understand the effects of different circuit parameters, a closed-form expression is developed, as described in this chapter.

For a circuit shown in Figure 3.1(a), R_c is the resistance between decoupling capacitance C and load, R_d is the resistance between decoupling capacitor and V_{dd}, where load is modeled with a linear current source in the form of a ramp signal, as shown in Figure 3.1(b). This ramp achieves a peak at the end of transition time t_r. Decoupling capacitor C discharges from $t = 0$ to $t = t_r$, while supplying current to the load modeled by a current source $I_L(t)$. Voltage across the load is denoted by $V_L(t)$. The power supply noise at the load should not exceed a limit and this limit is denoted by V_{tol}. V_{tol} is considered to be 5% of V_{dd} throughout this work. Decoupling capacitor C is responsible for keeping power supply noise below V_{tol}, even when $I_L(t)$ achieves its peak value I_p. In absence of R_c (when the on-chip decoupling capacitor C is located adjacent to the load), capacitor would supply current to the load when switching occurs and maintain the load voltage within limit. However, when decoupling capacitor C is located at some distance from the switching load and therefore *sees* resistance R_c, it has to overcome voltage drop

across R_c. This requires decoupling capacitance C to provide extra current and still maintain load voltage above $V_{dd} - V_{tol}$. This means that additional decoupling capacitance would be required to provide this extra current. Thus *effective distance* is the ratio of amount of decoupling capacitance required in the presence of R_c to the amount of decoupling capacitance required without R_c; having power supply noise constraint satisfied in both of these cases [13]. Thus, effective distance is defined as,

$$\text{Effective distance} = \frac{C(Rc)}{C(Rc = 0)} \ .$$

(3.1)
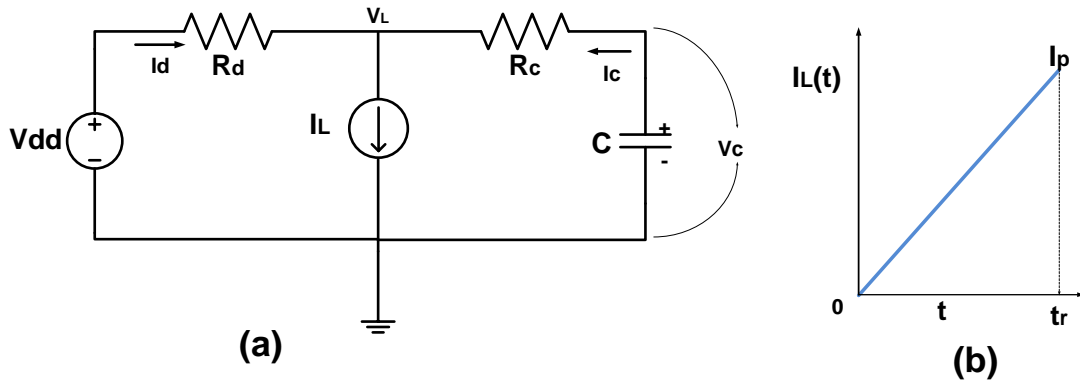
Figure 3.1: **(a) Circuit used for deriving effective distance, (b) switching load current modeled as ramp.**

3.1 Derivation for Effective Distance of a Decoupling Capacitor Based on Proposed Model

Effective distance in [13] is based on a pulse current model for load current. Proposed model uses ramp current to model the load, as shown in Figure 3.1(b). Detailed derivation to obtain a closed-form expression for effective distance using the proposed model is presented in this section. The current equations from circuit

14

diagram shown in Figure 3.1(a) are

$$I_c(t) = -C\frac{dV_c}{dt} \ , \tag{3.2}$$

when

$$I_L(t) = I_c(t) + I_d(t) \ , \tag{3.3}$$

wherein

$$I_L(t) = I_p\frac{t}{t_r} \ . \tag{3.4}$$

Using Kirchoff's voltage law for the circuit,

$$V_{dd} - I_d(t)R_d = V_L(t) \ , \tag{3.5}$$

and

$$V_L(t) + I_c(t)R_c = V_c(t) \ . \tag{3.6}$$

From (3.3) and (3.5)

$$V_L(t) = V_{dd} - I_L(t)R_d + I_c(t)R_d \ . \tag{3.7}$$

Thus, from (3.5) and (3.6),

$$V_{dd} - I_d(t)R_d + I_c(t)R_c = V_c(t) \ . \tag{3.8}$$

Substituting (3.3) in (3.8) gives

$$V_{dd} - I_L(t)R_d + I_c(t)(R_d + R_c) = V_c(t) \ . \tag{3.9}$$

Substituting (3.2) and (3.4) in (3.9) gives

$$V_{dd} - I_p(t)\frac{t}{t_r}R_d = V_c(t) + C\frac{dV_c(t)}{dt}(R_d + R_c) \ . \tag{3.10}$$

15

Solving differential equation (3.10) in $V_c(t)$ and applying initial condition, the result is

$$V_c(t) = V_{dd} - \frac{I_p(t)R_d}{t_r}[t - C(R_d + R_c)(1 + e^{\frac{-t}{C(R_d+R_c)}})] , \qquad (3.11)$$

and

$$I_c(t) = \frac{CI_p(t)R_d}{t_r}(1 - e^{\frac{-t}{C(R_d+R_c)}})] . \qquad (3.12)$$

Substituting (3.2), (3.4), and (3.12) in (3.7),

$$V_L(t) = V_{dd} + \frac{I_p(t)R_d}{t_r}[R_dC(1 - e^{\frac{-t}{C(R_d+R_c)}}) - t] . \qquad (3.13)$$

Re-arranging the terms in (3.13) yields

$$t + t_r\frac{V_L(t) - V_{dd}}{I_p(t)R_d} = R_dC(1 - e^{\frac{-t}{C(R_d+R_c)}}) . \qquad (3.14)$$

Applying Taylor's expansion [27] up to second order in (3.14) gives

$$t + t_r\frac{V_L(t) - V_{dd}}{I_p(t)R_d} = R_d[\frac{t}{R_d + R_c} - \frac{t^2}{C(R_d + R_c)^2}] . \qquad (3.15)$$

Re-arranging (3.15) to obtain a closed-form equation in C and substituting $V_L(t) = V_{dd} - V_{tol}$ yields

$$C = \frac{(R_d)^2 t^2 I_p(t)}{(R_d + R_c)t R_d^2 I_p(t) - (Rd + Rc)^2[tI_pR_d - t_rV_{tol}]} . \qquad (3.16)$$

From definition of effective distance in (3.1) and substituting $t = t_r$ since power supply noise reaches maximum when the load current reaches its peak value,

$$\text{Effective distance} = \frac{R_d^2 V_{tol}}{(R_d + R_c)^2 V_{tol} - (R_d + R_c)R_c V_{noise}} , \qquad (3.17)$$

16

where $V_{noise} = I_p.R_d$ is the noise voltage at the load in the absence of a decoupling capacitor. Equation (3.17) is in closed-form and provides a relationship between effective distance and electrical parameters of the circuit.

Here, another important characteristic of decoupling capacitor becomes evident. It is important for a decoupling capacitor to effectively overcome the voltage drop across the resistance along the path between decoupling capacitor C and load during switching. To do so, this resistance should be less than a certain value denoted by R_{max}. It is defined as [13]

$$R_{max} = \frac{R_d V_{tol}}{V_{noise} - V_{tol}}, \tag{3.18}$$

where $R_c < R_{max}$.

Total required decoupling capacitance is calculated from base decoupling capacitance and effective distance. Base decoupling capacitor C_{base} is the required capacitance when R_c is zero and is given by [13]

$$C_{base} = \frac{Q}{V_{tol}}, \tag{3.19}$$

$$Q = \int_0^{t_r} I_L t \, dt \tag{3.20}$$

Thus, from (3.4), (3.20) and substituting $t = t_r$,

$$Q = \frac{I_p t_r}{2}. \tag{3.21}$$

Hence, substituting (3.21) in (3.19),

$$C_{base} = \frac{I_p t_r}{2V_{tol}}. \tag{3.22}$$

17

R_c in Ω	Calculated E.D	Simulated V(t) in mV at calculated E.D	Simulated E.D	Percent error in E.D
0.1	1.042	957.3563	0.75	38.93
0.15	1.099	955.311	0.83	32.41
0.2	1.19	953.6971	0.95	25.26
0.25	1.333	952.4507	1.15	15.91
0.3	1.562	951.5018	1.35	15.70
0.35	1.961	950.8147	1.8	8.94
0.4	2.778	950.3468	2.6	6.85
0.45	5.263	950.0831	5.2	1.21
0.48	12.76	950.0129	12.7	0.47
0.49	25.25	950.0028	25.2	0.19
0.5	∞	NA	NA	NA

Table 3.1: Validation of effective distance calculations with SPICE

Total required decoupling capacitance C is

$$C = \text{Effective distance (E.D) x } C_{base} . \qquad (3.23)$$

Equations (3.17), (3.18), (3.22), and (3.23) determine the *effectiveness* of a decoupling capacitor along a 2-D IC.

Effectiveness of decoupling capacitors given by (3.17), (3.18), (3.22), and (3.23) is verified using SPICE simulations, when $V_{tol} = 50\ mV$, $V_{dd} = 1\ V$, $I_p = 200\ mA$, $t_r = 50\ pS$ and $R_d = 0.5\ \Omega$ for a circuit shown in Figure 3.1(a). Here, $V_{noise} = 100\ mV$, $R_{max} = 0.5\ \Omega$, and $C_{base} = 100\ pF$ are obtained from calculations. Table 3.1 shows different R_c values, calculated effective distance from (3.17), simulated V(t) at calculated effective distance using SPICE and simulated effective distance, also using SPICE. From the table, noise voltage at the load is always within the tolerable limit of 50 mV for all possible values of R_c. Average error in calculation of effective distance is 14.59%.

Figure 3.2 shows the plot of calculated and simulated effective distance. From Table 3.1, for $R_c = 0.2\ \Omega$, observed effective distance is 0.95 and calculated effective distance is 1.19. However, as R_c approaches R_{max}, calculated effective distance values are sufficiently close to simulated effective distance values, as seen for R_c values of 0.48 Ω and 0.49 Ω. As also seen in Figure 3.2, there is a slight overesti-

mation of effective distance for smaller values of R_c. It should be noted here that at $R_c = R_{max} = 0.5\ \Omega$, calculated effective distance value is unreasonably large, and simulated effective distance is also unreasonably large. Base decoupling capacitor value from simulations is $C_{base} = 62.78\ pF$, which is the total required decoupling capacitance when R_c is zero.
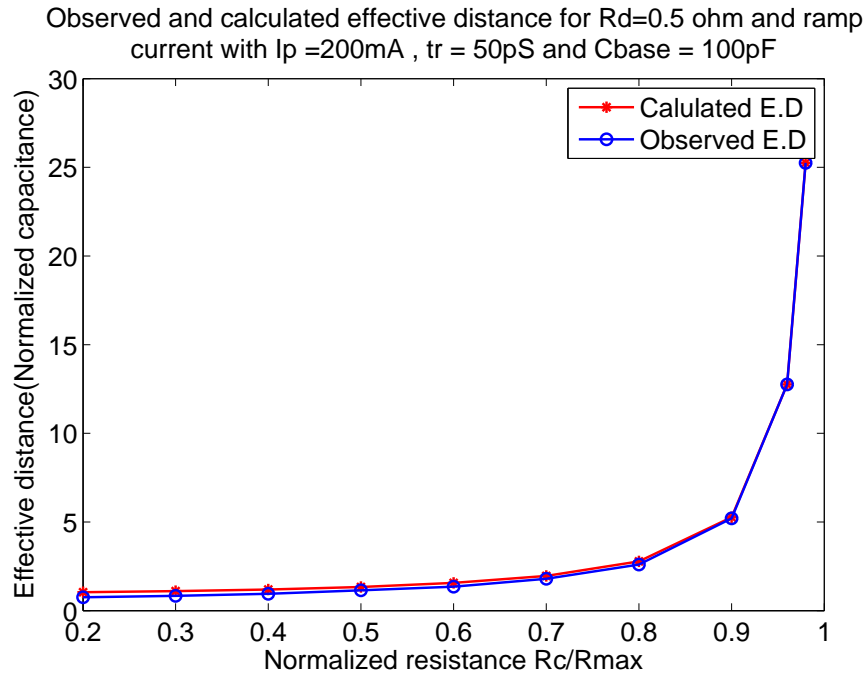
Figure 3.2: **Calculated and simulated effective distance for** $V_{tol} = 50\ mV$**,** $V_{dd} = 1\ V$**,** $I_p = 200\ mA$**,** $t_r = 50\ pS$**, and** $R_d = 0.5\ \Omega$**.**

3.2   Comparison of Existing Model and Proposed Model for Effective Distance of Decoupling Capacitors

The proposed model of effective distance presented in this work is compared with the existing model in [13]. Existing model assumes load current to be a pulse with a constant value of $I_h = 200\ mA$, whereas the proposed model assumes ramp current

19

model with a peak value of $I_p = 200 \, mA$ as given by (3.17). Rise time and duration of pulse are required only for base decoupling capacitor C_{base} calculation. Hence, effective distance calculation is independent of the duration of current irrespective of the type of model. Total decoupling capacitance, however, depends upon pulse duration (for the existing model) or rise time (for the proposed model), since base decoupling capacitance is determined by pulse duration or rise time.

Resistance between power supply and decoupling capacitor R_d is 0.5 Ω. At R_c/R_{max} of 0.3, 0.5, and 0.8, the error in calculated effective distance is 32.41%, 15.91%, and 6.85% respectively. Figure 3.3 shows the comparison of calculated effective distance using existing pulse current model and proposed ramp current model. According to this this plot, existing model overestimates the effective distance towards larger values of R_c. As described before, towards higher values of R_c, effective distance increases exponentially. Thus, overestimation of decoupling capacitance would create significant and unnecessary increase in the area. However, as seen from Figure 3.2, proposed model more precisely estimates required decoupling capacitance when R_c values are higher, and close to R_{max}. The existing model overestimates effective distance when compared to proposed model, by 12.65%, 20.48% and 31.57% for R_c/R_{max} values of 0.3, 0.5 and 0.8 respectively. Thus, proposed model achieves enhanced performance by more accurately estimating the required decoupling capacitance compared to existing model.
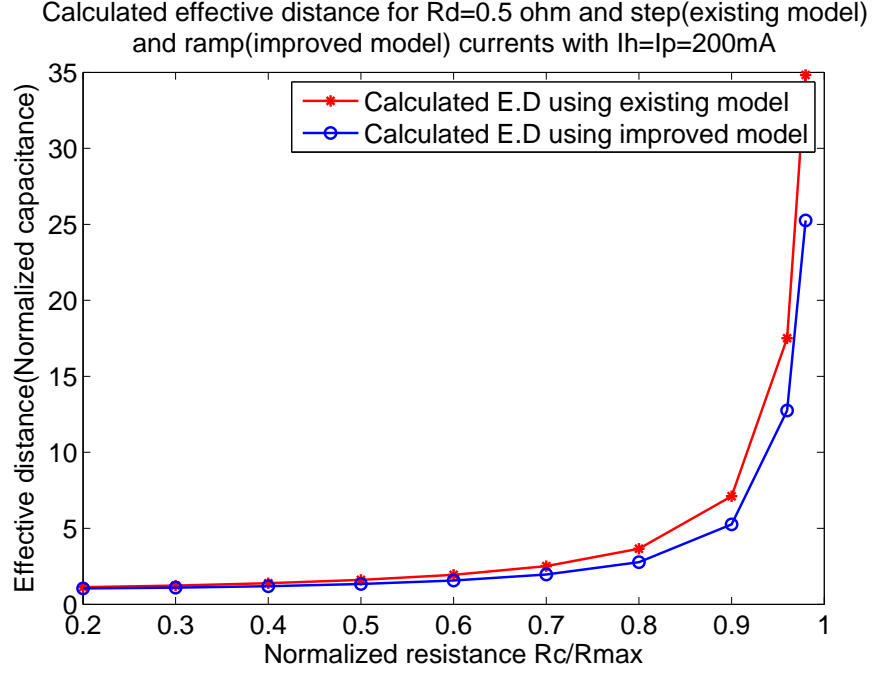
Figure 3.3: **Comparison of existing and proposed effective distance model for** $I_h = I_p = 200 \, mA$ **and** $R_d = 0.5 \, \Omega$**.**

3.3 Effect of Circuit Parameters on Effective Distance of a Decoupling Capacitor

For the circuit shown in Figure 3.1(a), analytical results are obtained using a ramp load current shown in Figure 3.1(b) with a peak value $I_p = 100 \, mA$, $t_r = 50 \, pS$, and $V_{dd} = 1V$. Effect of R_d and V_{tol} for a range of R_c is analyzed in this section. In addition, these analytical results obtained from the proposed model are verified using SPICE simulations, demonstrating reasonable accuracy.

3.3.1 Effect of R_d on Effective Distance

R_d signifies the resistance between voltage source and decoupling capacitor, so more the R_d, less is the R_{max}, more is the decoupling capacitance required and

higher is the effective distance predicted from (3.17) and (3.18). Here, noise toler-
ance is constant at 50 mV for all values of R_d.
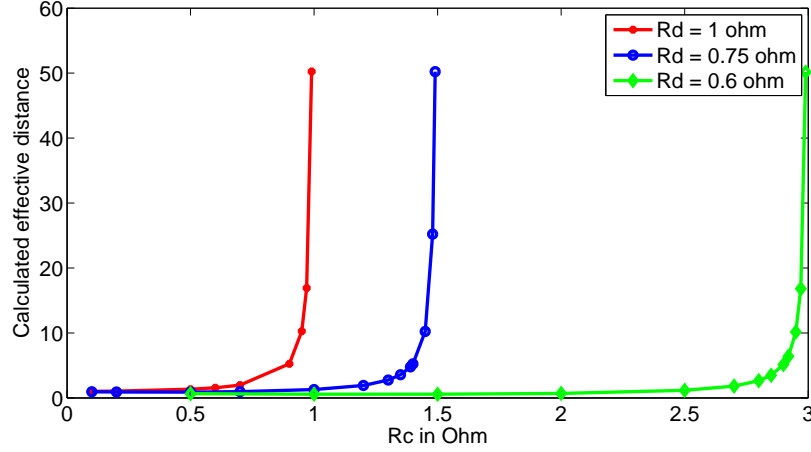
Figure 3.4: **Effect of variation in R_d on effective distance for $V_{tol} = 50mV$, $V_{dd} = 1V$, $I_p = 100mA$, and $t_r = 50pS$.**

As seen from Figure 3.4, higher values of R_d require higher effective distance
for the same value of R_c. For example, for $R_c = 0.5\ \Omega$, effective distance with R_d
equal to 0.6 Ω, 0.75 Ω, and 1 Ω is 0.65, 0.9, and 1.33 respectively.

3.3.2   Effect of V_{tol} on Effective Distance

Higher noise tolerance limit V_{tol} allows R_{max} to increase, permitting a larger range
of R_c values. For the same R_c, increased V_{tol} requires less decoupling capacitance.
This is equivalent to a smaller effective distance as seen from (3.17) and (3.18). As
shown in Figure 3.5, for a constant R_c of 0.2 Ω, if V_{tol} increases from 25 mV to 50
mV, and to 75 mV, effective distance decreases from 2.083 to 1.042, and to 0.8929
respectively. Thus, expected effect of V_{tol} on effective distance is verified.
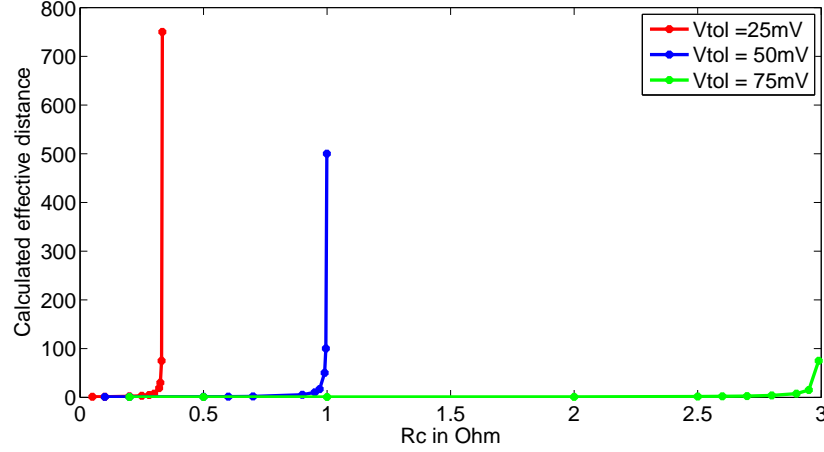
Figure 3.5: **Effect of variation in V_{tol} on effective distance for $V_{dd} = 1V$, $I_p = 100mA$, $R_d = 1\Omega$,** $t_r = 50pS$**.**

3.3.3 Combined effect of R_d and I_p on Effective Distance

From (3.17), effective distance depends on R_d, V_{tol} and V_{noise}. Figures 3.4 and 3.5 show the dependence of effective distance on R_d and V_{tol} respectively, when the remaining parameters are constant. Load voltage in the absence of a decoupling capacitor is given by V_{noise}, where V_{noise} is a product of R_d and I_p. Thus, it is interesting to see the simultaneous effect of R_d and I_p on effective distance. Figure 3.6 shows a plot that describes the effect of R_d and I_p simultaneously on effective distance. Effective distance increases when R_d or I_p increase, or both of these parameters increase simultaneously. For example, for $I_p = 230\,mA$ and $R_d = 0.7\,\Omega$, effective distance is 2.217. When I_p remains constant at 230 mA and R_d increases to 1.4 Ω, effective distance increases to 3.926. Alternatively, when R_d is kept constant at 0.7 Ω and I_p increases from 230 mA to 270 mA, effective distance becomes 3.781. When both R_d and I_p are high such as 1.4 Ω and 270 mA respectively, effective distance increases to 13.92.

From (3.18), R_{max} depends on R_d and V_{noise}. Thus, for higher values of R_d and I_p, there is a decrease in R_{max}. As mentioned earlier, R_c should be less than R_{max}. Hence, on this plot, the points where R_c exceeds R_{max}, effective distance is

considered to be zero. Therefore, there is a break in the graph creating two spikes in the region of highest values of R_d and I_p. For example, for $I_p = 280 \, mA$ and $R_d = 1.4 \, \Omega$, R_c exceeds R_{max}, and decoupling capacitor becomes ineffective, as indicated by the break in Figure 3.6.
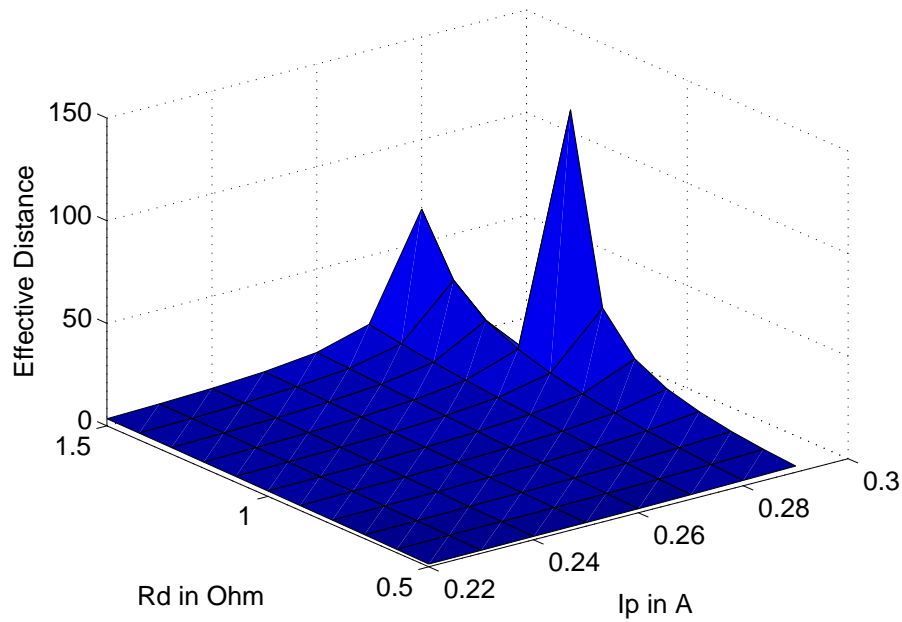
Figure 3.6: **Effect of variation in R_d & I_p on effective distance for $V_{dd} = 1V$, $R_c = 0.2 \, \Omega$, $V_{tol} = 50 \, mV$.**

Various aspects of proposed effective distance model have been discussed in this chapter. This model is extended to 3-D integrated circuits in the next chapter. As 3-D ICs include TSVs, characteristics of TSVs are modeled and included to apply the proposed effective distance model for decoupling capacitance calculations in 3-D ICs.

Chapter 4

Application of Effective Distance to 3-D Integrated Circuits

Vertical stacking of multiple silicon wafers is possible due to 3-D integration. Electrical connectivity between different layers is achieved with the help of high aspect ratio TSVs, as described in Chapter 2. In this chapter, effect of TSVs and their electrical characteristics on required decoupling capacitance is emphasized. The electrical effects of different types of TSVs are presented in the form of equivalent electrical circuits. Effective distance introduced and derived in the previous chapter is extended from 2-D to 3-D integrated circuits. Results obtained for 3-D integrated circuits are summarized in this chapter. These results verify the idea of *effective distance* for decoupling capacitors in 3-D ICs.

4.1   Electrical Model for Via-first/Via-middle TSVs

As mentioned in Chapter 2, electrical characteristics of via-middle and via-first TSVs are considered to be identical since their connectivity with local metal layers is similar. Figure 4.1 shows electrical model for via-middle/via-first TSV. This model considers three planes of vertically stacked wafers connected using TSVs and supplied with the power and ground voltages at the bottom plane. Via-first and

Figure 4.1: **Electrical model for via-first/via-middle TSV, and power distribution network**

via-middle TSVs start from the topmost metal layer of nth plane and end at the first metal layer of the $(n+1)^{th}$ plane. Hence, they are represented by resistance R_{TSV} between topmost metal layer of nth plane and the first metal of $n+1^{th}$ plane. The effective resistance of a number of TSVs connected in parallel is denoted by $R_{TSV}^{effective}$. A stack of metal vias exists from first metal layer to the topmost metal layer of any plane to deliver power. Resistance due to the stack of metal vias is denoted by $R_{vertical}$. Via-middle/via-first TSVs have alternative power distribution paths within a plane (parallel to $R_{vertical}$). R_{M1} is the resistance of metal interconnect along this alternative current path in the bottommost (first) metal layer. Resistance of the local power distribution network is denoted by R_{local}^{PDN}. Power and ground pads are assumed to be at the bottom of 3-D stack and are represented by voltage source V_{dd} and ground respectively. Since power and ground pads are connected to the package, package resistance $R_{package}$ is also considered in the model. The switching block (load circuit) is modeled as current source I_L. A decoupling capacitor C is connected across each load with a resistance of R_c. This model considers resistive characteristics of TSVs while ignoring capacitive coupling into the substrate.

4.2   Electrical Model for Via-last TSV

The electrical model shown in Figure 4.2 is for three planes of vertically stacked wafers connected using via-last TSVs where the power and ground pads are located at the bottom. Via-last TSVs connect the topmost metal layers of two adjacent planes. Power is distributed from the topmost metal layer in every plane to lower metal layers using local power distribution network within the plane. Resistance of this local power distribution network is given by R_{local}^{PDN}. There are no alternative current paths in via-last TSV configuration. Hence, R_{M1} resistance seen for via-middle TSVs does not exist in this case. $R_{TSV}^{effective}$ is the effective resistance of a number of via-last TSVs connected in parallel. Decoupling capacitor C is located at a certain distance from the load, and this distance is modeled by resistance R_c. Power and ground are represented by a voltage source V_{dd} and ground at the bottom plane.
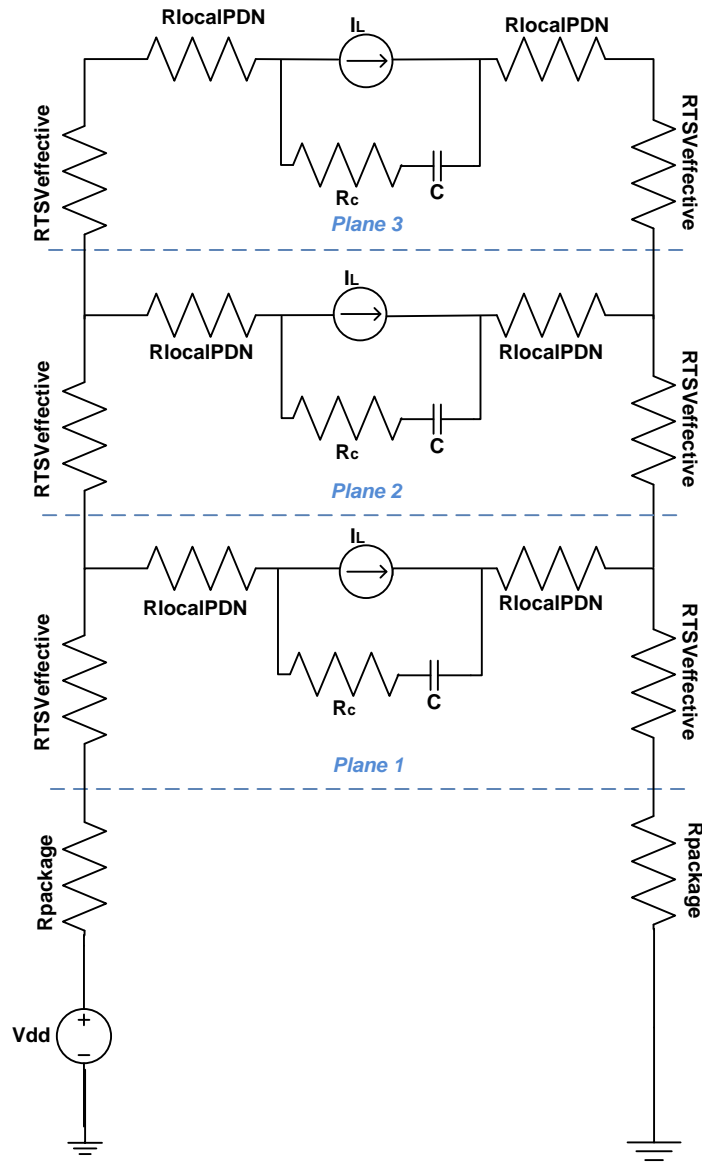
Figure 4.2: **Electrical model for via-last TSV, and power distribution network**

Package resistance is represented by $R_{package}$. The switching block is modeled by current source I_L.

This model considers only resistive characteristics of TSVs. TSV inductance and capacitance are not considered, as they make the effective distance expression transcendental. The primary objective in this work is to obtain a closed-form expression for the effective distance with a more realistic supply current waveform modeled as a ramp function, and apply this model to 3-D ICs.

4.3 Approach for Using Electrical Models of TSVs

In order to use models shown in Figures 4.1 and 4.2 for effective distance calculation, it is required to express R_c and R_d in terms of circuit parameters of Figures 4.1 and 4.2. This is done for every plane shown in Figures 4.1 and 4.2. Here, R_d^1 is the resistance from power source V_{dd} to the decoupling capacitor C located in the first plane. R_c^1 is the resistance between decoupling capacitor C and the load I_L in the first plane. R_{max}^1 gives the maximum value of R_c allowed using *effective distance* formula. V_{noise}^1 is the noise voltage across switching load in plane one. Similarly, parameters are defined for other planes, where the superscript determines the plane number.

The load characteristics are assumed to be the same throughout all the planes of model. This includes the rise time of load current t_r, peak value of the load current I_p, and tolerable noise voltage across the load V_{tol}. Since load current is the same for all planes, base decoupling capacitor C_{base} is identical across all the planes. $V_{dd} = 1\,V$, $V_{tol} = 5\%$ of $V_{dd} = 50\,mV$, $t_r = 50\,pS$, $R_{package} = 3\,m\Omega$ are assumed to be constant across all the simulations for all types of TSVs.

4.3.1 Via-middle TSVs

Resistance of each copper-filled via-middle TSV is considered to be 80 $m\Omega$ [19]. Hence,

$$R_{TSV}^{effective} = \frac{80\ m\Omega}{n}\ ,\qquad (4.1)$$

where n is the number of TSVs.

A peak power density of 250 W/cm^2 at 1 V is assumed [28]. Thus, for a die area of 1mm x 1mm, the peak load current I_p is equal to 2.5 A, and target resistance of local power distribution network should be 20 $m\Omega$, assuming 50 mV of tolerable noise. Hence R_{local}^{PDN} that consists of decoupling capacitors in addition to the rest of the network resources is considered to be in the range of tens of mΩ, such as 50 $m\Omega$. As the first metal layer that connects the devices in on-chip circuit is highly resistive, resistance of first metal layer interconnect R_{M1} is assumed to be $20R_{local}^{PDN}$, equal to 1 Ω. Calculation of $R_{vertical}$ requires a different approach. Since $R_{vertical}$ represents the resistance of metal vias from the first metal layer to the topmost metal layer within a plane, we need to find how many such metal vias are present in the area formed by the width of n such TSVs, as shown in Figure 4.3.

TSVs are cylindrical in shape. A via-middle TSV has a diameter of 4 μm, and pitch of 8 μm. Each TSV is surrounded by a minimum space of 2 μm (keep out zone) when the TSVs are closely packed in an area [19]. Metal vias have dimensions of 2λ x 2λ and they are surrounded by a minimum spacing of λ on a densely packed array of vias [29]. Figure 4.4 illustrates these details. Here, λ is half of the feature size and is determined by the technology.

Number of metal vias can be calculated from the area occupied by via-middle TSVs. Thus, a single via-middle TSV area is the same as the area occupied by $\frac{8\mu m\ x\ 8\mu m}{4\lambda\ x\ 4\lambda}$ number of metal vias. This yields the total number of metal vias stacks present in the area occupied by one via-middle TSV.

Hence $R_{vertical}$ is formulated as,

$$R_{vertical} = \frac{R[\text{single stack of metal vias (M1-top metal layer)}]}{\text{total number of metal via stacks in area occupied by TSVs}}\qquad (4.2)$$
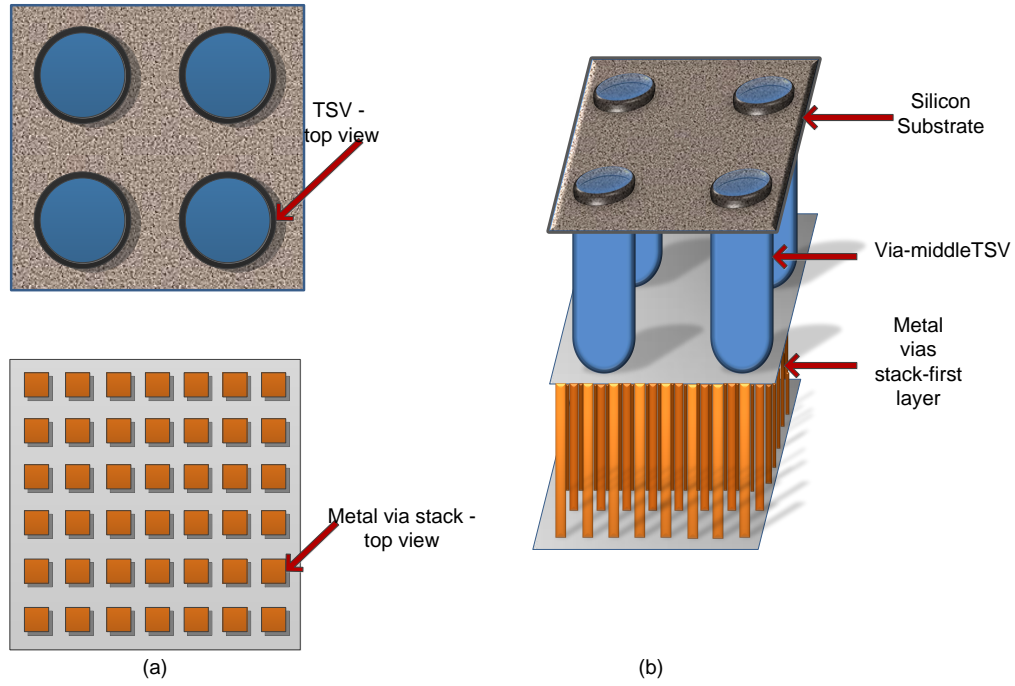
Figure 4.3: **Representation of via-middle TSV and stack of metal vias: (a) Top view of TSVs and stack of metal via shown separately, (b) side view of TSVs and stack of metal via.**
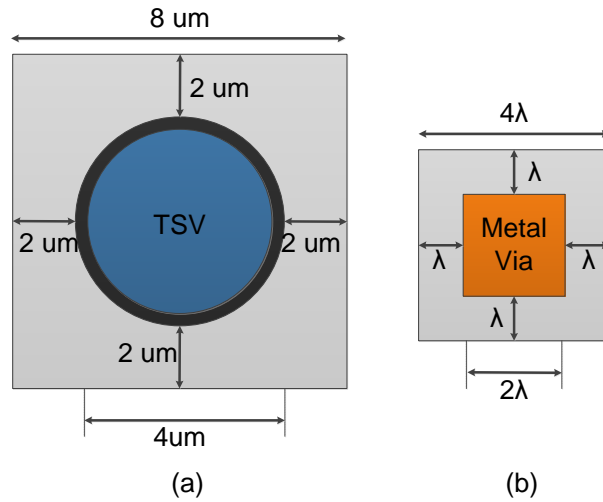

Figure 4.4: **Physical dimensions of (a) via-middle TSV, (b)metal via.**

Here R[single stack of metal vias (M1-top metal layer)] is assumed to be 12.4 Ω. For a 130 nm technology

$$R_{vertical} = \frac{12.4}{\frac{8\mu m \ x \ 8\mu m}{4x65nm \ x \ 4x65nm \ x \ n}} = \frac{12.4}{947 \ x \ n} \ , \tag{4.3}$$

where n is the number of via-middle TSVs.

As seen in Figure 4.1, there are several delta networks present on the model that consist of $R_{vertical}$, $R_{localPDN}$, and R_{M1}. These delta networks are converted to Y networks with equivalent resistances, as shown in Figure 4.5. The simplified model replaces $R_{vertical}$, R_{local}^{PDN}, and R_{M1} with their corresponding Y equivalents R_1, R_2 and R_3 where

$$R_1 = \frac{R_{vertical}.R_{local}^{PDN}}{R_{vertical} + R_{local}^{PDN} + R_{M1}} \ , \tag{4.4}$$

$$R_2 = \frac{R_{vertical}.R_{M1}}{R_{vertical} + R_{local}^{PDN} + R_{M1}} \ , \tag{4.5}$$

$$R_3 = \frac{R_{local}^{PDN}.R_{M1}}{R_{vertical} + R_{local}^{PDN} + R_{M1}}. \tag{4.6}$$
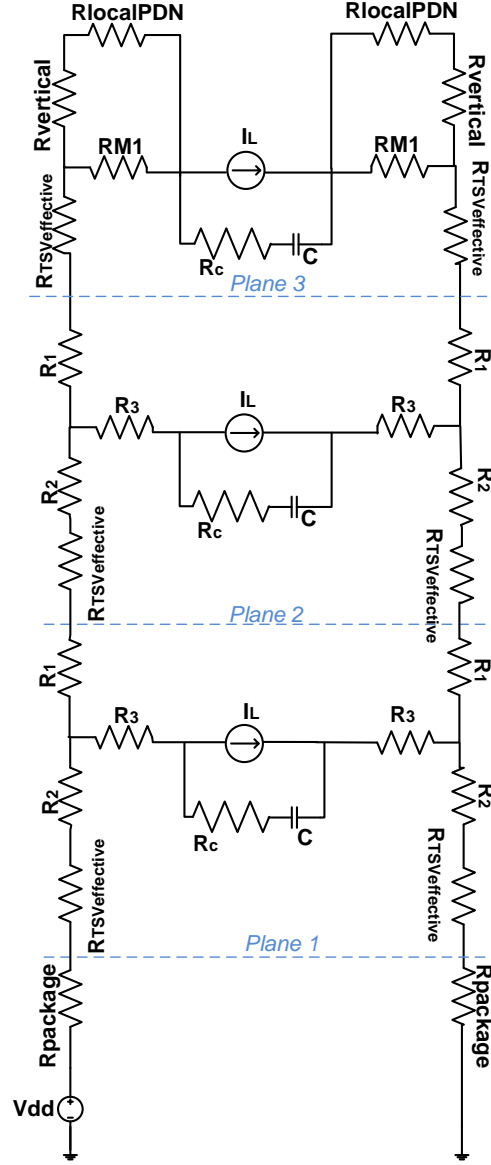
Figure 4.5: **Equivalent electrical model for via-first/via-middle TSV and power distribution network obtained after conversion of Δ networks in Figure 4.1 to Y networks**

From the definition of R_d as the resistance between power supply and decoupling capacitor, following equations are obtained for all of the planes.

$$R_d^1 = R_{package} + R_{TSV}^{effective} + R_2 + R_3 \, , \tag{4.7}$$

$$R_d^2 = R_{package} + 2.R_{TSV}^{effective} + 2.R_2 + R_1 + R_3 \,, \qquad (4.8)$$

$$R_d^3 = R_{package} + 3.R_{TSV}^{effective} + 2.R_2 + 2.R_1 + [(R_{vertical} + R_{local}^{PDN})//R_{M1}] \,. \qquad (4.9)$$

Since current flowing into the topmost plane is supplied by source at the bottom (power pad), current flowing through TSVs located between plane one and plane two is equal to sum of all planar currents. Thus, noise voltage calculation is achieved by taking such currents into consideration,

$$V_{noise}^1 = (R_{package} + R_{TSV}^{effective} + R_2).3I_p + R_3.I_p \,, \qquad (4.10)$$

$$V_{noise}^2 = (R_{package} + R_{TSV}^{effective} + R_2).3I_p + (R_1 + R_{TSV}^{effective} + R_2).2I_p + R_3.I_p \,, \qquad (4.11)$$

$$V_{noise}^3 = (R_{package} + R_{TSV}^{effective} + R_2).3I_p + (R_1 + R_{TSV}^{effective} + R_2).2I_p +$$
$$(R_1 + R_{TSV}^{effective} + [(R_{vertical} + R_{local}^{PDN})//R_{M1}]).I_p \,. \qquad (4.12)$$

Maximum value for R_c defined as the resistance between load and decoupling capacitor in each plane is

$$R_{max}^1 = \frac{R_d^1.V_{tol}}{V_{noise}^1 - V_{tol}} \,, \qquad (4.13)$$

$$R_{max}^2 = \frac{R_d^2.V_{tol}}{V_{noise}^2 - V_{tol}} \,, \qquad (4.14)$$

$$R_{max}^3 = \frac{R_d^3.V_{tol}}{V_{noise}^3 - V_{tol}} \,. \qquad (4.15)$$

Note that the numerical superscript indicates the plane number.

4.3.2 Via-last TSVs

Resistance of each via-last TSV is assumed to be 20 $m\Omega$ [19]. Hence, when n via-last TSVs are used,

$$R_{TSV}^{effective} = \frac{20\ m\Omega}{n}. \tag{4.16}$$

Here, R_{local}^{PDN} is assumed to be 50 $m\Omega$. Peak value of load current I_p is 2.5 A. From the definition of R_d as the resistance between power supply and decoupling capacitor, following equations are obtained for all the planes

$$R_d^1 = R_{package} + R_{TSV}^{effective} + R_{local}^{PDN}, \tag{4.17}$$

$$R_d^2 = R_{package} + 2.R_{TSV}^{effective} + R_{local}^{PDN}, \tag{4.18}$$

$$R_d^3 = R_{package} + 3.R_{TSV}^{effective} + R_{local}^{PDN}. \tag{4.19}$$

Since current flowing into the topmost plane is supplied by source at the bottom plane (power pad), current flowing through TSVs located between plane one and plane two is equal to sum of all planar currents. Thus, noise voltage calculation is achieved by taking such currents into consideration,

$$V_{noise}^1 = (R_{package} + R_{TSV}^{effective}).3I_p + R_{local}^{PDN}.I_p, \tag{4.20}$$

$$V_{noise}^2 = (R_{package} + R_{TSV}^{effective}).3I_p + R_{TSV}^{effective}.2I_p + R_{local}^{PDN}.I_p, \tag{4.21}$$

$$V_{noise}^3 = (R_{package} + R_{TSV}^{effective}).3I_p + R_{TSV}^{effective}.2I_p + (R_{TSV}^{effective} + R_{local}^{PDN}).I_p. \tag{4.22}$$

Maximum value for R_c defined as the resistance between load and decoupling capacitor in each plane is

$$R_{max}^1 = \frac{R_d^1.V_{tol}}{V_{noise}^1 - V_{tol}}, \tag{4.23}$$

$$R_{max}^2 = \frac{R_d^2.V_{tol}}{V_{noise}^2 - V_{tol}}, \tag{4.24}$$

$$R^3_{max} = \frac{R^3_d . V_{tol}}{V^3_{noise} - V_{tol}}. \tag{4.25}$$

4.4 Analytical Results for Via-middle and Via-last TSVs

This section shows the anlytical results obtained with the help of equations listed in Sections 4.3.1 and 4.3.2.

4.4.1 Via-middle TSVs- Effect of $R_{vertical}$ and number of TSVs

Figures 4.6, 4.7 and 4.8 show the effect of $R_{vertical}$ on effective distance for plane one, two and three respectively. Identical values of $R_c = 6 \ m\Omega$, $I_p = 2.5 \ A$, $t_r = 50 \ pS$ and base capacitor $C_{base} = 1.25 \ nF$ are used.

As predicted, the higher the number of TSVs used in parallel, the less the effective TSV resistance. Hence, less decoupling capacitance is required. From Figure 4.6 for plane one and $R_{vertical} = 30 \ m\Omega$, ten TSVs need $1.879C_{base}$, whereas 50 TSVs require $1.755C_{base}$. The ratio of effective distance for ten TSVs to effective distance for 50 TSVs is 1.07 for plane one and $R_{vertical} = 30 \ m\Omega$. For plane two in Figure 4.7, increasing number of TSVs from 10 to 50 reduces the effective distance from 2.039 to 1.923 when $R_{vertical} = 30 \ m\Omega$. The ratio of effective distance for ten TSVs to 50 TSVs is 1.06 for plane two when $R_{vertical} = 30 \ m\Omega$. Similarly, for plane three, for $R_{vertical} = 30 \ m\Omega$, ten TSVs need $1.847C_{base}$, whereas 50 TSVs require $1.781C_{base}$. The ratio of effective distance for ten TSVs to 50 TSVs is 1.04 for plane three when $R_{vertical} = 30 \ m\Omega$. Thus, effective distance is influenced less in higher planes by number of TSVs.

In addition, linear relationship between effective distance and $R_{vertical}$ in plane one becomes non-linear in plane two and plane three. For example, in plane one, for higher values of $R_{vertical}$ as $40 \ m\Omega$, $45 \ m\Omega$, and $50 \ m\Omega$ with 500 TSVs, effective distance values are 1.903, 1.986, and 2.069 respectively. In plane two, for higher values of $R_{vertical}$ as $40 \ m\Omega$, $45 \ m\Omega$, and $50 \ m\Omega$ with 500 TSVs, effective distance values are 2.059, 2.132, and 2.2 respectively. For higher values of $R_{vertical}$ as $40 \ m\Omega$, $45 \ m\Omega$, and $50 \ m\Omega$ for third plane, effective distance values are sufficiently close as

1.858, 1.896, and 1.93 for 500 TSVs. This indicates saturating nature of effective distance with higher values of $R_{vertical}$ in higher planes.
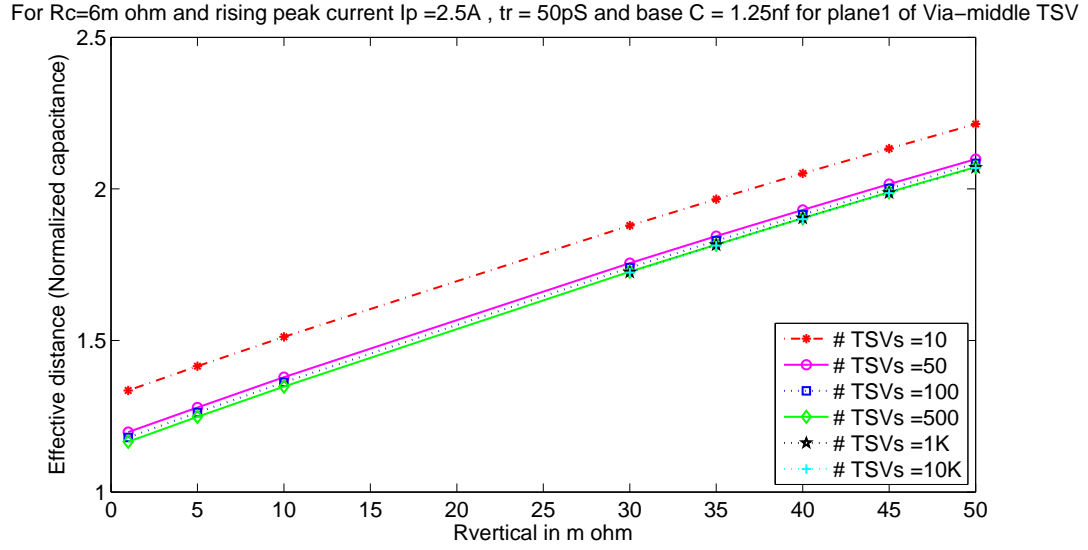

Figure 4.6: **Variation in effective distance with respect to $R_{vertical}$ in *plane one* for different number of via-middle TSVs when $R_c = 6\,m\Omega$, $I_p = 2.5\,A$, $t_r = 50\,pS$ and base capacitor $C_{base} = 1.25\,nF$.**

For Rc=6m ohm and rising peak current Ip =2.5A , tr = 50pS and base C = 1.25nf for plane2 of Via−middle TSV

Figure 4.7: **Variation in effective distance with respect to $R_{vertical}$ in *plane two* for different number of via-middle TSVs when $R_c = 6\,m\Omega$, $I_p = 2.5\,A$, $t_r = 50\,pS$ and base capacitor $C_{base} = 1.25\,nF$.**

For Rc=6m ohm and rising peak current Ip =2.5A , tr = 50pS and base C = 1.25nf for plane3 of Via−middle TSV
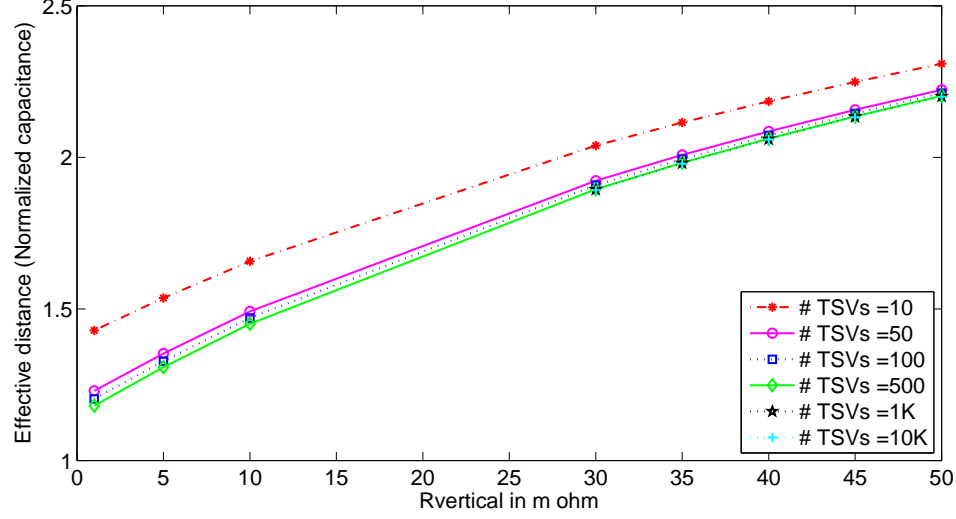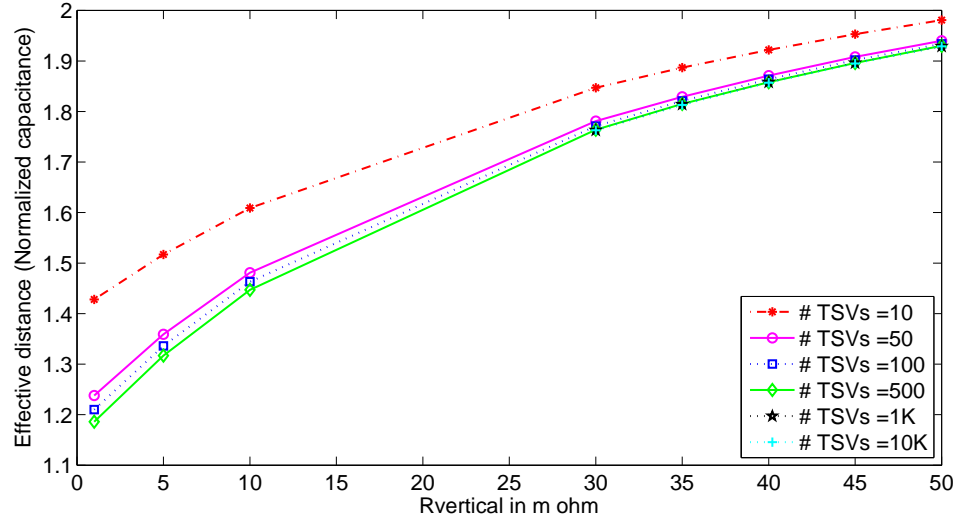
Figure 4.8: **Variation in effective distance with respect to $R_{vertical}$ in *plane three* for different number of via-middle TSVs when $R_c = 6\,m\Omega$, $I_p = 2.5\,A$, $t_r = 50\,pS$ and base capacitor $C_{base} = 1.25\,nF$.**

Also, for higher $R_{vertical}$ values, number of TSVs plays a negligible role. In

plane one, for $R_{vertical} = 30\ m\Omega$ with number of TSVs equal to 100, 500, 1K, and 10K, the effective distance values are 1.74, 1.727, 1.725, and 1.724 respectively. As seen in plane two, with a large number of TSVs such as 100, 500, 1K, and 10K, reduction in effective distance due to additional TSVs diminishes as seen by effective distance values of 1.908, 1.895, 1.894, and 1.892 respectively when $R_{vertical} = 30\ m\Omega$. In plane three, for $R_{vertical} = 30\ m\Omega$, with number of TSVs equal to 100, 500, 1K, and 10K, the effective distance values are 1.771, 1.764, 1.763, and 1.763 respectively.

## 4.4.2 Via-middle and Via-last TSVs - Effect of $R_{vertical}$ and Number of TSVs

Figures 4.9, 4.10, and 4.11 compare via-middle and via-last TSVs for plane one, two, and three respectively. As already discussed, via-last TSVs offer less resistance per TSV than that of via-middle TSVs. While analyzing via-last and via-middle TSVs, number of via-last TSVs is less than number of via-middle TSVs, such that both TSV types offer the same effective resistance. This allows a fair comparison and highlights the effect of $R_{vertical}$, which exists only for via-middle TSVs.

From Figures 4.9(a), 4.10(a) and 4.11(a), for a constant value of $R_{vertical}$ such as $5\ m\Omega$, linear relationship between effective distance (or total decoupling capacitance) and effective TSV resistance $R_{TSV}^{effective}$ changes to non-linear from lower to higher planes.

For $R_{vertical}$ of $5\ m\Omega$ and $R_{TSV}^{effective}$ of $10\ m\Omega$ in plane one, effective distance is 1.456 and 1.36 for via-middle and via-last TSVs respectively. For $R_{vertical}$ of $5\ m\Omega$ and $R_{TSV}^{effective}$ of $10\ m\Omega$ in plane two, effective distance is 1.588 and 1.456 for via-middle and via-last TSVs respectively. For $R_{vertical}$ of $5\ m\Omega$ and $R_{TSV}^{effective}$ of $10\ m\Omega$ in plane three, effective distance is 1.558 and 1.452 for via-middle and via-last TSVs respectively. From these plots, for $R_{TSV}^{effective}$ of $10\ m\Omega$, via-last TSVs perform better due to the absence of $R_{vertical}$, requiring 7.06%, 9.07%, and 7.3% less decoupling capacitance in plane one, two, and three respectively than that of via-middle TSVs.
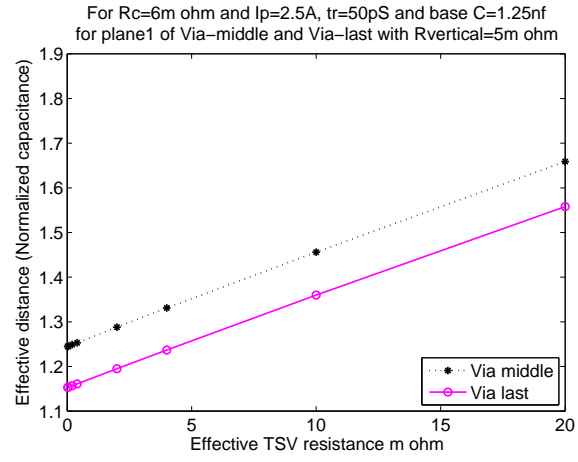
(a)
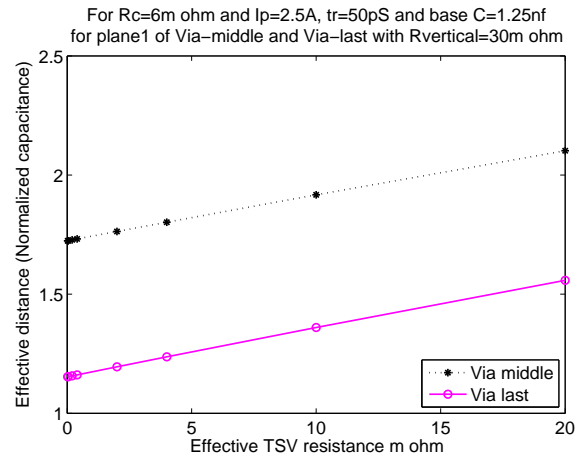
(b)
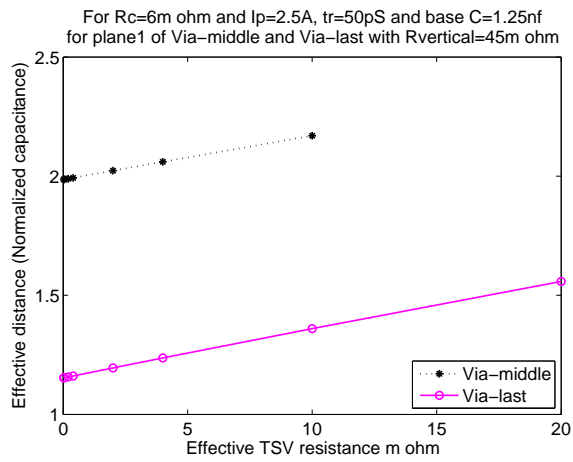
(c)

Figure 4.9: **Effect of** $R_{vertical}$ **on effective distance for** *plane one* **with via-middle TSVs**

For Rc=6m ohm and Ip=2.5A, tr=50pS and base C=1.25nf
for plane2 of Via−middle and Via−last with Rvertical=5m ohm

(a)

For Rc=6m ohm and Ip=2.5A, tr=50pS and base C=1.25nf
for plane2 of Via−middle and Via−last with Rvertical=30m ohm

(b)

For Rc=6m ohm and Ip=2.5A, tr=50pS and base C=1.25nf
for plane2 of Via−middle and Via−last with Rvertical=45m ohm
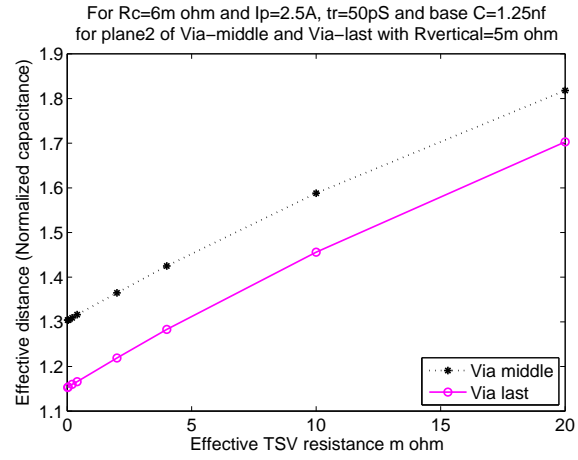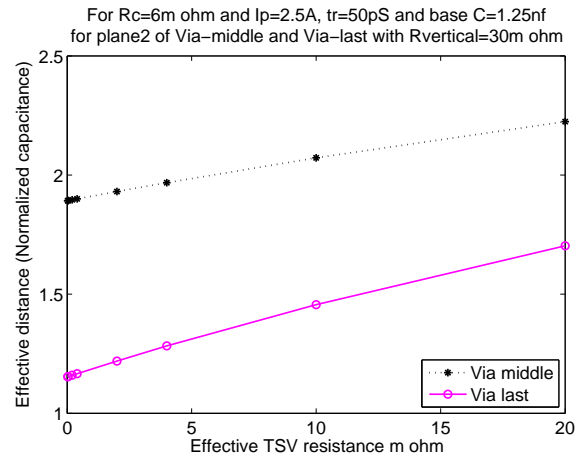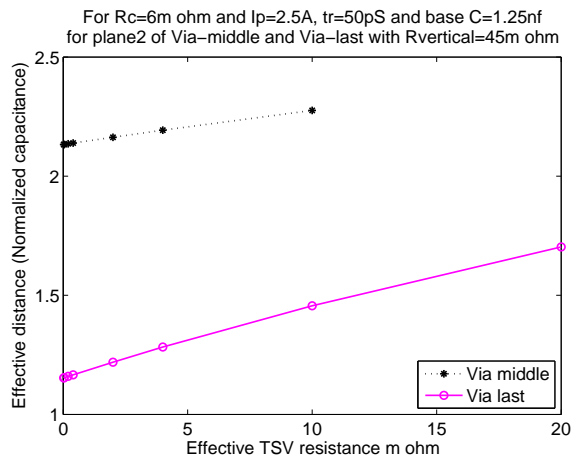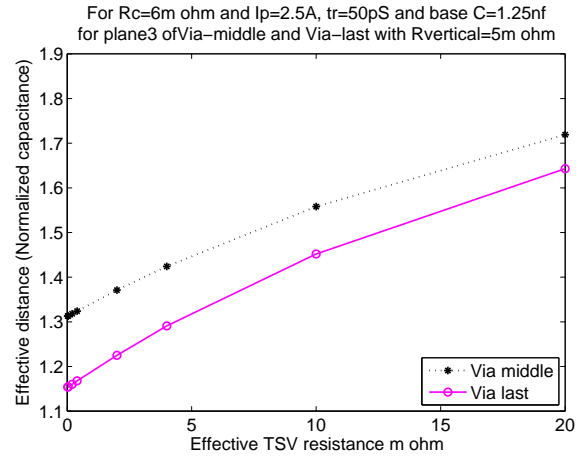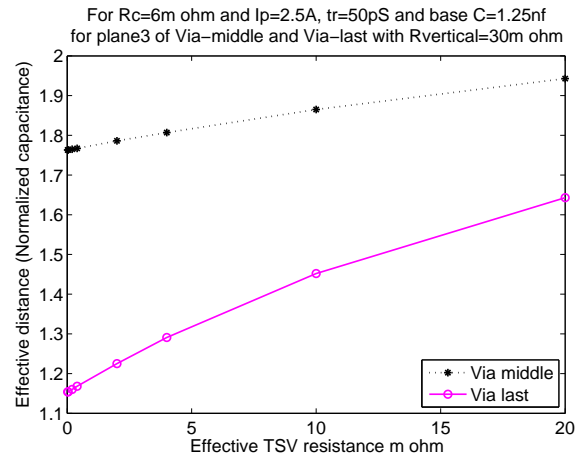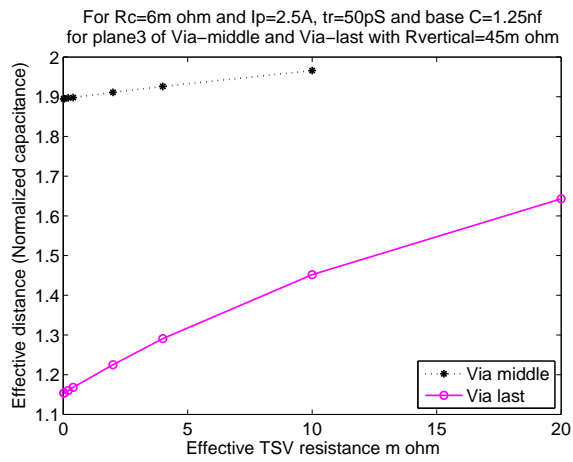
(c)

Figure 4.10: **Effect of $R_{vertical}$ on effective distance for** *plane two* **with via-middle TSVs**

41

(a)

(b)

(c)

Figure 4.11: **Effect of $R_{vertical}$ on effective distance for** *plane three* **with via-middle TSVs.**
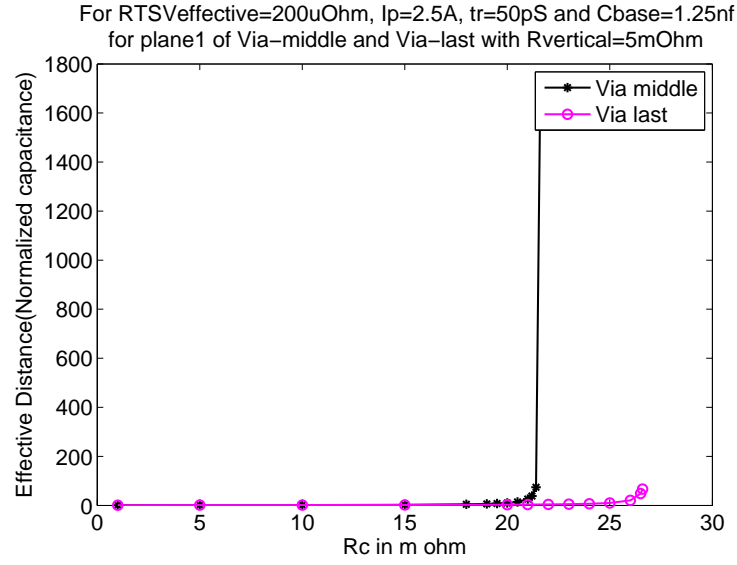
42

It is interesting to consider the effect of $R_{vertical}$ at a constant effective TSV resistance for different planes. The constant value of $R_{TSV}^{effective}$ assumed is 10 $m\Omega$. For plane one with via-middle TSVs, effective distance values are 1.456, 1.917, and 2.06 for $R_{vertical}$ of 5 $m\Omega$, 30 $m\Omega$ and 45 $m\Omega$ respectively. For plane two with via-middle TSVs, effective distance values are 1.588, 2.072, and 2.276 for $R_{vertical}$ equal to 5 $m\Omega$, 30 $m\Omega$ and 45 $m\Omega$ respectively. In plane three with via-middle TSVs, effective distance values are 1.558, 1.865, and 1.966 for $R_{vertical}$ of 5 $m\Omega$, 30 $m\Omega$ and 45 $m\Omega$ respectively. For $R_{TSV}^{effective}$ of 10 $m\Omega$, in plane one, two and three effective distance values for via-last TSVs are 1.36, 1.456, and 1.452 respectively. As via-last TSVs do not have $R_{vertical}$, effective distance values for via-last TSVs are independent of $R_{vertical}$. However, for via-middle TSVs in any plane, effective distance increases with increase in $R_{vertical}$.

As seen from Figures 4.9(c), 4.10(c) and 4.11(c) where $R_{vertical}$ is the largest, effective TSV resistance increases from left to right along x-axis (which suggests that less number of TSVs are used). Thus, at a point where $R_{TSV}^{effective}$ is 10 $m\Omega$, this $R_{TSV}^{effective}$ becomes so large that it can not satisfy the condition of R_c should be less than R_{max}. Hence, there is a break in the curve for via-middle TSVs. From this trend, for higher values of $R_{vertical}$, if effective TSV resistance of via-middle TSVs is higher than a limit (due to insufficient number of via-middle TSVs), decoupling capacitor is not effective. It imposes a restriction of using large number of via-middle TSVs if $R_{vertical}$ value is high.

Also, the effect of adding a large number of TSVs diminishes for any $R_{vertical}$ and any plane. For example, Figure 4.10(b) shows that a decrease in $R_{TSV}^{effective}$ from 4 $m\Omega$ to 40 $\mu\Omega$ reduces effective distance from 1.968 to 1.896 for via-middle TSVs. Decrease in $R_{TSV}^{effective}$ from 4 $m\Omega$ to 40 $\mu\Omega$ is accomplished by increasing the number of via-middle TSVs from 20 to 2000. Thus, a small reduction in effective distance is achieved at the expense of a significant increase in the area.

4.4.3 Via-middle and Via-last TSVs - Effect of R_c

Similar to 2-D integrated circuits, effect of R_c on effective distance is investigated when the remaining parameters are constant. In addition, simultaneous comparison of via-middle and via-last TSVs is interesting. A plane-by-plane approach is taken as shown before. Figures 4.12, 4.13 and 4.14 show the analytical results for plane one, two, and three respectively. In Figures 4.12(a) and 4.12(b), $R_{TSV}^{effective}$, I_p, t_r and base decoupling capacitor C_{base} are kept constant. Number of TSVs for via-last and via-middle are chosen to be different such that $R_{TSV}^{effective}$ remains the same for both TSV types. Two separate values of $R_{vertical}$ are considered over a range of R_c values for indicating the significance of $R_{vertical}$.

For RTSVeffective=200uOhm, Ip=2.5A, tr=50pS and Cbase=1.25nf
for plane1 of Via−middle and Via−last with Rvertical=5mOhm

(a)

For RTSVeffective=200uOhm, Ip=2.5A, tr=50pS and Cbase=1.25nf
for plane1 of Via−middle and Via−last with Rvertical=30mOhm
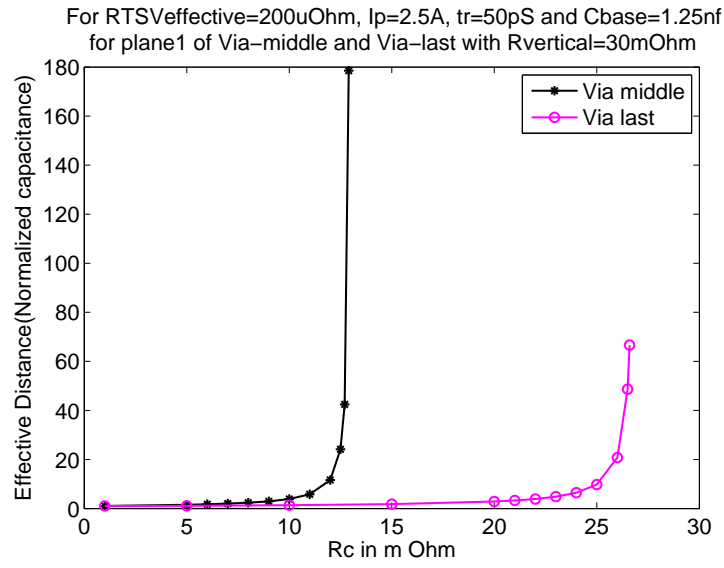
(b)

Figure 4.12: **Variation in effective distance with respect to R_c in** *plane one* **for TSV resistance** $R_{TSV}^{effective} = 200 \, \mu\Omega$ **when** $I_p = 2.5 \, A$, $t_r = 50 \, pS$, **and base decoupling capacitor** $C_{base} = 1.25 \, nF$ **for via-middle and via-last TSVs: (a)** $R_{vertical} = 5 \, m\Omega$, **(b)** $R_{vertical} = 30 \, m\Omega$.

For RTSVeffective=200uOhm, Ip=2.5A, tr=50pS and Cbase =1.25nf
for plane Two of Via−middle and Via−last with Rvertical=5mOhm

(a)

For RTSVeffective=200uOhm, Ip=2.5A, tr=50pS and Cbase=1.25nf
for plane Two of Via−middle and Via−last with Rvertical=30mOhm

(b)

Figure 4.13: **Variation in effective distance with respect to R_c in** *plane two* **for TSV resistance** $R_{TSV}^{effective} = 200\ \mu\Omega$ **when** $I_p = 2.5\ A$**,** $t_r = 50\ pS$**, and base decoupling capacitor** $C_{base} = 1.25\ nF$ **for via-middle and via-last TSVs: (a) is for** $R_{vertical} = 5\ m\Omega$**, (b)** $R_{vertical} = 30\ m\Omega$**.**

For RTSVeffective=200uOhm, Ip=2.5A, tr=50pS and Cbase=1.25nf
for plane Three of Via−middle and Via−last with Rvertical=5mOhm

(a)

For RTSVeffective=200uOhm, Ip=2.5A, tr=50pS and Cbase=1.25nf
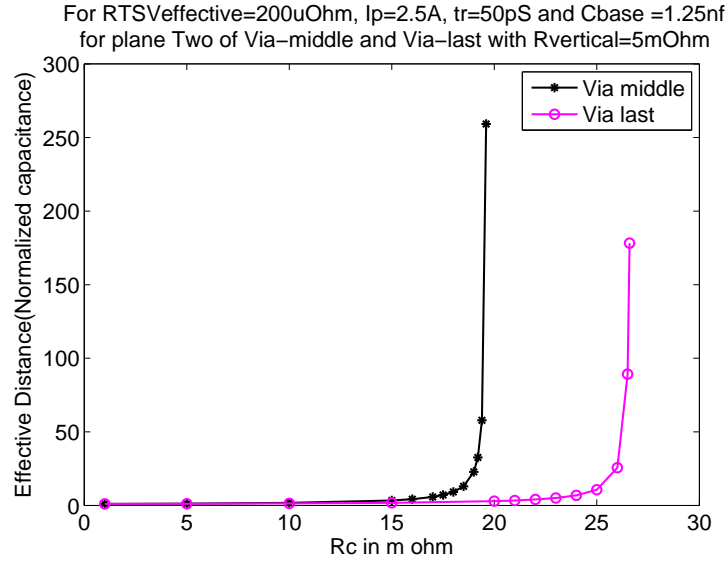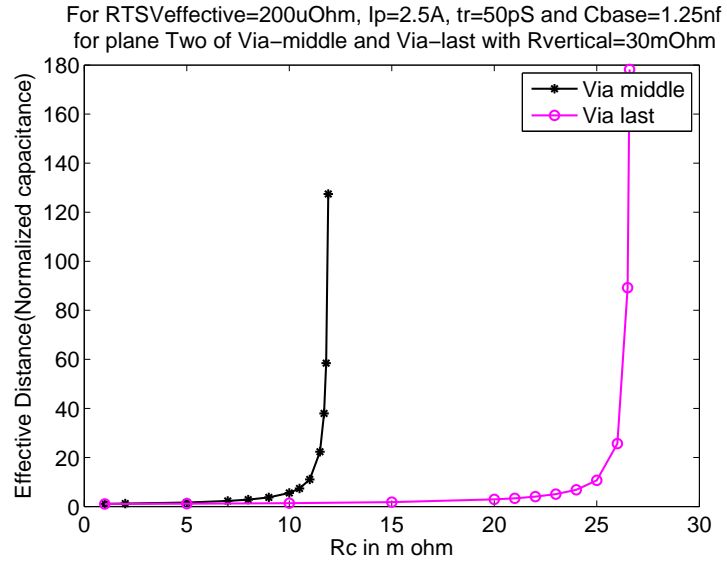for plane Three of Via−middle and Via−last with Rvertical=30mOhm
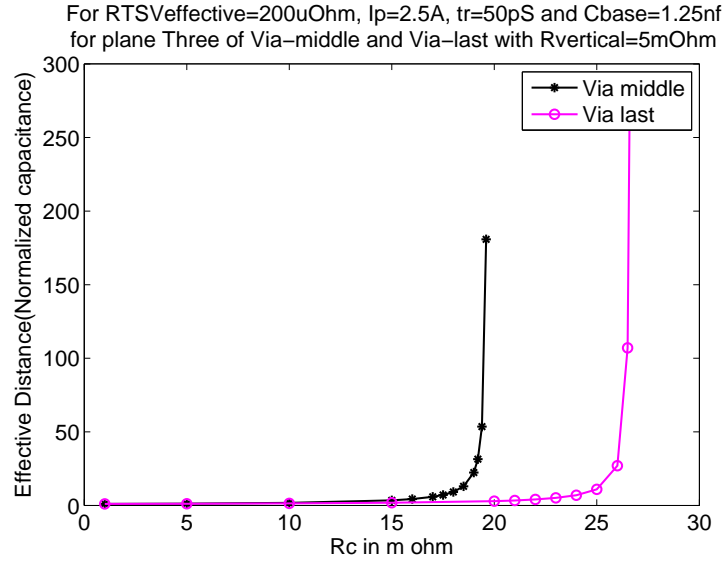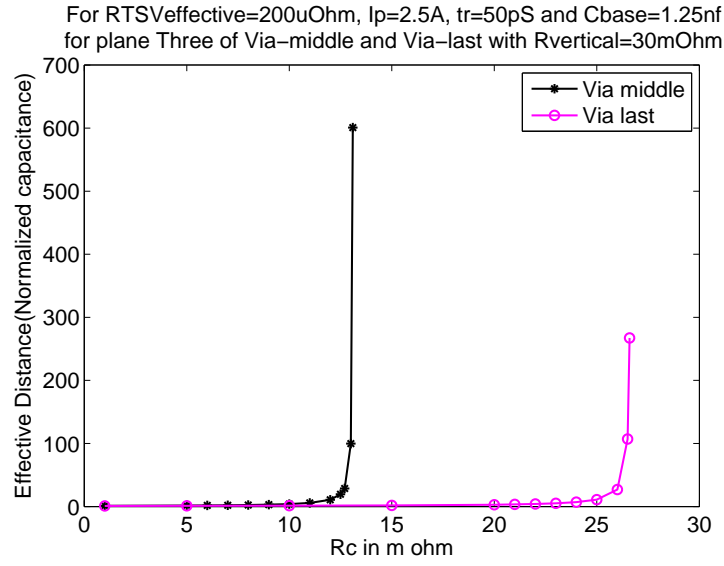
(b)

Figure 4.14: **Variation in effective distance with respect to R_c in** *plane three* **for TSV resistance** $R_{TSV}^{effective} = 200\ \mu\Omega$ **when** $I_p = 2.5\ A$, $t_r = 50\ pS$, **and base decoupling capacitor** $C_{base} = 1.25\ nF$ **for via-middle and via-last TSVs: (a) is for** $R_{vertical} = 5\ m\Omega$, **(b)** $R_{vertical} = 30\ m\Omega$.

Comparing results for plane one, two, and three from Figures 4.12(a), 4.13(a) and 4.14(a) for a constant $R_{vertical}$ of 5 $m\Omega$, for same value of R_c, larger decoupling capacitance is required for higher planes. For example, for R_c of 10 $m\Omega$ and $R_{vertical}$ of 5 $m\Omega$, via-middle TSVs require decoupling capacitance of 1.576, 1.747, and 1.764 times the C_{base} in plane one, two, and three respectively. Similarly, for R_c of 10 $m\Omega$, via-last TSVs require decoupling capacitance of 1.346, 1.347, and 1.348 times the C_{base} in plane one, two, and three respectively. Thus, via-last TSVs require 17.08%, 29.70%, and 30.86% of less decoupling capacitance than via-middle TSVs for R_c of 10 $m\Omega$ and $R_{vertical}$ of 5 $m\Omega$. Similarly, for higher values of R_c, larger decoupling capacitance is required for any plane for a given type of TSV (and a constant $R_{vertical}$ in case of via-middle TSVs). Also, in any plane, for a constant R_c, increase in $R_{vertical}$ causes increase in effective distance for via-middle TSVs.

Furthermore, in any plane, for a constant value of $R_{vertical}$, increase in R_c causes exponential increase in effective distance after a certain value. As seen from Figure 4.12(a), in plane one with $R_{vertical}$ of 5 $m\Omega$, increase in R_c causes exponential increase in effective distance after R_c exceeds 21 $m\Omega$ and 25 $m\Omega$ for via-middle and via-last TSVs respectively. With increase in $R_{vertical}$ to 30 $m\Omega$ as seen in Figure 4.12(b), this threshold shifts to a smaller value of 10 $m\Omega$, requiring additional decoupling capacitance for via-middle TSVs. Via-last TSVs are not influenced by any change in $R_{vertical}$, since they do not rely on metal vias to connect the planes.

Due to absence of $R_{vertical}$, via-last TSVs are superior than via-middle TSVs in a given plane as via-last TSVs require less effective distance for given value of R_c. This is seen from Figure 4.14(a), where for 15 $m\Omega$ of R_c, via-middle TSVs require $3.421C_{base}$ decoupling capacitance and via-last TSVs require only $1.786C_{base}$ decoupling capacitance. This effect becomes more visible beyond threshold value for via-middle TSVs. For example, at 19.6 $m\Omega$ of R_c, via-middle TSVs need $180.788C_{base}$ of decoupling capacitance and via-last TSVs need only $1.8C_{base}$ of decoupling capacitance. Thus, in 3-D ICs with via-last TSVs, circuit blocks can more efficiently utilize decoupling capacitors in adjacent planes.

Chapter 5

Conlusions

The concept of effective distance has been presented and discussed in detail with the help of analytical results that have also been verified by SPICE simulations. Effectiveness of a decoupling capacitor depends on its magnitude and distance from switching load. This distance is quantified in terms of R_c. In general, R_c signifies resistance between the switching load and decoupling capacitor within a plane (for 2-D ICs) or across the planes (for 3-D ICs). Concept of effective distance remains valid for both 2-D and 3-D integrated circuits. With the help of effective distance, a decoupling capacitor does not need to be adjacent to the load. The switching loads can use not only the adjacent decoupling capacitors, but also the decoupling capacitors within a certain distance. The idea of effective distance demonstrated here suggests that a decoupling capacitor sized properly can lie at any distance from the load where the resistance between load and decoupling capacitor is less than a critical value of R_{max}, and still be as effective as if it were next to the load.

3-D ICs that benefit from vertical integration of dies can effectively use on-chip decoupling capacitors across different planes if two conditions are satisfied: 1) resistance between load in one plane and decoupling capacitor in other plane R_c is less than R_{max}, and 2) total decoupling capacitance C is equal to or greater than the product of effective distance calculated for R_c and base decoupling capacitor C_{base}.

Existing effective distance formulation is improved and extended to a load cur-

rent modeled as a ramp signal which is more realistic for practical switching currents. With resistive approximations of TSV models, a closed-form expression for effective distance is obtained. This closed-form expression has been validated through SPICE simulations.

Different types of TSVs, their models and influence on determining required effective distance are shown with the help of different graphs. It is visible from these graphs that a reduction in effective TSV resistance helps decoupling capacitors to be effective for larger distances within that plane and other planes. However, beyond a certain limit, this gain diminishes.

When comparing via-last and via-first/via-middle TSVs, via-last TSVs with less resistance are found to be superior, requiring less decoupling capacitance when the rest of the circuit parameters are the same. For effective TSV resistance of $10\ m\Omega$, via-last TSVs perform better due to absence of $R_{vertical}$, requiring 7.06%, 9.07%, and 7.3% of less decoupling capacitance in plane one, two, and three respectively than that of via-middle TSVs.

With accurate estimation of required decoupling capacitance calculated using effective distance, unnecessary on-chip decoupling capacitance added in *ad-hoc* manner can be avoided. This saves die area. In addition, if die level power gating is applied, the decoupling capacitor in that die would be useful for other planes if it lies within the limit. This applies to power gating within a plane or across the planes in 3-D ICs.

5.1 Future scope

On-chip decoupling capacitors are allocated to the white space after layout is completed. If larger decoupling capacitance is needed, larger area is required, so the layout is performed again to allocate this extra space among circuit blocks. This process is repeated until the timing and signal/power integrity constraints are satisfied. This iteration causes increased time-to-market, design effort, and cost. The approach presented in this work tries to overcome this issue, by allocating precise

amount of decoupling capacitance. Thus, during physical design phase, required amount of decoupling capacitance and circuit block can be placed simultaneously. Development of such algorithms with this improved model of effective distance can speed up and improve physical design process.

Load current in this work is modeled as a ramp signal with a rising transition, which corresponds to the discharging phase of a decoupling capacitor. Decoupling capacitor also requires a recharging process when the switching activity cycle is over. This recharge phase can be modeled by a load current with a falling transition. Hence, load current model can be further improved with a sawtooth current waveform (that involves rising and falling transitions) instead of a ramp current. Effective distance can be extended to the recharging phase of a decoupling capacitor.

Bibliography

[1] E. Salman and E. G. Friedman, *High Performance Integrated Circuit Design*, McGraw-Hill, 2012.

[2] J. Lu, "3-D Hyperintegration and Packaging Technologies for Micro-Nano Systems," *Proceedings of the IEEE*, Vol. 97, No. 1, pp. 18–30, January 2009.

[3] E. Salman, M. H. Asgari, and M. Stanacevic, "Signal integrity analysis of a 2-D and 3-D integrated potentiostat for neurotransmitter sensing," *Proceedings of the IEEE Biomedical Circuits and Systems Conference*, pp. 17–20, November 2011.

[4] A. W. Topol *et al.*, "Three-dimensional integrated circuits," *IBM Journal of Research and Development*, Vol. 50, No. 4.5, pp. 491–506, July 2006.

[5] E. Salman, E. G. Friedman, and R. M. Secareanu, "Substrate and Ground Noise Interactions in Mixed-Signal Circuits," *Proceedings of the IEEE International SOC Conference*, pp. 293–296, September 2006.

[6] P. Andry *et al.*, "Fabrication and characterization of robust through-silicon vias for silicon-carrier applications," *IBM Journal of Research and Development*, Vol. 52, No. 6, pp. 571–581, November 2008.

[7] M. Popovich, A. V. Mezhiba, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors*, Springer, 2007.

[8] E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Worst Case Power/Ground Noise Estimation Using an Equivalent Transition Time for Resonance," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, Vol. 56, No. 5, pp. 997–1004, May 2009.

[9] L. D. Smith, "Decoupling capacitor calculations for CMOS circuits," *Electrical Performance of Electronic packaging*, pp. 101–105, Nov 1994.

[10] H. Su, S. S. Sapatnekar, and S. R. Nassif, "Optimal decoupling capacitor sizing and placement for standard-cell layout designs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 22, No. 4, pp. 428–436, April 2003.

[11] S. Zhao, K. Roy, and C. Koh, "Decoupling capacitance allocation and its application to power-supply noise-aware floorplanning," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 21, No. 1, pp. 81–92, January 2002.

[12] M. Popovich, M. Sotman, A. Kolodny, and E. G. Friedman, "Effective Radii of On-Chip Decoupling Capacitors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 16, No. 7, pp. 894–907, July 2008.

[13] E. Wong, J. R. Minz, and S. Lim, "Decoupling-Capacitor Planning and Sizing for Noise and Leakage Reduction," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 11, pp. 2023–2034, November 2007.

[14] H. Jao *et al.*, "The impact of through silicon via proximity on CMOS device," *Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 7th International*, pp. 43–45, Oct 2012.

[15] G. Pares *et al.*, "Through Silicon Via technology using tungsten metallization," *IEEE International Conference on IC Design & Technology (ICICDT)*, pp. 1–4, May 2011.

[16] A. Agarwal, R. B. Murthy, V. Lee, and G. Viswanadam, "Polysilicon interconnections (FEOL): Fabrication and characterization," *Electronics Packaging Technology Conference*, pp. 317–320, Dec 2009.

[17] N. Lin,and J. Miao, "Through-silicon via fabrication with pulse-reverse electroplating for high density nanoelectronics," *IEEE 5th International Nanoelectronics Conference (INEC)*, pp. 381–384, Jan 2013.

[18] P. Andry *et al.*, "A CMOS-compatible process for fabricating electrical through-vias in silicon," *Proceedings of Electronic Components and Technology Conference, 56th*, pp. 831–837, 2006.

[19] S. M. Satheesh, and E. Salman, "Power Distribution in TSV-Based 3-D Processor-Memory Stacks," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 2, No. 4, pp. 692–703, December 2012.

[20] C. Laviron *et al.*, "Via First Approach Optimisation for Through Silicon Via Applications," *Proceedings of the IEEE Electronic Components and Technology Conference*, pp. 14–19, May 2009.

[21] G. Pares *et al.*, "Mid-Process Through Silicon Vias Technology Using Tungsten metallization: Process optimazation and electrical results," *Proceedings of the IEEE Electronics Packaging Technology Conference*, pp. 772–777, December 2009.

[22] T. Dao *et al.*, "Thermo-Mechanical Stress Characterization of Tungsten-Fill Through-Silicon-Via," *Proceedings of the IEEE International Symposium on VLSI Design Automation and Test*, pp. 7–10, April 2010.

[23] M. Kawano *et al.*, "A 3D Packaging Technology for 4 Gbit Stacked DRAM with 3 Gbps Data Transfer," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 1–4, December 2006.

[24] M. Puech *et al.*, "DRIE Achievements for TSV Covering Via First and Via Last Strategies," *Proceedings of the Advanced Technology Workshop on 3D*

Packaging in IMAPS 4th International Conference and Exhibition on Device Packaging, March 2008.

[25] S. Ramaswamy *et al.*, "Process Integration Considerations for 300 mm TSV Manufacturing," *IEEE Transactions on Device and Materials Reliability*, Vol. 9, No. 4, pp. 524–528, December 2009.

[26] D. H. Kim, S. Mukhopadhyay, and S. K. Lim, "Through-silicon-via Aware Interconnect Prediction and Optimization for 3D Stacked ICs," *Proceedings of the International Workshop on System Level Interconnect Prediction*, pp. 85–92, September 2009.

[27] C. G. Small, *Expansions and Asymptotics for Statistics*, CRC Press, 2010.

[28] S. Logan, and M. R. Guthaus, "Fast thermal-aware floorplanning using white-space optimization," *IFIP International Conference on Very Large Scale Integration (VLSI-SoC)*, pp. 65–70, October 2009.

[29] N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison-Wesley, 2010.