## Frontend Electronic System for a Triboelectric Harvester in a Smart Knee Implant

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#### Abstract of the Dissertation

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Total knee replacement (TKR) is an increasingly common surgery, particularly among active young and elderly people who suffer from knee pain. Continuous monitoring of the load on the knee after the surgery is highly desirable for designing an efficient and more functional smart knee implant. This thesis outlines the design of a frontend electronic system for a triboelectric harvester in a smart knee implant. The triboelectric harvester produces an output signal, which is used by the proposed frontend electronic system to extract power and efficiently monitor the load on the knee. The peak magnitude of the harvested signal changes with the applied force. Thus, harvested signal is used both as a data signal for processing (to monitor the load) and power signal for rectification without any external bias voltage. First, an electrical model is developed for the fabricated harvester to produce a signal with similar electrical characteristics. In the next step, the output signal is divided into a signal path and power path via an impedance matching circuitry. The power transfer along the power path is maximized. The implementation of a PCB prototype demonstrates that the output harvester signal can be digitized by relying only on the harvested power.

For a potential application specific integrated circuit (ASIC) implementation, several feature extraction circuits are developed. These circuits extract useful features of the harvester signal (such as peak voltage

and pulse width) rather than digitizing the entire signal, thereby significantly reducing the on-chip storage requirement. A power management system incorporating supercapacitors, diodes and switches is also developed to store excess energy when harvested power is more than what is consumed by the circuit. This power management system ensures optimal charging and discharging of the supercapacitor. Finally, wireless power transfer for the knee implant is investigated by using a near-field inductive link where the implanted coil is placed within the harvester package. Wireless power transfer is used to transmit the data to an external reader device. The methods developed in this thesis demonstrate the feasibility of triboelectric energy harvesting in continuously monitoring the loads on knee implants.

This work is dedicated to GOD, to my advisor, and to my family and friends for supporting me throughout these years.

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# **Chapter 1**

# Introduction

The number of total knee replacement (TKR) surgeries has been increasing tremendously. For instance, in the United States, it is expected to reach 3.48 million by 2030 [1, 2]. TKR is more frequently being performed for younger, more active patients who demand a longer service life from their implants. Such activities, however, place greater demands on implant components, with the possible and undesirable outcome of premature implant failure. A major contributor to poor functioning TKRs is incorrect ligament balancing [3], which can accelerate wear from joint reaction force imbalances and promote prosthetic loosening [4]. While there are various techniques for analyzing the kinematics of TKR implants after surgery, it remains a challenge to directly measure the loads experienced by these devices; loads that can eventually lead to implant failure.

The ability to monitor the magnitude and distribution of loads passing through TKR components would allow us to detect the unsafe loads, and provide immediate response to the patient before the implant fails. It can also help in post-operative joint monitoring to alert patients and surgeons about problems that could potentially be addressed early to avoid a more complex and expensive surgery later on [5]. Furthermore, sensing the load would enable a better understanding of the demands, which could be leveraged during the design process to enhance future implants.

In the triboelectric mechanism, power is generated when a certain material comes in contact with a

different material. These two materials are chosen based on their location in the triboelectric series. The farther away the two materials are in the series, the greater is the power generated. The triboelectric mechanism is classified in two categories based on the movement between the two materials. If the movement is horizontal, it is known as sliding-mode triboelectric mechanism, otherwise if the movement is vertical, it is known as contact-mode triboelectric mechanism [6]. The harvester designed for this research is based on contact-mode triboelectric mechanism [7].

Compared to other harvester types such as piezoelectric or electromagnetic, triboelectric material achieves greater energy density and offers key advantages such as simple fabrication, excellent reliability, high efficiency, and low cost [8, 9]. Furthermore, the piezoelectric energy harvesters generate voltage from deformations and since TKR implants have limited space, the piezoelectric element deformations are not significant, which degrades the output power [10]. Alternatively, in the triboelectric mechanism, contact electrification occurs when a certain material comes in a frictional contact with a material of different polarity. Since in a TKR implant, this movement occurs naturally, the triboelectric mechanism is suitable to harvest energy, which can be used to self-power an electronic system and monitor the load [6–9, 11, 12].

Fig. 1.1 shows a typical TKR implant as demonstrated by the American Academy of Orthopaedic Surgeons [13]. In a typical TKR surgery, damaged bone and cartilage are removed and replaced with metal components that recreate the surface of the joint between the femur and tibia. A plastic spacer is also placed in between the components [13]. For the research described in this thesis, the triboelectric harvester and the proposed frontend electronic chip will be placed inside the 3D package and finally implanted between the femoral and tibial layers in the knee [7, 12, 14, 15].

This thesis demonstrates the frontend electronic system designed to process the signal from the harvester and eventually monitor the load on the knee. The triboelectric harvester produces an AC signal with different peak voltages depending on the magnitude of the force applied to it. The electronic chip then processes that signal and converts it into readable information which can eventually be used to monitor the knee loads and most importantly implant failures. The electronic system comprises of several components - an electrical model to model the signal from the harvester, a voltage processing unit to attenuate the high peak voltages in the harvested signal, a rectifier and a regulator to produce a biasing voltage for the ADC, and



Figure 1.1: A typical TKR implant [13].

finally an analog-to-digital converter (ADC) to convert the analog input into digital bits. These bits can be stored within nonvolatile memory and read using inductive coupling to monitor the knee load [7, 12, 14, 15].

The rest of the thesis is organized as follows. In Chapter 2, the background on triboelectric mechanism and related prior research is summarised. An overview of the harvester, experimental setup and the harvester output waveform (which is input to the frontend electronic system) are also presented in this chapter. The printed circuit board (PCB) prototype implementation of the designed frontend electronic system for a small range of cyclic loads and the corresponding test results are described in Chapter 3. In Chapter 4, the PCB implementation of an improved electronic frontend circuit that can work with a wider range of cyclic loads is presented. The measurement results with the harvester are also shown. Chapter 5 demonstrates a potential ASIC implementation of the design and also provides the details of the feature extraction circuitry designed to extract several important features from the harvested signal (rather than digitizing the entire signal). The implementation of a power management circuit with supercapacitors is also shown. The design of the inductive link for wireless power/data transfer is analyzed in Chapter 6. Finally, the thesis is concluded in Chapter 7 and some potential directions for future work are summarized.

# Chapter 2

# Background

Activities of daily living (ADL) such as walking, running, jumping, and other activities result in the transfer of significant amount of loads through the human knee joint [16]. Continuous monitoring of these knee loads after surgery offers the potential to improve surgical procedures, current implants and most importantly, helps designing new and better implants. The main objective of this research is to develop a frontend electronic system for a triboelectric energy harvester in a smart knee implant, which continuously monitors the load on the knee and helps in providing quick response to the patient/care giver much before the implant failure.

## 2.1 History of TKR Implants

In order to monitor the proper functionality of the knee after surgery, different TKR implants have been proposed in literature. In [17, 18], one of the very first TKR implants was embedded in the knee of a senior patient. The implant consisted of four load cells with wireless micro-transmitters. However, the major limitation of this design was that the load measurement could only be done in a medical clinic as remote powering using magnetic near-field coupling was required for operation. Extensive *in vivo* studies have also been reported on measuring the load at knee joints during activities of daily living [19–21]. They provided a detailed description of the forces and moments acting on the knee joints. However, the major drawback of this approach was that the reported data was measured for a specific implant design and could not be transferred directly to another implant or the natural human knee.

The utilization of sensors for intra-and post-operative estimation has pulled in much enthusiasm for the field of biomedical research in recent years, particularly in the field of orthopaedics. Such intra-operative estimation sensors are now available commercially for the total knee replacement surgeries. Yet, they provide data only during the surgery and should be removed by the end of the surgery [22–24], while the post-operative measurement is still missing. Since, the required *in vivo* information consists of gathering force measurements during and after surgery, recent studies investigated load sensors that can measure the knee loads as well as make use of these loads for harvesting energy and providing a self-powering mechanism [10, 25–28].

### 2.2 Current Research on TKR Implants

A smart knee implant has been designed in [29], which is powered using the energy harvested from an electromagnetic generator. This harvester is a combination of a few magnets inserted between the coil, hence, increasing the size of the system and consuming more power in the range of milliwatts.

Piezoelectric mechanism is one of the most common techniques used for powering load sensors. In [26], the benefits of piezoelectric ceramics have been investigated for power generation in total knee replacement applications. The TKR design in [25] incorporates four piezoelectric transducers placed between the tibial tray and polyethylene for knee load sensing and self-powering. The design has the ability to detect the knee forces and harvest energy up to 5 mW under normal walking activity. In [10], the TKR design was optimized by embedding the piezoelectric sensor in the polyethylene bearing, which is considered more preferable and suitable with the traditional and FDA-approved tibial components. Piezoelectric energy harvesters generate voltage from material deformations. Since the space is very limited in TKR surgeries, the piezoelectric element deformations are not significant, thereby limiting the amount of harvested power. Furthermore, these deformations degrade performance and service life.

In recent years, triboelectric mechanism has been demonstrated as an alternative mechanism for vibration energy harvesting [6, 8, 30]. Triboelectric transducers generate voltage from pressure (force) [31] and they do not require large deformations, thus do not have the size limitation of piezoelectric devices. The larger the pressure, the higher the output power is. As knee is one of the body joints that takes 3 to 6 times the body weight [18], triboelectric energy harvesting can serve as an ideal candidate for scavenging energy from the loads at the knee joint. An example triboelectric harvester and a triboelectric TKR implant is shown in Fig. 2.1. This harvester has two layers, an upper Ti and a lower polydimethylsiloxane (PDMS) insulator which are bonded to either another Ti layer to form a Ti-PDMS-Ti harvester or an Al layer to create a Ti-PDMS-Al harvester. The upper Ti and lower PDMS layers have reverse sawtooth ridges, as shown in Fig. 2.1(a). PDMS is a commonly used polymer, because of its flexibility, manufacturing ease and bio-compatibility. On the other hand, Ti is highly suitable due to its stiffness and strength. Two of these identical harvesters are centered at the medial and lateral positions between the tibial tray and ultra-high molecular weight polyethylene (UHMWPE) bearing in the TKR implant, as shown in Fig. 2.1(b) [32].



Figure 2.1: Triboelectric Effect: (a) an example triboelectric energy harvester, and (b) the triboelectric TKR implant [32].

In the triboelectric mechanism, contact electrification happens when two different materials at different polarities come into contact and then separate [33–38]. Because in the total knee replacement, this movement occurs naturally, the triboelectric energy harvesting mechanism is very suitable to harvest energy in a TKR. This cyclic process of contact and separate leads to the flow of charges between the two triboelectric layers. The charge density is a function of multiple factors such as chemical properties of the materials and the micro-surface patterns that control the area of contact [39]. Surfaces with micro patterns increase the contact area and enhance the power efficiency [40, 41].

In [42], a scalable, wearable e-textile triboelectric energy harvesting (WearETE) system has been designed. The WearETE system features ultra-low-cost material and manufacturing methods, high accessibility, and high feasibility for powering the wearable sensors and electronic devices. Hence, the triboelectric mechanism has been incorporated for powering the frontend electronic system.

### **2.3** Frontend Electronics in Implantable Devices

Significant research has been conducted in the field of integrating the frontend electronics with any energy harvesting mechanism so that the system can be used in implantable biomedical applications. The fundamental architecture of a frontend electronic system in an implantable device typically comprises of the following components [43–46]:

- a *voltage processing unit* (filters/amplifiers/attenuators) if the input from the harvester is higher or lower than required (this components also acts as the impedance matching unit),
- an *AC-DC converter* (rectifier) and/or a *DC-DC converter* (regulator) based on the input from the harvester,
- an analog-to-digital converter (ADC) to convert the harvested signal into digital form,
- a *power management unit* to manage energy storage and the flow of power among various components of the system,

- an oscillator to provide clock signal for synchronizing various components,
- a microprocessor or digital block to process the data, and
- a *memory* unit to store the data.

For instance, research in [47] demonstrates using a continuous-time sigma-delta ( $CT-\sum \triangle$ ) modulator for implantable and portable biomedical devices. The designed electronic system consists of a secondorder modulator and a decimation stage based upon a finite impulse response (FIR) filter. It consumes low power and achieves reasonable signal-to-noise ratio (SNR). The sigma-delta modulators do not use switched capacitors, hence the amplifier design constraints such as settling time and bandwidth have low impact on the performance of ADC. Another study in [44] describes a wireless power transfer system with dual-output regulated active rectifier for implantable medical devices. The rectifier uses pulse-skip modulation (PSM) to regulate both the output voltages without using low-dropout regulators (LDOs). The system consists of a power amplifier, a rectifier and resonant tanks, thereby achieving 67.2% maximum power conversion efficiency (PCE) [7].

Research performed in [48] describes a power management system which can turn an implantable biomedical device on or off on-demand, hence saving the energy. It is controlled ultrasonically which reduces the device size, provides directional insensitivity and offers deeper penetration depth. Rapid-prototyping laser-assisted circuit printing is also introduced to reduce the fabrication cost and size of the ultrasonic control module. The proposed power management system consists of a piezoelectric receiver, a bridge rectifier, a filter capacitor, a Schmitt trigger, and a D flip-flop.

Existing commercial approaches for load sensing include using strain gauges in implants to measure the *in vivo* tibiofemoral forces and moments on the tibial tray during various activities of daily living. However, strain gauge postoperative function requires a continuous source of electrical energy, which significantly limits its practicality. Specifically, the energy to operate this type of implantable devices is provided through an inductive link [49, 50]. In an inductive link, an external primary coil transmits electro-magnetic power to the secondary coil integrated within the implantable device. The link is also used to continuously transmit sensory data recorded from the implant. The external coil, integrated with a wearable device, is constantly

worn to provide power to the implant, which presents an inconvenience to the user. To avoid continuous powering of sensor through an inductive link, a rechargeable battery could be integrated within the implant. This battery would be periodically recharged through inductive link. However, a rechargeable battery has a limited number of charging cycles. Considering the maximum capacity of the rechargeable battery that could fit in the limited available space and the lifetime of the knee implant, this option is not feasible. More recent studies developed self-powered instrumented knee implants for postoperative load detection using electromechanical [51] or piezoelectric mechanisms [10, 25]. However, these mechanisms require major changes to the implant designs that complicate fabrication, adversely affect their lifetime, and limit their use for various prostheses [7].

Patients using implantable biomedical devices with wireless inductive telemetry as the energy source are required to carry external hardware and antennas on their body during the data monitoring period. The discomfort can be reduced by using supercapacitors as the energy source. These supercapacitors can be charged using the external wireless telemetry unit which activates the implantable device. After the wireless telemetry unit is removed, the supercapacitor provides power to the implantable device. The benefits of integrating supercapacitors onto an existing pressure sensing medical implant that utilizes an inductive telemetry link are demonstrated in [52]. This work demonstrates that the medical implant can be powered for a full day using a 88 mF supercapacitor. The inductive link can fully charge the supercapacitor in 81 seconds at a wireless distance of 20 cm.

While designing an implantable electronic system, several general constraints should be addressed such as compact size and weight, low power consumption, high bio-compatibility (minimal toxicity), sufficient reliability, and high data rate. In addition to being less invasive to the body of the patient during implantation, smaller and lightweight devices are likely to cause less pain and discomfort. The excessive weight and size may be problematic in the healing process by putting pressure on the adjacent tissues that have already been damaged during surgery, contributing to inflammatory processes within the peri-implant space. Lighter and smaller implant devices are less restrictive in terms of normal level of human activity, and thus provide better quality of life to the patients [53]. Low power consumption is important for the long-term performance of the device and safety to the patient.

Close proximity of the electrodes to living tissues places limitations on the maximum amount of power that an implanted electronic system can dissipate, as extensive power dissipation may inflict damage onto the soft tissues [54]. For battery-less devices powered by a wireless link, the low power restriction also ensures that electromagnetic energy radiated or back-scattered by the device during wireless communication satisfies the IEEE human tissue exposure standards [55]. Excessive electromagnetic fields can potentially degrade device functioning, and can eventually lead to temporary malfunction or permanent damage. Device reliability is important, as failure may not only cause pain, discomfort or local damage to the peri-implant space, but may also cause irreversible damage to the patient. Considering that many implants are introduced deep into the tissues and cavities of the body, device maintenance is also complicated, with risks to the health of the patient [53, 56].

Communication technologies used for data transfer should support, in general, high data rate, low error rate, and adequate data security. These technologies should also be reliable and consume minimal power [57]. Remote monitoring facilities are more commonly used. The essential benefits include the ability to respond promptly to the patient, minimize harmful effects of malfunction or failure of the implant; ability to monitor the effectiveness of the treatment and also to alter the stimulation parameters based on monitored data. Furthermore, remote monitoring can effectively reduce the weight of in-clinic follow-up on the healthcare system, while maintaining or improving the existing patient safety standards [58].

### 2.4 The TKR System for this Research

The schematic of triboelectric total knee replacement (TKR) system that incorporates the frontend electronic system designed in this research is illustrated in Fig. 2.2(a). TKR consists of the femoral and tibial tray, and the UHMWPE bearing parts. For optimal load monitoring, the designed triboelectric harvesters are placed between the tibial tray and the UHMWPE bearing. The proposed electronic system is placed on the tibial tray so that it can be powered entirely through the power generated by the designed triboelectric harvesters without external biasing. The harvesters and the electronic system are placed in a 3D package

[59]. The enlarged view of the package with the triboelectric generators is shown in Fig. 2.2(b). These tribolectric harvesters are designed by the mechanical engineering team at SUNY Binghamton and the 3D package is developed by the material science team at University of Western Ontario.



Figure 2.2: Total knee replacement (TKR) system design: (a) schematic of the TKR system, and (b) enlarged view of the package with the harvesters.

#### 2.4.1 Harvester Design and Fabrication

Vertical contact mode triboelectric energy harvester has been used to generate the AC voltage signal from cyclic contact and separation motions. For providing the necessary contact and separation motions, the parts of the harvester are fixed inside a mechanical spring-controlled housing, as shown in Fig. 2.3(a). This is a preliminary package used for testing the generators and electronic system together. The upper tribolayer of the harvester, also a metal electrode, is CNC machined from micro-patterned Ti (100  $\mu$ m sawtooth ridge) and the lower tribolayer is fabricated by spin-coating PDMS mixtures on a back electrode that has been machined from a flat Ti. The upper and the lower titanium parts are designed according to the shape of a standard tibial tray, as shown in the exploded view of the design in Fig. 2.3(b). To make PDMS, first, the Titanium electrodes are cleaned with acetone and distilled water in an ultrasonic cleaner. Then, the PDMS

elastomer base and the curing agent are mixed in 10:1 weight ratio. The mixture is stirred thoroughly and degassed in a vacuum chamber. After degassing, the PDMS paste is spin coated at 500 RPM for 36s on the surface of the flat titanium. Finally, the PDMS coated titanium is cured at  $90^{\circ}C$  for 45 minutes on a hot plate [60].



Figure 2.3: Harvester Housing: (a) mechanical spring-controlled housing for the triboelectric harvester, and (b) exploded view of the design [60].

#### 2.4.2 Experimental Setup for Measurements

The experimental setup to generate the voltages using the triboelectric generator (TEG) is depicted in Fig. 2.4 [7, 12, 14, 15]. The setup consists of MTS 858 Servo Hydraulic Test System for conducting cyclic axial load, and a FlexTest controller for the amplitude tuning. The MTS has a built-in load cell to measure the applied force. The generated voltage signal is measured using a Keithley M6514 and an ExceLINX program. According to this experimental setup, for an applied force of 1500 N, the harvester produces a 120 V peak AC signal at a frequency of 1 Hz with a power of 20  $\mu$ W. This signal is shown in Fig. 2.5. The peak voltage and power of the harvested signal change as the applied force changes. For instance, at an applied force of 500 N, the signal peak reduces to 53 V and power is reduced to 6.5  $\mu$ W, as shown in Fig. 2.6 [59,60].



Figure 2.4: Experimental setup for measurements [7, 12, 14, 15].



Figure 2.5: Signal produced by the harvester at a force of 1500 N.



Figure 2.6: Signal produced by the harvester at a force of 500 N.

This harvested signal serves as both the power and data signal for the frontend electronic system. The power in the output harvested signal is used to operate the circuitry such that no external biasing is required. This signal is also digitized and ultimately used to monitor the load on the knee.

### 2.4.3 Innovations in the Proposed TKR Frontend Electronic Circuit

Although several TKR systems have been proposed in the literature [61–63], the proposed system in this thesis incorporates several key innovations:

• *The load monitoring is self-powered and can provide continuous force measurement.* Previous systems have incorporated batteries with limited lifespans or required external power supplied via inductive coupling [17,61,63,64]. Such systems limit the useful life of the sensor, and inhibit the ability to record data continuously. The proposed sensor in this research harvests energy through triboelectric mechanism based on contact electrification and electrostatic induction. Through this principle, power is harvested from the cyclic compressive loads between the femoral and tibial tray during normal

activities of daily living. This energy can be used to continuously power the electronic system and monitor the loads.

- *The energy harvester and the load sensor are combined in a compact system.* Previous systems have separate circuitry for receiving power and sensing loads. This inherently increases the size and complexity, and could potentially decrease system efficiency (resulting in a greater power demand). In the proposed system, the voltages generated via the triboelectric effect are proportional to the applied load, which means that the energy harvester itself can simultaneously act as a load sensing device. The proposed system utilizes the harvested energy to directly measure forces using fewer components, which reduces the system size.
- *The electronic system can accommodate a wide range of input peak voltages from the harvester*, hence the proposed design is able to monitor the load for various activities of daily living such as walking, running, jumping, etc.
- In order to limit memory and power requirements, important parameters (peak voltage and pulse width) from the harvested signal are extracted. This is helpful as storing the entire digital signal requires significant memory within the implant where the overall size is limited.
- The inductive link designed for wireless power transfer through the implant incorporates the actual implant package for real scenario. The designed inductive link is compact, efficient and is able to receive enough power for data transfer and monitoring.

# Chapter 3

# **PCB Prototype for Small Range of Cyclic Loads**

This chapter demonstrates the printed circuit board (PCB) prototype implementation of the frontend electronic system for a small range of cyclic loads (450 N to 650 N) and also demonstrates the PCB measurement results with the triboelectric harvester.

## 3.1 Electrical Model of the Harvester

The triboelectric harvester is first modelled electrically to facilitate circuit-level analysis. This electrical model produces an output AC signal similar to the actual harvester. This signal is then used to design the further components of the electronic system. Based on [65–68], the output voltage V of triboelectric harvester is given by (3.1) and the internal resistance r of the voltage source is given by (3.2),

$$V = -\frac{1}{C_M}Q + V_M - Ir, \qquad (3.1)$$

$$r = R(\frac{V_M}{V} - 1).$$
(3.2)

In (3.1),  $C_M$  refers to the capacitance between the two electrodes of the harvester, and  $V_M$  represents the voltage due to the separation of the polarized tribo-charges. The capacitive term originates from the ca-

pacitance between the two electrodes of the harvester, the voltage term arises because of the separation of the polarized tribo-charges, and the resistance term models the impedance of the voltage source [12]. The electrical model can be represented by a serial connection of these three components, as shown in Fig. 3.1.



Figure 3.1: Electrical model of the triboelectric harvester.

This electrical model is connected to an external load resistance *R* based on (3.2). Increasing the velocity of motion increases the frequency of AC voltage source  $V_M$ , which in turn decreases the matched resistance. The tribo-charge density does not affect the matched load resistance [12].

From basic thermodynamics theory,  $V_M$  and  $C_M$  depend only on the separation distance (*x*) and structural parameters, and not on motion parameters such as velocity and acceleration. Using the finite element method (FEM) and continuous fractional interpolation, a  $V_M$ -*x* and  $C_M$ -*x* relationship for a contact-mode triboelectric harvester has been generated, as given by (3.3) and (3.4) [65–68],

$$V_M = \frac{\sigma x}{\varepsilon_0},\tag{3.3}$$

$$C_M = \frac{\varepsilon_0 S}{d_0 + x},\tag{3.4}$$

where  $\sigma$  is tribo-charge surface density,  $\varepsilon_0$  is the permittivity of free space, *S* is area of dielectrics in the harvester and  $d_0$  is the effective dielectric thickness. The values of the physical and electrical parameters for the model based on the designed harvester are listed in Table 3.1 and Table 3.2, respectively.

S. No.	Parameter	Symbol	Value
1.	Dielectric 1	$\varepsilon_{r1}$	2.4
2.	Thickness of Dielectric 1	$d_1$	150µm
3.	Dielectric 2	E <sub>r2</sub>	1.6
4.	Thickness of Dielectric 2	$d_2$	0µm
5.	Effective dielectric thickness	$d_0 = d_1 / \varepsilon_{r1} + $	62.5µm
		$d_2 / \varepsilon_{r2}$	
6.	Area of dielectrics	S	Left oriented - 9.5 cm <sup>2</sup>
			Right oriented - 9.2
			cm <sup>2</sup>
7.	Max. Separation distance	x <sub>max</sub>	0.4 mm
8.	Tribo-charge surface density	σ	90 $\mu$ Cm <sup>-2</sup>

Table 3.1: Physical parameters for the model.

Table 3.2: Electrical parameters for the model.

S. No.	Parameter	Symbol	Value
1.	Internal resistance	r	218 MΩ
2.	External load resistance	R	220 MΩ
3.	Model capacitance	$C_M$	75 pF - 200 pF

Based on these values, SPICE simulations of the electrical model have been performed. The relationship between output voltage and the separation distance x is depicted in Fig. 3.2. The voltage increases with the distance x between the dielectrics.



Figure 3.2: Voltage output of the model as a function of separation distance *x*.

The measured output voltage (using the setup shown in Fig. 2.4) of the harvester is compared with the transient output voltage produced by the electrical model in Fig. 3.3 for an optimum load (matched resistive load of 220 M $\Omega$ ). As demonstrated by this figure, the model represents the harvester with sufficient accuracy. For the matched load, the model produces a signal of peak 89 V as compared to the 90 V peak signal generated by the actual harvester. The plot also shows the output voltage of the model when it is connected to the realistic load (the designed circuitry). For actual load circuits, the model generates a signal with a 88 V peak amplitude since the input impedance of the circuit at 1 Hz is 185 M $\Omega$ , lower than the optimum resistance of 220 M $\Omega$ .



Figure 3.3: Comparison of harvester and model output voltages at resistive and circuit load.

# 3.2 System Description

The architectural block diagram of the PCB prototype of the electronic system for the triboelectric knee implant for a small range of cyclic loads is shown in Fig. 3.4.



Figure 3.4: Architectural block diagram of the PCB prototype of the electronic system for small range of cyclic loads.

The system consists of two attenuators, a rectifier, a regulator, an 8-bit successive approximation register (SAR) ADC and an oscillator to generate the clock signal for ADC. All of these components are described in the following subsections.

#### 3.2.1 Attenuators

The electronic system comprises of two attenuators: Attenuator I (a two-stage *LC* filter common to both the power and signal paths), and Attenuator II (a single-stage *LC* filter and a diode) along the signal path to further condition the data signal for digitization. The high peak voltages in the harvested signal are converted into low peak voltages through Attenuator I, as shown in Fig. 3.5. This filter also acts as an impedance matching block to maximize power transfer from the load. The values of the circuit elements are chosen to achieve the desired attenuation (approximately a factor of 14) while ensuring high power efficiency. The equivalent series resistance (ESR) is considered during the design process for the inductors and capacitors (based on their respective data sheets [69, 70]), as listed in Table 3.3.



Figure 3.5: Two-stage *LC* filter to attenuate the high voltages in the harvested signal.

The output of this two-stage *LC* filter, *VS*2, is passed through Attenuator II, as shown in Fig. 3.6. The component values are tabulated in Table 3.4. Attenuator II ensures that the input signal for the ADC, *Vout* is within the acceptable range of the SAR ADC. A Schottky diode manufactured by the Infineon Technologies [71] is used as *D*2. The output capacitor, *C*5, is 0.18  $\mu$ F.

Table 3.3: Component values within the two-stage *LC* filter.

Element	Value
L1	56mH
ESR1	100.3Ω
L2	47mH
ESR2	88.83Ω
C1	5.6mF
ESR3	0.1Ω
C2	5.6mF
ESR4	0.1Ω



Figure 3.6: Schematic of Attenuator I to get the input data for the SAR ADC.

Element	Value
L3	47mH
ESR5	88.83Ω
C3	5.6mF
ESR6	0.1Ω

Table 3.4: Component values within Attenuator I.

#### **3.2.2 Diode Rectifier**

A diode rectifier is incorporated to convert the AC signal, VS2 from the two-stage LC filter into a DC voltage. The same diode as in Attenuator II is used. The output capacitor is 5.6 mF.

#### 3.2.3 LDO Regulator

The DC rectifier output is passed through a linear regulator to produce a stabilized voltage free from the variations in the input voltage. The regulator used here is a low-dropout (LDO) regulator manufactured by the Texas Instruments [72].

#### **3.2.4 SAR ADC**

A successive approximation register (SAR) analog-to-digital converter (ADC) is incorporated in the proposed system to convert the analog harvested signal into digital data. This digital data is then used to monitor the load on the knee. The SAR ADC used here is a commercially available chip manufactured by the Texas Instruments [73]. The output of the regulator is used as the supply voltage and the output of the Attenuator II is used as the analog input data to the ADC. Hence, the harvested signal is used as both the power and data signal. The clock frequency is chosen to be 10 kHz for sufficient accuracy since the input signal frequency is 1 Hz and is generated using a MEMS Oscillator manufactured by the Microchip Technology [74].

### **3.3** Simulation and Measurement Results

In this section, the ORCAD simulation results along with the PCB testing results are demonstrated and compared. The prototype PCB of the frontend electronic system is shown in Fig. 3.7.



Figure 3.7: PCB prototype of frontend electronic system for small range of cyclic loads.

### 3.3.1 Testing with the Function Generator and Signal Amplifier

In this section, the ORCAD simulation results are compared with the PCB measurement results for an input of 45 V peak sinusoidal waveform. The sinusoidal input signal to the PCB is generated using the function generator and signal amplifier. The ORCAD simulation also uses an ideal 45 V peak sinusoidal waveform.

Table 3.5: Comparison of ORCAD simulation and PCB measurement results for an input sine wave with a
peak voltage of 45 V.

S.No.	Circuit Component	PCB Test Output	ORCAD Simulation Output
1.	Attenuator I (Two-stage LC Filter)	3.4 V peak AC	3.42 V peak AC
2.	Diode Rectifier	2.5 V DC	2.6 V DC
3.	Regulator	2 V DC	2.08 V DC
4.	Attenuator II (ADC Data Input)	0.1 V to 0.9 V	-0.1 V to 0.93 V
5.	SAR ADC (for 0.7 V)	Digital Data 11010010	Digital Data 11010010
### 3.3.2 Testing with the Triboelectric Harvester

Here, the PCB measurement results are presented when tested with the actual triboelectric harvester. The results are also compared with the ORCAD simulations for a similar input generated through an electrical model of the harvester. The model generates a signal with similar electrical characteristics as the harvested signal (as described in Section 3.1). Fig. 3.8 shows the setup to test the PCB with the harvester.



Figure 3.8: Setup to test the PCB prototype with the triboelectric harvester.

Table 3.6 lists the PCB measurement results for a harvested signal of peak 53 V generated by the triboelectric harvester. It also shows the ORCAD simulation results that correspond to a similar 53 V peak voltage.

Table 3.6: Comparison of ORCAD simulation and PCB measurement results for a 53 V peak harvested signal.

S.No.	Circuit Component	PCB Test Output	ORCAD Simulation Output
1.	Attenuator I (Two-stage <i>LC</i> Filter)	4 V peak AC	4.1 V peak AC
2.	Diode Rectifier	3 V DC	3.1 V DC
3.	Regulator	2.4 V DC	2.38 V DC
4.	Attenuator II (ADC Data Input)	0.1 V to 1.1 V	-0.1 V to 1.11 V
5.	SAR ADC (for 0.9 V)	Digital Data 11111100	Digital Data 11111100

Fig. 3.9 shows both input voltages, one generated through the actual harvester and other generated through the electrical model for ORCAD simulations.



Figure 3.9: Input voltages for the measurement and simulation (harvester and electrical model output voltages), 53 V peak voltage.

Fig. 3.10 compares the output of the two-stage *LC* filter for the PCB test with the ORCAD simulation result. The PCB output signal has a peak voltage of 4 V as compared to the 4.1 V peak signal from the ORCAD simulation, hence the signals exhibit sufficient accuracy. Fig. 3.11 compares the output of the rectifier for the PCB test with the ORCAD simulation result. The PCB output is a 3 V DC signal while the ORCAD simulation produces a 3.1 V DC signal, certifying a good accuracy for the system. Fig. 3.12 compares the output of the regulator for the PCB test with the ORCAD simulation result. The PCB output is a 2.4 V DC signal while the ORCAD simulation produces a 2.38 V DC signal. Fig. 3.13 compares the output of the Attenuator II (the data input to ADC) for the PCB test with the ORCAD simulation result. The PCB output signal has a range from 0.1 V to 1.1 V. The ORCAD simulation also produces a signal in the similar range of -0.1 V to 1.11 V.



Figure 3.10: PCB and ORCAD results for the two-stage LC filter.



Figure 3.11: PCB and ORCAD results for the rectifier.



Figure 3.12: PCB and ORCAD results for the regulator.



Figure 3.13: PCB and ORCAD results for the ADC data input.

Fig. 3.14 compares the output of the ADC for the PCB test with the ORCAD simulation result. The input to the ADC is 0.9 V. The PCB output data is 11111100. The ORCAD simulation also produces the identical digital data of 11111100.



Figure 3.14: PCB and ORCAD results of the SAR ADC: (a) 0.9 V input and (b) digitized output data.

S.No.	Circuit Component	Power Consumption $(\mu W)$
1.	Attenuator I	0.8
2.	Diode Rectifier	0.5
3.	Regulator	1.95
4.	Attenuator II	0.6
5.	SAR ADC	1.5
Overall Power Consumption		5.35

Table 3.7: Power consumption of various blocks of the system.

The power consumed by each block is also analyzed, as listed in Table 3.7. The overall system consumes approximately 5.35  $\mu$ W power. The regulator and SAR ADC contribute the most to overall power consumption. The harvester produces approximately 6.5  $\mu W$  power when the peak voltage is 53 V. Thus, the proposed frontend electronic circuitry can be entirely self-powered. Note that the system power consumption is expected to be further reduced when the PCB is replaced with an integrated circuit implementation.

Similarly, Table 3.8 compares the PCB measurement and ORCAD simulation results for a harvested signal with a peak voltage of 60 V.

Table 3.8: Comparison of ORCAD simulation and PCB measurement results for a 60 V peak harvested signal.

S.No.	Circuit Component	PCB Test Output	ORCAD Simulation Output
1.	Attenuator I (Two-stage LC Filter)	4.6 V peak AC	4.55 V peak AC
2.	Diode Rectifier	3.4 V DC	3.42 V DC
3.	Regulator	2.7 V DC	2.69 V DC
4.	Attenuator II (ADC Data Input)	0.1 V to 1.12 V	-0.1 V to 1.05 V
5.	SAR ADC (for 0.9 V)	Digital Data 11001100	Digital Data 11001100

The measurement results discussed in this section validate the proposed prototype system implementation as PCB test results and ORCAD circuit simulation results sufficiently match. The slight mismatch between simulations and measurements is primarily due to the disparity between the input signals in each case. Specifically, for simulations, the input signal is produced by the electrical model of the harvester which approximates the actual signal generated by the harvester.

The prototype system described in this chapter works only for a relatively small range of cyclic loads (450 N to 650 N). This corresponds to input peak voltages ranging from 45 V to 65 V. Since the knee implant would be subject to a wider range of loads in practice, the frontend circuitry should be able to accommodate AC signals with a relatively large range of peak amplitudes (10 V to 150 V). For an harvested input signal of 10 V peak, the two-stage *LC* filter converts it to 0.7 V peak. Similarly, if the input signal is 150 V peak, it is converted to 11.5 V peak. Other components in the above mentioned PCB design cannot handle such wide range of 0.7 V to 11.5 V peak voltages. Thus, an improved PCB prototype is developed to handle a wider range of input voltages, as described in the following chapter.

# 3.4 Summary

A PCB prototype for a small range of cyclic loads has been developed for the frontend electronic system. The ORCAD simulation and PCB measurement results have been shown and they match with sufficient accuracy validating the functionality and feasibility of the proposed approach.

# **Chapter 4**

# **PCB Prototype for Wide Range of Cyclic Loads**

The PCB prototype described in the previous chapter can only monitor loads in the range of 450 N and 650 N, corresponding to peak voltages of 45 V to 65 V. In practice, the harvester output ranges from 10 V peak to 150 V peak voltage depending upon the applied force. Thus, linear *LC* filter based attenuation is not sufficient since the filter output would have a peak voltage of 11.5 V when the harvester output signal has peak voltage of 150 V. Furthermore, *LC* attenuation requires relatively large passive circuit elements due to low operating frequency of approximately 1 Hz. The architectural block diagram of the improved sensor circuitry designed for wide range of cyclic loads is shown in Fig. 4.1.



Figure 4.1: Architectural block diagram of the PCB prototype of the improved electronic system for wide range of cyclic loads.

In this design approach, the signal and power paths do not share a passive filter or attenuator. Instead, a non-linear attenuator is used for the power path, followed with rectification and regulation. For the signal path, a capacitive divider based linear attenuator is used with significantly lower capacitors. These blocks are explained in the following sections.

### 4.1 Linear and Non-linear Attenuator

The improved electronic circuitry comprises of two attenuators; a linear attenuator along the signal path and a non-linear attenuator along the power path, as shown in Fig. 4.2. The input impedance of the signal path is significantly larger to minimize current flow into the signal path. The input impedance of the nonlinear attenuator is adjusted to match the input impedance of the harvester ( $\approx 220 \text{ M}\Omega$ ) to maximize power transfer. Table 4.1 lists the values of all the passive components from the linear and non-linear attenuator. The equivalent series resistance (ESR) is also considered for all the capacitors (based on their datasheets [75, 76]).

S.No.	Component	Value	ESR
1.	C1	1nF	0.01Ω
2.	C2	15nF	0.06Ω
3.	C3	5nF	0.03Ω
4.	C4	10nF	$0.04\Omega$
5.	C5	0.5nF	0.01Ω
6.	C6	20nF	$0.07\Omega$
7.	C7	0.3nF	0.01Ω
8.	C8	15nF	0.06Ω
9.	C9	1nF	0.01Ω

Table 4.1: Component values of the linear and non-linear attenuator.





Along the power path, the signal from the harvester is attenuated through the first capacitive divider, C1 and C2 (attenuation factor is 3.5). This signal is passed through the diode rectifier, D2, and capacitor, C6, to provide the biasing for the amplifier, LM358-N, incorporated in this design. The signal from the first capacitive divider is again attenuated through the capacitive divider, C3 and C4 (attenuation factor is 1.5), and diode, D1. This step ensures that the input signal to the opamp, Vi is always less than the biasing signal, V+. C5 is a feedback capacitor that provides the desired attenuation between the input and output of the amplifier as described below. Referring to Fig. 4.2 and applying KCL, the following expressions are obtained,

$$\frac{Vin - V1}{Z1} \approx \frac{V1 - Vi}{Z3} + \frac{V1}{Z2},$$
(4.1)

$$\frac{V1 - Vi}{Z3} \approx \frac{Vi}{Z4} + \frac{Vi - Vout}{Z5},\tag{4.2}$$

where Z1, Z2, Z3, Z4 and Z5 are the impedances for the respective capacitances. Note that the current of the diodes D1 and D2 is neglected in (4.1) and (4.2). For the amplifier, the characteristic equation is (4.3),

$$Vout = A(Vi - Vout), \tag{4.3}$$

where A is the gain of the amplifier. Replacing (4.3) in (4.2) and rearranging yields (4.4),

$$\frac{Vout}{Vin} \approx k1 + \frac{k2}{A} + \frac{1}{A(Z5-1)},$$
(4.4)

where k1 and k2 are functions of impedances Z1 to Z5 and are constant at constant frequency. The amplifier, *LM*358-*N*, is a voltage controlled current source where the transconductance (and therefore the open loop gain *A*) changes with the input voltage [77]. Specifically, as the input voltage increases, the gain decreases, thereby achieving non-linear attenuation at the output of the amplifier. The accuracy of (4.4) is evaluated by comparing the analytic results with the simulated values (see Fig. 4.4) for different harvester output voltages. The average error is approximately 1.71%.

Along the signal path, linear attenuation is achieved via C7 and C8 (attenuation factor is approximately 62.5), followed with a rectification stage consisting of D3 and C9. This attenuation ensures that the input data to ADC is always less than the supply voltage Vdd of the ADC, which is determined by the power path. Note that the supply voltage of the ADC varies in the range of 1.8 V to 2.8 V depending upon the peak voltage of the harvested signal.

The voltages at the output of the linear and non-linear attenuators are illustrated in Fig. 4.3 for a harvested signal with a peak voltage *Vin* of 105 V. The input voltage of the amplifier, *Vi* has a peak voltage of 3.5 V, as shown in Fig. 4.3(b). The output voltage of the non-linear attenuator, *Vout* has a peak value of 3.1 V, as shown in Fig. 4.3(c). This signal is converted into a DC voltage for the ADC bias through the rectifier and regulator. The output of the linear attenuator (input data signal for the ADC) has a peak voltage of 1.65 V, as shown in Fig. 4.3(d). The peak input and output voltages of the linear and non-linear attenuator for different peak harvested voltages are tabulated in Table 4.2. The output peak voltages for the non-linear attenuator lie in the range of 0.16 V to 2.4 V. The ADC works properly for this range of bias voltage and input data signals, which are within its resolution range. Thus, the overall circuit can work for a wide range of harvester signals (from 10 V to 150 V peak voltage). Fig. 4.4 plots the peak linear and non-linear attenuator output voltages versus the peak harvester voltage.

S. No.	Peak Harvester	Peak Output of	Peak Output of
	Voltage (V)	Non-linear Attenuator (V)	Linear Attenuator (V)
1.	10	2.5	0.16
2.	30	2.6	0.48
3.	50	2.7	0.83
4.	70	2.8	1.12
5.	90	3.0	1.44
6.	110	3.15	1.76
7.	130	3.3	2.08
8.	150	3.5	2.40

Table 4.2: Peak input and output voltages of the linear and non-linear attenuator.



Figure 4.3: Output waveforms of the proposed linear and non-linear attenuator: (a) harvester output with 105 V peak voltage Vin, (b) amplifier input voltage Vi, (c) non-linear attenuator output voltage Vout, and (d) linear attenuator output voltage.



Figure 4.4: Peak linear and non-linear attenuator output vs. peak harvester output voltages.

# 4.2 Diode Rectifier

A diode rectifier is incorporated to convert the AC output signal from the non-linear attenuator, *Vout* into a DC voltage. The diode used is a switch-mode power rectifier manufactured by the ON Semiconductor [78]. The output capacitor used is 10 nF.

# 4.3 LDO Regulator

The DC rectifier output is passed through a linear regulator to produce a stabilized voltage free from the variations in the input voltage. The regulator used is a low-dropout (LDO) regulator manufactured by the Texas Instruments [72].

### 4.4 SAR ADC

A SAR ADC is incorporated in the proposed system to convert the analog harvested signal into digital data. This digital data is used to monitor the load on the knee. The SAR ADC used is a commercially available chip manufactured by the Texas Instruments [73]. The output of the regulator is used as the supply voltage, *Vdd* and the output of the linear attenuator is used as the analog input data to the ADC. Hence, the harvested signal is used as both the power and data signal for the ADC. The clock frequency is chosen to be 10 kHz since the input signal frequency is 1 Hz and is generated using a commercially available MEMS Oscillator chip [74].

### 4.5 Simulation and Measurement Results

In this section, the PCB measurement results are presented when tested with the triboelectric harvester for various cyclic loads. The results are also compared with the ORCAD simulations where a similar input signal is generated through the electrical model of the harvester. The prototype PCB of the improved fron-



Figure 4.5: PCB prototype of the improved frontend electronic system for wide range of cyclic loads.

tend electronic system for wide range of cyclic loads is shown in Fig. 4.5. Fig. 4.6 shows the experimental setup to test the PCB prototype with the triboelectric harvester.



Figure 4.6: Experimental setup to test the PCB prototype of the enhanced frontend electronic circuit with the triboelectric harvester.

Table 4.3 lists the PCB measurement results for a harvested signal of peak 100 V generated by the triboelectric harvester. It also lists the ORCAD simulation results for comparison. Fig. 4.7 illustrates the measured harvester output voltage and the simulated output voltage of the electrical model of the harvester.

Table 4.3: Comparison of ORCAD simulation and PCB measurement results for a 100 V peak harvested signal.

S.No.	Circuit Component	PCB Test Output	ORCAD Simulation Output
1.	Non-linear Attenuator	2.95 V peak	3.08 V peak
2.	Regulator	1.99 V DC	2.05 V DC
3.	Linear Attenuator (ADC Data Input)	1.55 V peak	1.6 V peak
4.	SAR ADC (for 0.9 V)	Digital Data 11100011	Digital Data 11100011



Figure 4.7: Measured harvester output voltage and the simulated output voltage of the electrical model of the harvester.

Fig. 4.8 compares the output of the non-linear attenuator for the PCB test with the ORCAD simulation. The PCB output signal has a peak of 2.95 V as compared to the 3.08 V peak signal from the ORCAD simulation, demonstrating sufficient accuracy. Fig. 4.9 compares the output of the regulator for the PCB test with the ORCAD simulation result. The PCB output is a 1.99 V DC signal while the ORCAD simulation produces a 2.05 V DC signal. Fig. 4.10 compares the output of the linear attenuator (data input to ADC) for the PCB test with the ORCAD simulation result. The PCB output signal has a peak of 1.55 V. The ORCAD simulation output signal has a peak of 1.6 V. Finally, Fig. 4.11 compares the output of the SAR ADC for the PCB test with the ORCAD simulation result. The input to the ADC is 0.9 V. The PCB output data is 11100011. The ORCAD simulation also produces the identical digital data.



Figure 4.8: PCB and ORCAD results for the non-linear attenuator output voltage.



Figure 4.9: PCB and ORCAD results for the regulator output voltage.



Figure 4.10: PCB and ORCAD results for the linear attenuator output voltage.



Figure 4.11: PCB and ORCAD results of the SAR ADC: (a) 0.9 V input and (b) digitized output data.

Similarly, Tables 4.4 and 4.5 list the PCB measurement results for harvested signals of peak 80 V and 150 V, respectively. The measurement results are compared with the ORCAD simulation results.

Table 4.4: Comparison of ORCAD simulation and PCB measurement results for a 80 V peak harvested signal.

S.No.	Circuit Component	PCB Test Output	ORCAD Simulation Output
1.	Non-linear Attenuator	2.81 V peak	2.9 V peak
2.	Regulator	1.81 V DC	1.89 V DC
3.	Linear Attenuator (ADC Data Input)	1.2 V peak	1.28 V peak
4.	SAR ADC (for 1 V)	Digital Data 11110011	Digital Data 11110011

Table 4.5: Comparison of ORCAD simulation and PCB measurement results for a 150 V peak harvested signal.

S.No.	Circuit Component	PCB Test Output	ORCAD Simulation Output
1.	Non-linear Attenuator	3.38 V peak	3.5 V peak
2.	Regulator	2.42 V DC	2.49 V DC
3.	Linear Attenuator (ADC Data Input)	2.31 V peak	2.4 V peak
4.	SAR ADC (for 1.2 V)	Digital Data 11110011	Digital Data 11110011

These test results validate the proposed design approach as the PCB and ORCAD results match with sufficient accuracy. Finally, the minimum change in the harvester voltage that can be sensed by the circuit with sufficient accuracy (i.e. voltage resolution) is characterized. This result is shown in Fig. 4.12 for various intervals of the peak harvester voltage. The resolution ranges from approximately 12 mV to 21 mV. The worst case resolution corresponds to harvester voltages greater than 111 V. Also, the difference between the digitized ADC output and corresponding harvester voltage is calculated to evaluate accuracy. For this comparison, the ADC output data is multiplied by the overall attenuation factor of the signal path, which is approximately 62.5. The maximum error is 3.48% whereas the average error is 2.83%.



Figure 4.12: Voltage resolution of the proposed electronic system for various intervals of the harvester voltage.

The power consumed by each block is also analyzed, as listed in Table 4.6. This system consumes approximately 5.1  $\mu$ W power. The regulator and SAR ADC contribute the most to overall power consumption. According to this result, the proposed frontend electronic circuitry can be entirely self-powered by a single harvester for cyclic loads 500 N to 2000 N, corresponding to harvester output peak voltages of 55 V to 150 V. To monitor loads less than 600 N, it is possible to utilize two harvesters in parallel or leverage supercapacitors to store excess energy. Note that less power is consumed as compared to the previous design described in Chapter 3 due to the much smaller passive devices with significantly lower ESR values.

S.No.	Circuit Component	Power Consumption ( $\mu$ W)
1.	Non-linear Attenuator	0.75
2.	Diode Rectifier	0.5
3.	Regulator	1.95
4.	Linear Attenuator	0.4
5.	SAR ADC	1.5
Total P	ower Consumption	5.1 μW

Table 4.6: Power consumption of various blocks within the circuit.

## 4.6 Summary

A PCB prototype of an improved frontend electronic system for a wide range of cyclic loads has been designed and fabricated. The ORCAD simulations and PCB measurement results have been presented, validating the functionality and feasibility of the proposed approach.

# Chapter 5

# ASIC Implementation of the Proposed Electronic System

In this Chapter, a potential application specific integrated circuit (ASIC) implementation of the proposed frontend electronic system is described. Even though some of the components of the ASIC implementation are similar to the PCB version, the ASIC implementation employs several different blocks to reduce on-chip storage space, as discussed in this chapter.

### 5.1 Block Diagram of the ASIC Implementation

The architectural block diagram of the proposed frontend electronic system is shown in Fig. 5.1. The electronic system consists of a linear and a non-linear attenuator, a rectifier, a low dropout regulator (LDO), a delta-sigma analog-to-digital converter (ADC), feature extraction circuitry and a power management system. The harvested signal flows through two paths (power path and signal path) since the harvested signal acts as a power signal to be rectified and data signal to be monitored. The non-linear attenuator is along the power path and provides the maximum power transfer. This power signal is then used to provide bias voltage for the ADC and other circuit components. There is no other external biasing required for any of the circuit components.





The linear attenuator is along the signal path and provides the input signal for feature extraction and digitization circuitries. The digital data from the ADC is then used to monitor the load on the knee. The electronic system also comprises of a simple power management system consisting of a diode, a switch and two supercapacitors. The supercapacitors are incorporated so that the excess input power can be stored.

The feature extraction circuitry is employed to extract important features (peak and pulse width) from the harvested signal (rather than digitizing the entire waveform) in order to save on both power consumption and memory (on-chip storage) requirements. The feature extraction and the power management circuitry are the distinctive features of the ASIC implementation as compared to the PCB prototype design. In the following subsections, detailed description of each component is provided.

#### 5.1.1 Linear and Non-linear Attenuator

The design of both the attenuator circuits has been described in detail in Section 4.1, Chapter 4. The schematic was shown Fig. 4.2. The power supply, V+, for the amplifier within the non-linear attenuator is initially supplied through the *Supercap I*. In the following cycles, V+ is generated from the output of the rectifier through a voltage multiplier circuit. For any cycle, if this supply is not sufficient, *Supercap I* provides the V+. Fig. 5.2 shows the output voltage waveform of the linear and non-linear attenuator for a harvested signal *Vin* of peak 88 V generated through the electrical model of the harvester. The input voltage of the opamp, *Vi* has a peak of 3.35 V, as shown in Fig. 5.2(b). This signal is attenuated through the opamp and the output voltage of the non-linear attenuator, *Vout* has a peak of 2.85 V, as shown in Fig. 5.2(c). This signal is converted into a DC biasing signal for the other circuit components. The harvested signal also passes through a linear attenuator and is attenuated into a 1.4 V peak signal, as shown in Fig. 5.2(d).

### 5.1.2 Negative Voltage Converter (NVC) Rectifier

This section describes the third component in the frontend electronic system, the rectifier. Specific voltage levels are needed to ensure correct functioning of the circuit. Hence, the alternating power signal



Figure 5.2: Output waveforms of the linear and non-linear attenuator: (a) 88 V peak input from the harvester model, *Vin*, (b) opamp input voltage, *Vi*, (c) non-linear attenuator output voltage, *Vout*, and (d) linear attenuator output voltage.

from the non-linear attenuator should be transformed to a specific shape and value required by the other components of the system. This transformation requires a rectification stage that can produce a DC voltage leve. This rectification should be as efficient as possible to reduce power loss. Hence, a Negative Voltage Converter (NVC) rectifier is incorporated in the proposed system as shown in Fig. 5.3 [14, 79–81].



Figure 5.3: Schematic of the Negative Voltage Converter (NVC) rectifier.

During the positive input cycle, when the input voltage is less than the threshold voltage ( $V_{ac} < V_{th}$ ), neither of the transistors conducts and no current flows through the circuit. When the input voltage becomes greater than the threshold voltage ( $V_{ac} > V_{th}$ ), transistors  $M_{P1}$  and  $M_{P2}$  provide a current path to the output. The operation is similar during the negative cycle where the transistors  $M_{N1}$  and  $M_{N2}$  provide the current path [14]. The input and output waveforms of the rectifier are shown in Fig. 5.4. The attenuated AC signal from the non-linear attenuator is converted into a DC voltage of 2.1 V. This signal is regulated and used by the other components of the system. The rectification efficiency achieved is approximately 71 %.

Due to the full gate cross-coupled topology, the NVC rectifier performs the rectification process with high efficiency as compared to other rectifiers. It achieves high power efficiency when the load is purely resistive. The efficiency, however, is reduced when a reactive element is added to the load due to the reverse current induced from output to the input port.



Figure 5.4: Input and output waveforms of NVC rectifier.

The NVC rectifier provides a low sensitivity to input voltage variations and is widely used in low voltage, high efficiency energy harvesters. Moreover, the NVC rectifier is highly suitable for implantable applications because of low power consumption [14].

### 5.1.3 Low Drop-out (LDO) Regulator

The fourth component of the frontend electronic system, regulator, is described in this chapter. A low drop-out (LDO) regulator, as shown in Fig. 5.5, converts the input rectified DC voltage into a regulated voltage of desired value within a specified tolerance range, while compensating for variations in the output current [82]. The LDO consists of a voltage reference circuit for producing the voltage  $V_{ref}$ , an error amplifier, EA, that produces an output voltage proportional to the difference between the reference and output voltages according to (5.1), a pMOS power transistor,  $M_P$ , to deliver the required current to output, resistive divider to determine voltage conversion ratio, and an output capacitor,  $C_L$ , to ensure stability.

$$V_a = V_{ref} - V_{fb}.\tag{5.1}$$



Figure 5.5: Schematic of a low-dropout (LDO) regulator.

The error amplifier consists of a differential input stage followed with a common source output stage, producing a DC gain of approximately 70 dB. The high gain ensures a high resolution error signal at the output. The phase margin is 57.81°, ensuring a stable operation. Reducing the drop-out voltage and quiescent current increases the power efficiency of the LDO. Hence, the power transistor is sized sufficiently large to lower the drop-out voltage and quiescent current of the regulator, while permitting the flow of the required large current to the load. Furthermore, diode-connected nMOS transistors,  $M_{N1}$ ,  $M_{N2}$ ,  $M_{N3}$  and  $M_{N4}$ , are used (instead of resistors) to further enhance the efficiency and reduce physical area. These transistors are sized to achieve the desired voltage conversion ratio of 0.76 [14]. Thus, the unregulated input voltage of 2.1 V is converted into a regulated voltage of 1.6 V. The power efficiency achieved is approximately 74%. The input and output waveform of the regulator are shown in Fig. 5.6.

It is important to note that the proposed LDO is free from any external bias voltage, making it applicable to energy harvesting implantable applications. This regulated DC signal is used as the biasing voltage, Vdd, for the ADC and other circuit blocks that need a supply voltage.



Figure 5.6: Input and output waveforms of the LDO regulator.

### 5.1.4 Delta-Sigma Analog-to-digital Converter

In this section, the design of Delta-Sigma Analog-to-digital Converter (ADC) used for monitoring the load on the knee is described. The output of the triboelectric harvester is used not only as the power signal, but also as the data signal to be digitized for load monitoring. The delta-sigma ADC is highly suitable for biomedical implants and energy harvesting applications because of its low complexity, low power, small area and it provides high resolution. Irrespective of the number of bits, a delta-sigma ADC consists of only one integrator and comparator, as shown in Fig. 5.7.

The analog input voltage,  $V_{in}$ , is first differentiated from the output of 1 bit digital-to-analog converter (DAC) using a switched-capacitor circuit. An integrator then adds the output of the differentiator to the value it has stored from the previous integration step. The output of the integrator is fed into a comparator, which compares the output with voltage,  $V_{mid}$ . It outputs a logic-high if the integrator output is greater than or equal to  $V_{mid}$ . Otherwise, it produces a logic-low. A 1 bit DAC feeds the output of the comparator to

the differentiator through a feedback loop. The output of the comparator then goes through a D flip-flop to produce the final digital bit stream. The schematic of the designed ADC is shown in Fig. 5.8 [14,42,83–85].



Figure 5.7: Block diagram of the Delta-Sigma ADC.



Figure 5.8: Schematic of the Delta-Sigma ADC.

The regulated output voltage, 1.6 V, acts as the *Vdd*. The voltages,  $V_H$ ,  $V_{mid}$ , and  $V_L$  are, respectively, 1.2 V, 0.8 V, and 0.4 V which are generated using on-chip voltage reference circuits. The capacitors,  $C_1$  and  $C_2$ , are kept at 100 fF. The two non-overlapping clocks,  $\phi 1$  and  $\phi 2$ , run at 50 kHz to reduce power consumption and ensure correct functioning of the triboelectric knee implant. The *reset* and *reset2* signals have the same frequency, as determined by (5.2),

$$f_R = \frac{f_{clk}}{2^N},\tag{5.2}$$

where  $f_{clk}$  is the clock frequency,  $f_R$  is the *reset* and *reset2* frequency and *N* is the number of bits. In the designed ADC, *N* is equal to 8, hence, the *reset* and *reset2* frequencies are 195 Hz. The signals  $V\phi 2$  and  $\overline{V}\phi 2$  are produced using a CMOS NAND gate and an inverter. The switched capacitor integrator has been designed incorporating the folded cascode operational amplifier. A folded cascode opamp is widely used in energy harvesting systems because of its high DC gain, high stability, low power, small area and high output voltage swing. The designed opamp produces a DC gain of 76.84 dB, and its phase margin is 52.35°, making it a stable and high resolution integrator. The comparator employed in the designed ADC is a CMOS latch comparator. It compares the output of integrator with  $V_{mid}$  in accordance with clocks  $\phi 1$  and  $\phi 2$ . The ADC is free from any external biasing.

Note that the output of the linear attenuator goes through the feature extraction circuitry to obtain the peak value of harvested signal, which is digitized through the ADC that is described in this section. To check the accuracy of the ADC, the analog and digital figures-of-merit, represented, respectively, by (5.3) and (5.4), are calculated. The percentage error between the two should be minimized.

$$Analog FOM = \begin{cases} \frac{V_{in} - V_L}{V_H - V_L}, & \text{if } (V_{in} < V_H) \\ \frac{V_H - V_L}{V_{in} - V_L}, & \text{if } (V_{in} > V_H). \end{cases}$$
(5.3)

$$Digital \ FOM = \frac{\text{Number of 1s in the output data}}{2^N},$$
(5.4)

where, N is the number of bits, which is equal to 8. Fig. 5.9 shows the digital output obtained from the ADC for an input of 0.81 V.



Figure 5.9: Digital bit stream from the ADC for an input of 0.81 V.

For an input voltage of 0.81 V, the analog FOM is 0.51 and from the digital bit stream, the digital FOM is 0.52. The percentage error between the two is 1.96%. The figure-of-merits are calculated for various input voltages and the average percentage error is approximately 3.47%, demonstrating that the designed ADC is sufficiently accurate to digitize the sensed gait signals.

#### 5.1.5 Feature Extraction Circuitry

The harvester output voltage signal depends on the knee loading force and contains important information on the fatigue, lifetime and impact of the implant on the surrounding tissues and bone. Continuous wireless transmission of the sensed data has a prohibitive power and memory/storage (in the form of nonvolatile memory) cost. The speed and energy overhead of writing into non-volatile memory limits the amount of data that can be stored between readouts to a few thousand data points [86]. The input signal is generated only with the knee movement, so the system spends significant time in inactive, sleep mode. Because of the self-powered nature of the system, there is no wake-up circuitry and the system logs data only when the energy is harvested. The entire transient signal waveform cannot be stored in the memory due to limited space. Signal compression is highly desirable. Due to the pulse-like nature of the signal for a gait cycle, certain features can be extracted for each of the pulses. Here, two important feature extraction circuits developed to extract two useful features of the harvester signal (peak voltage and pulse width) are presented. This is highly desirable to reduce the memory size as compared to the PCB prototype designs described in Chapters 3 and 4. In those designs, the data was digitized continuously and would require a large non-volatile memory for storage.

#### 5.1.5.1 Peak Detection Circuit

The schematic of the designed peak detector circuit is shown in Fig. 5.10 [87, 88]. The main idea behind this circuit is that the output signal follows the input signal only when the input is rising. To achieve this objective, the level of *Vin* is compared to its previous value stored in capacitor *C*, thus monitoring the increasing monotony of the signal. The output of the operational transconductance amplifier, OTA, inside the peak detector circuit is  $A \times Vin \times V peak$ , where *A* is the OTA gain.

Device *M*10 has two roles: first, charge the capacitor *C* for rising input signal and second, disconnect the input when the input falls. For rising input signal, Vin > V peak and hence device *M*10 charges *C* until Vin = V peak. This charging causes some hysteresis, depending on the value of capacitor *C* (the smaller the



Figure 5.10: Schematic of the peak detector circuit.

capacitor, the closer *V peak* tracks *Vin*, reducing the error between the two). At the peak point, the signal switches direction and *Vin* < *V peak*, causing *M*10 to switch off. *C* is then slowly discharged through the *M*11, which can be tuned using *Vs* [87].

The voltages *Vb* and *Vs* make sure that the peak detector circuit is turned off until the next cycle once the peak voltage has been detected in order to save power. Delta-sigma ADC sends this signal to trigger that it is ready to acquire and digitize the peak harvested voltage. The regulator output voltage is used as the *Vdd* for the peak detector. Table 5.1 lists the various design parameters of the peak detector circuit. The harvested peak in this example is 88 V generated through the electrical model, which is converted into a regulated DC voltage of 1.6 V, as previously described. Hence, the designed peak detector circuit is highly stable, achieves a high DC gain and consumes low power making it suitable for this application. Note that decreasing the output capacitance, although, reduces the error, degrades stability, increases power consumption and makes the design more prone to device mismatch.

S. No.	Design Parameter	Value
1.	Vdd	1.6 V
2.	DC Gain	63.5 dB
3.	Phase Margin	59°
4.	Power Consumption	0.49µ W
5.	Output Cap C	1 pF

Table 5.1: Design parameters of the peak detector circuit for a 88 V peak harvested signal.

Fig. 5.11 shows the output of the circuit for an input of 1.41 V (which is the peak output of the linear attenuator for a harvested signal of peak 90 V). The peak detected is 1.404 V. The % error between the two is only 0.43 %. Table 5.2 lists the output of the peak detector circuit for several peak harvested voltages. The average percentage error between the linear attenuator and peak detector circuit output is 0.37%.



Figure 5.11: Input and output waveforms of the peak detector circuit.
S. No.	Peak Harvester	Peak Linear Attenuator	Peak Detector	% Error	
	Voltage (V)	Output (V)	Output (V)		
1.	10	0.150	0.1495	0.33	
2.	30	0.450	0.448	0.44	
3.	50	0.813	0.810	0.37	
4.	70	1.100	1.097	0.27	
5.	90	1.410	1.404	0.43	
6.	110	1.700	1.693	0.41	
7.	130	2.000	1.995	0.25	
8.	150	2.350	2.340	0.43	

Table 5.2: Output voltages of the peak detector circuit.

Fig. 5.12 plots the peak output of the linear attenuator and the output of the designed peak detector circuit versus the peak harvester voltage. It can be seen that peak detector circuit output and linear attenuator peak voltage match with high accuracy. Note that the peak detector circuits are in general susceptible to the mismatch in the transistor sizes. Hence, considering that these device sizes can vary by up to 3 % (in the simulations), the average error between the linear attenuator and peak detector circuit output is found to be 0.98 %.



Figure 5.12: Peak harvester output vs. peak linear attenuator output and the output of the peak detector circuit.

This peak detector circuit output acts as the input data for the delta sigma ADC. The ADC output for the detected 1.404 V peak for the harvested signal of peak 90 V is shown in Fig. 5.13.



Figure 5.13: ADC output for the 1.404 V peak output from the peak detector for a 90 V peak harvested signal.

#### 5.1.5.2 Pulse Width Measurement Circuit

Another important feature of the harvested signal is its pulse width. Instead of storing the entire signal, it is highly feasible to rather store the pulse width. The pulse width can be measured using the voltage comparing or voltage thresholding circuit and a counter. The harvested signal is first attenuated to make it suitable for feature extraction, as shown in Section 5.1.1. Then, the voltage comparing circuit converts this attenuated analog input signal into a digital pulse. The threshold is set just above the baseline for

comparison. Second, this digital pulse is converted into a digital value using a counter. The counter output is then digitized through the delta-sigma ADC. The architectural block diagram is shown in Fig. 5.14.



Figure 5.14: Architectural block diagram of the pulse width measurement circuit.

Voltage comparators either use positive feedback or no feedback at all (open-loop mode) such that the output switches between two saturated states, because the voltage gain of the amplifier equals A in the open-loop mode. The comparator output switches between the negative and positive supply rails, V- and V+ respectively, on the application of varying input signal when compared with the preset threshold value. The opamp based comparator operates in the non-linear region and acts like a digital bistable device as triggering causes it to switch between two possible outputs, V+ or V-. Hence, the voltage comparator acts simila to a 1-bit analog-to-digital converter, as the input signal is analog with the output behaving digitally. The comparator can be characterized using (5.5) and (5.6),

If 
$$Vin > Vth$$
, then  $Vout = V+$ , (5.5)

If 
$$Vin < Vth$$
, then  $Vout = V$ -. (5.6)

If *Vin* is less than *Vth*, the output is equal to the negative supply voltage, resulting in a negative saturation of the output. If *Vin* exceeds *Vth*, the output voltage rapidly switches to the positive supply voltage, resulting in a positive saturation of the output.

The regulator output voltage is used as the supply voltage V+ for the comparator circuit designed for this system. The digital output of the comparator is then passed through the counter. The output waveforms are illustrated in Fig. 5.15.



Figure 5.15: Waveforms related to the pulse width measurement circuit: (a) harvester voltage, (b) output of the linear attenuator, (c) output of the voltage comparator circuit, and (d) output of the counter.

The harvester output, 88 V peak signal as generated by the electrical model (as shown in Fig. 5.15(a)) gets attenuated into a 1.4 V peak digital signal, as shown in Fig. 5.15(b). The attenuated signal is the input for the pulse width measurement circuit. The output of the comparator is shown in Fig. 5.15(c). This signal is converted into a digital value equal to the pulse width (0.39 sec) (as shown in Fig. 5.15(d)) through the counter. The output is then digitised through the ADC and is shown in Fig. 5.16. The % error between the actual pulse width and the measured pulse width is 1.1%. Also, the designed pulse width measurement circuit can measure the pulse width from 0.1 sec to 1.5 sec and the average error between the actual and measured values is approximately 1.55 %.



Figure 5.16: Waveforms of the pulse width measurement circuit: (a) pulse width (output of the counter) and (b) digitized output of the ADC.

#### 5.1.6 Power Management System

In this section, the design of a simple power management system consisting of a switch, a diode and two supercapacitors is described, as shown in Fig. 5.1. The harvester peak voltage and input power changes as

the applied force varies. Fig. 5.17 plots the apparent power generated by the Polyethylene package-harvester with no upper spacer for various sinusoidal forces [89].



Figure 5.17: Apparent power generated by the Polyethylene package-harvester with no upper spacer for various sinusoidal forces [89].

Table 5.3 lists the harvested power for different peak voltages for the single Polyethylene packageharvester with no upper spacer. This power increases when the harvesters are connected in parallel, as shown in Fig. 5.17.

Table 5.3: Harvested power for different peak voltages for the Polyethylene package-harvester with no upper spacer [60].

S. No.	Peak Voltage (V)	Harvested Power ( $\mu W$ )
1.	10	0.8
2.	50	5.1
3.	60	7.1
4.	80	10
5.	120	20
6.	150	25

Table 5.4 lists the power consumption of the various circuit components in the potential ASIC implementation. The total power consumed is approximately 6.15  $\mu$ W.

S.No.	Circuit Component	Power Consumption $(\mu W)$
1.	Non-linear Attenuator	0.78
2.	NVC Rectifier	0.55
3.	LDO Regulator	1.75
4.	Linear Attenuator	0.38
5.	Delta-Sigma ADC	1.35
6.	Peak Detection Circuit	0.49
7.	Pulse width Measurement Circuit	0.85
Overall Power Consumption		6.15

Table 5.4: Power consumption of various circuit components of the proposed ASIC system.

The Polyethylene package-harvester generates power greater than 6.15  $\mu$ W for forces greater than 500 N. Since the circuit consumes approximately 6.15  $\mu$ W, the harvested power is either in excess or is deficient. Hence, a power management system is needed that can store the excess power and supply it in the case of power deficiency.

Without the power management system, if the energy generated by the harvester is higher than the energy instantaneously consumed by the electronic system, the excess energy is wasted within the regulator. The power management system senses the voltage at the input of the regulator and enables the transfer of the excess energy to a storage device, a supercapacitor. Supercapacitors can have a large number of charge and recharge cycles. The power management system also ensures optimal charging and discharging of the supercapacitor to maximize its service life. The energy stored in the supercapacitor provides power when there is no AC signal supplied by the harvester. This is critical to enable data processing when an activity is finished, but there is data that need to be further processed and stored.

The power management system comprises of a diode, a switch and two supercapacitors, Supercap I and Supercap II, as shown in Fig. 5.1. The Supercap I is required for two reasons: first, to operate the switch to control the non-linear attenuator, and second, to provide power to run the non-linear attenuator when the input power is not sufficient. The switch is an nMOS transistor to turn on or off the non-linear attenuator so as to reduce the power consumption. Turning off the non-linear attenuator saves significant power when the system is in idle state. This Supercap I is charged from the input harvested power through a diode. This input

diode rectifies the alternating input signal from the harvester to control/charge the Supercap I. Supercap II is required so that it can provide power to run the delta-sigma ADC and feature extraction circuitry when the input power is not sufficient.

#### 5.1.6.1 Supercapacitor Modeling and Design

Although supercapacitors have lower energy density than batteries, their power density is much higher, which enables their use in applications that require short-term high power draw, such as medical equipment and electric vehicles. In particular, despite the lower energy density, their very long life cycles make them promising to be used as an energy storage element (ESE) for energy harvesting systems, thereby justifying the use of supercapacitors in the proposed system.

The modeling and design of the two supercapacitors mentioned above, Supercap I and Supercap II, is discussed here. The circuit model of a supercapacitor is shown in Fig. 5.18 for n branches [90,91]. It is an *RC* ladder circuit with a voltage dependent capacitance in the first branch.



Figure 5.18: RC ladder circuit model of a supercapacitor.

For both the supercapacitors, Supercap I and Supercap II, for simplicity, a three-branch model (n = 3) is considered as it provides a suitable level of accuracy for the supercapacitor and less computational effort, as shown in Fig. 5.19.



Figure 5.19: Three-branch equivalent *RC* ladder circuit of a supercapacitor.

The first branch represents the "fast" response of the supercapacitor, and the subsequent two branches model the "intermediate" and "long" responses. The model can be extended to further stages if longer time-periods are required. This model includes a voltage-dependent capacitor in the first branch to represent the realistic nonlinear behavior of the device. The use of multiple branches enables the long-term charging process to be modeled, which is dependent on the physical distribution of electrical charge [91]. Equations (5.7) to (5.10) below are used to design the supercapacitor and compute the values of the components in the three-branch *RC* ladder circuit for both Supercap I and Supercap II. In these equations,  $\alpha$  represents the equivalent capacitance of a linear capacitor holding the same charge as a double-layer capacitor at the same voltage. Resistors have been substituted for conductances and the voltage-dependent capacitor *Cv* has been used to represent the nonlinear behavior of the supercapacitor [91].

$$\alpha = (C_1 + \frac{C_{\nu} \cdot V_1}{2}), \tag{5.7}$$

$$\alpha.\dot{\mathbf{V}}_1 = G_1.\frac{I + G_2(V_2 - V_1) + G_3(V_3 - V_1)}{G_1 + G_2 + G_3},$$
(5.8)

$$C_2.\dot{V}_2 = G_2.\frac{I + G_1(V_1 - V_2) + G_3(V_3 - V_2)}{G_1 + G_2 + G_3},$$
(5.9)

$$C_3.\dot{\mathbf{V}}_3 = G_3.\frac{I + G_2(V_2 - V_3) + G_1(V_1 - V_3)}{G_1 + G_2 + G_3}.$$
(5.10)

Table 5.5 lists the values of the elements in the *RC* ladder circuit for both the supercapacitors, Supercap I and Supercap II that are 4.2 F and 3.2 F, respectively.

S.No.	Circuit element	Value for Supercap I	Value for Supercap II
1.	$C_{v}$	0.841 F/V	0.621 F/V
2.	$C_1$	2.51 F	1.81 F
3.	<i>C</i> <sub>2</sub>	1.89 F	0.98 F
4.	<i>C</i> <sub>3</sub>	3.22 F	2.59 F
5.	$R_1$	0.2 Ω	0.1 Ω
6.	$R_2$	122 Ω	110 Ω
7.	<i>R</i> <sub>3</sub>	800 Ω	700 Ω

Table 5.5: Element values in the RC ladder circuit for both the supercapacitors.

The harvested power at 1000 N of cyclic load ( $\approx 14 \ \mu$  W) is larger than the required power to run the circuit. Hence, the excess power is used to charge the supercapacitors through the diode and regulator, as shown in Fig. 5.20. Fig. 5.20(a) shows the voltage signal generated by a single triboelectric harvester at 1000 N. The peak of the signal is 100 V. Fig. 5.20(b) shows the corresponding current signal. Fig. 5.20(c) shows the output of the diode. This signal charges the Supercap I. Since the input power is larger than the consumed power, the excess power from the regulator output (as shown in Fig. 5.20(d)) is also used to charge the Supercap I and Supercap II. Fig. 5.21 shows the charging profile of both the supercapacitors. It can be seen that the charging time of the supercapacitors is 80 seconds and 100 seconds for, respectively, Supercap I and Supercap II.

Through the stored charge in the supercapacitors, the circuit is able to be self-powered even for the forces that generate less power than 6.15  $\mu$ W. For instance, the circuit can now operate even at 400 N (generated power is approximately 3  $\mu$ W). The harvested voltage and non-linear attenuator output waveform that correspond to 400 N cyclic load are shown in Fig. 5.22.



Figure 5.20: Charging the supercapacitors through the harvested power at 1000 N of cyclic load: (a) harvester voltage at 1000 N, (b) corresponding current at 1000 N, (c) output voltage of the diode, and (d) output of the regulator.



Figure 5.21: Charging profile of the supercapacitors.



Figure 5.22: Non-linear attenuator waveforms at 400 N cyclic load. The attenuator operates via the power supplied by Supercap I: (a) harvester voltage at 400 N, and (b) output of the non-linear attenuator.

Also, when the supercapacitors are charged to their fullest capacity, they can be used to operate/selfpower the circuit at minimum force (200 N) for approximately 4.67 hours. Hence, through the use of supercapacitors, the input harvested power can be efficiently managed, making load monitoring a selfpowered procedure for a wide range of cyclic loads.

### 5.2 Summary

A potential ASIC implementation of the proposed frontend electronic system has been presented. Various components of the system (linear and non-linear attenuator, rectifier, regulator and ADC) are discussed. Feature extraction circuitry is also demonstrated to extract important characteristics from the harvested signal to reduce on-chip memory/storage requirement. The use of supercapacitors is also discussed to manage the input harvested power and make the system applicable to a wide range of cyclic loads.

# Chapter 6

## **Wireless Power Transfer**

In order to reduce the power and size requirements of a biomedical implant, the use of batteries as the primary source of energy within the implant is typically avoided [92]. Instead, the battery is externally placed and power is transmitted wirelessly through inductive coupling. Even external batteries need to be small, lightweight, and should have a long lifetime due to portability, economic and aesthetic reasons [93]. In the previous chapters, it was demonstrated that the harvested power is enough for operating the frontend electronic circuitry to monitor the knee load, but external power is required for data transfer. Therefore, a wireless power transfer mechanism is needed to transmit the digitised data to an external reader device. The investigation of this wireless power transfer mechanism is the focus of this chapter.

Tibiofemoral forces are highly significant in total knee arthroplasty. These forces determine wear and cold flow in polyethylene, stress in the implant and implant–bone interface, and in the underlying bone [61]. Tibial prostheses have been instrumented with force transducers in measuring the *in vitro* tibial forces [94]; however, direct measurement of *in vivo* tibial forces has not been reported. Telemetry is a safe and accurate means of obtaining force data from implanted transducers and has been used in the hip, spine, and femur to measure *in vivo* forces [95, 96]. Knee is more complex and theoretic estimates of tibiofemoral forces have varied significantly depending on the mathematical models used and on the type of activity analyzed. Research work shown in [61] presented a telemetry system to monitor and measure the intra-articular tibial forces. A titanium tibial prosthesis design was instrumented with force transducers, a micro-transmitter,

and an antenna. The load cells were placed at four corners of the tibial tray. The analog signals from these four load transducers were converted to a digital signal. The microprocessor then generated a modulated RF signal which was transmitted through an antenna. The receiver contained a receiving antenna, an oscillator and a level converter. The system was powered through the magnetic near field coupling. AC magnetic field was produced by an external coil driven with AC current, which in turn generated an AC voltage signal in a receiving coil placed within the magnetic field. They could generate 40 mW of power in the internal coil which was sufficient to power their system. The mean absolute error in their load measurement was found to be 1.5%.

In [97], a ligament laxity telemetry system architecture was demonstrated for a knee replacement prosthesis. The designed system provided an indication on the balance of the lateral ligaments, which can be used to estimate the wear out of the polyethylene part of the prosthesis and also the patient rehab. Piezo ceramics were used both as pressure sensors and power generators. A possible ASIC architecture of the ligament balance measuring system was presented which consisted of an ADC, a transceiver and a digital data processing core. The worst case power consumption of the digital core was reported to be 0.003 mW.

An inductive link based wireless power transmission comprises of an external primary coil and a secondary coil located within the implanted device. The secondary coil changes the loading impedance, thus modulating the reflecting magnetic field. The primary coil detects the changes in the magnetic field and demodulates the transmitted data. The logged sensing data in a non-volatile memory of the implant, with the presence of a coil on the implant, can then be read by an external primary coil. The power for the operation of the implant during the readout is harvested via the inductive link.

The optimization of the coil size and shape and the characterization of the wireless channel is performed using a finite element method based simulator (Ansys HFSS - High Frequency Structure Simulator). HFSS is an electromagnetic (EM) field simulation software that is used for designing high-frequency electronic products such as antennas, microwave or RF components, filters, high-speed interconnects, inductive coils, and printed circuit boards. It is widely used to design high speed electronics found in communications systems, biomedical and Internet-of-Things (IoT) products. The design procedure of the inductive link for the designed smart knee implant is discussed in this chapter and the HFSS simulations are presented.

## 6.1 Design of the Inductive Link

First, the medium between the two inductive coils is modeled. The cross-section view of that model is shown in Fig. 6.1. A 3D view of the implant that houses the electronic system and harvesters is shown in Fig. 6.2. The implant consists of a UHMWPE bearing layer, a package, and three M3 (steel) screws. Various dimensions of the package are depicted in Fig. 6.3 [59].



Figure 6.1: Cross-section view of the inductive link model.



Figure 6.2: Top view of the implant.



Figure 6.3: Various dimensions of the package [59].

The lumped circuit model of the inductive link is shown in Fig. 6.4, which accurately approximates the link characteristics up to a transmitting frequency of 100 MHz [93]. L1 and L2 represent the individual inductances and M is the mutual inductance.  $R_{S1}$  and  $R_{S2}$  represent the parasitic resistances, while  $C_{P1}$ and  $C_{P2}$  are the parasitic capacitances of the coils.  $C_1$  and  $C_2$  capacitances are added in order to achieve resonance with the inductors L1 and L2.  $R_S$  and  $R_L$  are the source  $V_S$  and load resistances. The design of the coils and the operating frequency depend primarily on the application. From electromagnetics theory, it can be observed that M, L1 and L2 are dependent on the coil geometries, which includes their relative distance, orientation, and number of turns.

Hence, coil geometries play an important role on the power efficiency of the link. An iterative procedure is followed to calculate various parameters of the primary and secondary printed spiral coils (PSC) of the inductive link. The top view of the square shaped PSC is shown in Fig. 6.5. Square shaped coils are chosen to obtain the maximum power transfer area.  $d_o$  and  $d_i$  are outer and inner diameters of the coil, respectively. w is the line width and s is the spacing between the turns of the coil. The primary coil is embedded into a specialized reader device and the secondary coil is located within the implant package. The implantable coil has a silicone coating material which decreases the parasitic resistance between coil and tissue and it also increases the receiver coil quality factor [98].



Figure 6.4: Schematic of the lumped equivalent circuit model of the inductive link.



Figure 6.5: Top view of the square shaped printed spiral coil (PSC).

Initially, all of the coil parameters are optimized through MATLAB to obtain a reasonable starting point for HFSS simulations. The coils parameters in MATLAB are obtained via the following steps [93,99]. The flowchart of this process is also illustrated in Fig. 6.6.



Figure 6.6: Iterative printed spiral coil (PSC) design flowchart.

*Step 1 - Design Constraints*: Various parameters affect wireless link efficiency because of factors related to the implantable device application and fabrication technology. The application usually determines the size constraints depending on where it is implanted inside the body. The technology on the other hand indicates the minimum size features that result in acceptable yield in manufacturing. Table 6.1 lists several constraints which are set while designing the inductive link for the triboelectric knee implant.

S.No.	Parameter	Value		
1.	Thickness of Package	9 mm		
2.	Thickness of muscle	5 mm		
3.	Thickness of fat	12 mm		
4.	Thickness of skin	3 mm		
5.	Thickness of air	10 mm		
6.	Substrate thickness	0.61 mm		
7.	Substrate dielectric constant	4.4 (FR4)		
8.	Minimum conductor width	150 µm		
9.	Minimum conductor spacing	150 µm		
10.	Implanted coil outer diameter, $d_{02}$	8 mm		
11.	Minimum coil inner diameter, $d_{imin}$	1 mm		
12.	Primary coil copper thickness	34.7 µm		
13.	Secondary coil copper thickness	4 μ <i>m</i>		

Table 6.1: Design Constraints for inductive link design. Note that FR4 (flame retardant) epoxy glass is a widely used substrate for implantable electronics.

Step 2 - Initial Values and Frequency Optimization: Before starting the optimization process, a set of initial values needs to be selected. For a pair of identical spiral filament coils, the optimal fill factor  $\phi$  is 0.43 [93,99]. This fill factor is 0 when all the turns are concentrated on the perimeter like filament coils, and becomes 1 when the turns spiral all the way to the center of the coil. For  $d_{o2} = 8$  mm, according to (6.1),

$$\phi = \frac{d_o - d_i}{d_o + d_i},\tag{6.1}$$

 $d_{i2} = 4 \text{ mm} [93,99]$ . The optimal value for  $d_{o1}$  depends on the relative distance of the coils, which is typically not fixed and has a certain range. Therefore, depending upon the application and design constraints, it can

be chosen as the nominal distance where the coils are located for most of the time during normal operation or the maximum distance, which indicates the worst case scenario for power transmission. As a starting point, an initial value for  $d_{o1}$  is chosen which is optimized later based on other design constraints. Then, the frequency of operation is optimized with respect to the power transfer efficiency. Higher frequencies are attenuated more by the body, but on the other hand they enable smaller coils. Thus, an optimized frequency for less attenuation and smaller coil size should be chosen. The link power efficiency depends on coupling coefficients and quality factors of the primary and secondary coils, as described by (6.2),

$$\eta_{12} = \eta_1 \cdot \eta_2 = \frac{k^2 Q_1 Q_L}{1 + k^2 Q_1 Q_L} \cdot \frac{Q_L}{Q_2 + Q_L}.$$
(6.2)

Based on this optimization, the frequency of operation is chosen as 90 MHz.

Step 3 - Size and Fill Factor of Primary Coil: In this step, the optimization of the diameter and fill factor of primary coil is performed based on the initial values set in the previous step at the chosen frequency of operation. The optimization objective is power efficiency. For this optimization,  $d_{o1}$  and  $\phi 1$  are varied in a wide range around their initial values. Based on this step, the  $d_{o1}$ ,  $\phi 1$ ,  $d_{i1}$ , and  $n_1$  values are optimized.

Step 4 - Fill Factor and Line Width of Secondary Coil: After temporarily optimizing the geometry of the primary coil, the size of the secondary coil is optimized. Here, the line width  $w_2$  and fill factor  $\phi 2$  are varied and optimized in a wide range around their initial values while calculating the power efficiency. Based on this optimization, the values for  $d_{o1}$ ,  $\phi 1$ ,  $d_{i1}$ , and  $n_1$  are chosen.

Step 5 - Size and Line Width of Primary Coil: In this step, the primary coil is further optimized. The width  $w_1$  is increased towards its optimal value (found in Step 3) while providing room for this change by increasing  $d_{o1}$ . Increasing  $w_1$  is likely to increase the efficiency by reducing resistance and increasing quality factor. However, it also requires larger  $d_{o1}$ . Ultimately, the  $w_1$  and  $d_{o1}$  values that achieve the desired efficiency are chosen.

Step 6 - Iteration by going back to Step 3: The coil geometries from Step 5 significantly improve com-

pared to the initial values. However, further improvement is possible by iterating over Steps 3–5. Iterations can continue until the improvement in efficiency saturates. Table 6.2 lists the optimized values of the design after several iterations.

S.No.	Parameter	Value
1.	Outer diameter, $d_{o1}$	32 mm
2.	Inner diameter, $d_{i1}$	12.6 mm
3.	Turns, $n_1$	4
4.	Width, $w_1$	1.5 mm
5.	Fill factor, $\phi 1$	0.43
6.	Outer diameter, $d_{o2}$	10 mm
7.	Inner diameter, $d_{i2}$	4 mm
8.	Turns, $n_2$	3
9.	Width, $w_2$	0.6 mm
10.	Fill factor, $\phi 2$	0.43
11.	Frequency	90 MHz

Table 6.2: Optimized parameter values of the inductive link.

### 6.2 HFSS Simulations

The inductive coils optimized in Section 6.1 are designed in HFSS software for electromagnetic simulations. The medium between the coils is modeled as depicted in Fig. 6.1. The side view of the HFSS setup that shows the placement of primary and secondary coils is illustrated in Fig. 6.7.

#### 6.2.1 Frequency of Operation

The reflected impedance between the primary and secondary coils depends on the frequency of operation due to the difference in the tissue absorption. In this analysis, the coils are assumed to be completely aligned (their centers are aligned) for high efficiency and minimal loss. The input power to the external/primary coil is 2.5 W, which satisfies the safety regulation for implantable biomedical applica-



Figure 6.7: Side view of HFSS setup illustrating the inductive link and 3D package.

tions [58, 100]. The medium between the coils is modeled as air, skin, fat, muscle and package as shown in Fig. 6.1 with an overall distance of approximately 39 mm between the two coils. Fig. 6.8 shows the received power obtained at various frequencies. It can be seen that the maximum received power (-4.5 dBm or 0.355 mW) is obtained at 90 MHz Fig. 6.8 also shows the received power obtained at various frequencies for the scenario when the implant (including package) is removed from the medium between the coils to understand the impact of package on the wireless link. Removal of the package does not change the optimum frequency of operation. When only the coils are simulated (without the implant or any tissue layer), the received power is 1.45 W for a the same input power. This analysis demonstrate that the tissue layers have a large impact on the received power whereas the implant has only a small impact. Table 6.3 lists the power transfer efficiency for these three cases.

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S.No.	HFSS Simulation Scenario	Power Transfer Efficiency (PTE) %
1.	Without tissue and implant	58
2.	With tissue and without implant	0.178
3.	With tissue and implant	0.142



Figure 6.8: Received power at various frequencies.

Intuitively, PTE determines how well the coils are coupled to each other. The highest efficiency across the inductive link is achieved when both *LC* tanks (coils) from Fig. 6.4 are tuned at the carrier frequency, as given by (6.3),

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 (C_2 + C_{P2})}}.$$
(6.3)

The expression for inductive link power transfer efficiency is given by (6.2). It depends on several parameters such as the coupling coefficient k, and quality factors  $Q_1$ ,  $Q_2$  and  $Q_L$ . The quality factors in turn depend upon the resistance, capacitance and frequency of operation [99].

### 6.2.2 Mutual Inductance

A printed spiral coil can be considered as a set of several single-turn coils with shrinking diameters, each connected in series. Hence, if the mutual inductance between a pair of single-turn coils in parallel planes can be determined, the overall mutual inductance M can then be evaluated by adding the partial mutual inductance values between each turn on one coil and all the turns on the other coil. Using Maxwell's equations,  $M_{ij}$  between a pair of parallel circular single-turn coils can be found using (6.4),

$$M_{ij} = \mu \pi \sqrt{r_i r_j} \int_0^\infty J_1(x \sqrt{\frac{r_i}{r_j}}) J_1(x \sqrt{\frac{r_j}{r_i}}) \times J_0(x \frac{\gamma}{\sqrt{r_i r_j}}) \exp\left(-x \frac{D}{\sqrt{r_i r_j}}\right) dx, \tag{6.4}$$

where  $r_i$  and  $r_j$  are the radii of the coils,  $J_0$  and  $J_1$  are, respectively, the Bessel functions of zeroth and first order, D is the relative distance between the coils,  $\mu$  is the medium permeability, and  $\gamma$  is the lateral misalignment [93]. By adding the partial mutual inductances between every two turns, the overall M can be evaluated using (6.5),

$$M = g \sum_{i=1}^{n_1} \sum_{j=1}^{n_2} M_{ij}(r_i, r_j, D),$$
(6.5)

where g is PSC shape dependent parameter which is 0.95, 1.0, and 1.1 for a pair of hexagonal, circular, and square-shaped PSCs with equal diameters, respectively [93]. Fig. 6.9 shows the relationship between mutual inductance and the rotation angle at the chosen frequency of operation (90 MHz).



Figure 6.9: Mutual inductance vs. rotation angle at 90 MHz.

Specifically, it presents the values of mutual inductances *M* between the two coils for different rotation angles from 0 to 90 deg. Since perfectly aligned coils provide minimal loss, the highest mutual inductance is obtained when the angle is 0 deg. This value reduces as the rotation angle changes. When the coils are simulated along with the implant and tissue layers, the maximum mutual inductance is 15 pH. This increases to 18 pH when the implant is removed from the HFSS simulation, demonstrating that implant does not have major impact on the mutual inductance.

#### 6.2.3 Coupling Coefficient

Another parameter related to mutual inductance M is the coupling coefficient k, defined by (6.6),

$$k = \frac{M}{\sqrt{L_1 L_2}},\tag{6.6}$$

where  $L_1$  and  $L_2$  are the individual coil inductances. Coupling coefficient is integral in determining the inductive link efficiency. It is the fraction of the magnetic flux that is produced by the current in one coil which is linked with the other coil. If k = 1, flux produced by one link is completely linked with the other coil and is called magnetically tightly coupled. Alternatively, if k = 0, flux produced by one link does not couple with the other link and is called magnetically isolated. The coupling coefficient depends on the distance between the coils, their core, mutual orientation and winding.

Fig. 6.10 shows the relationship between coupling coefficient k and the mutual inductance M for the designed inductive link, demonstrating a linear dependence. When the coils are simulated along with the implant and tissue layers, the coupling coefficient k is 0.15 at 15 pH. Coupling coefficient increases to 0.2 at 18 pH when the implant is removed from the HFSS simulation.



Figure 6.10: Coupling coefficient vs. mutual inductance at 90 MHz.

A wireless link for a similar application is described in [101], where the design of an efficient inductive link for transcutaneous powering and communication for a knee prosthesis is shown. Various parameters of the primary and secondary coils such as the distance between them, size, number of turns, width are discussed. Two schemes to choose the placement of the coils are compared: horizontal placement inside the polyethylene insert and vertical placement inside the insert. The first scheme is finally chosen as it provides higher coupling coefficient and quality factors and is more robust when the knee is bent. The radius of the primary coil is 60 mm. The dimensions of the secondary spiral coil are determined by the prosthesis. The short side of the elliptical spiral coil is 18 mm, and the long side has a length of 29 mm. The optimal distance between the turns is reported as 2.5 times the wire diameter for the solenoid type coil, and 1.5 times the wire diameter for the spiral coil when the conductors used have diameters of 1 and 0.4 mm, respectively. The optimal number of turns is 6 and 9 for primary and secondary coils, respectively. The frequency of operation is 27 MHz.

# 6.3 Summary

An inductive link has been designed and different tissue layers between the two coils have been modeled to characterize signal attenuation across air, skin, fat, muscle and the actual package. The HFSS simulations support the design procedure and the designed inductive link provides sufficient received power, which can be used for wireless data transfer for the smart knee implant. The effect of implant (package) and different tissue layers on the power efficiency, mutual inductance and coupling coefficient is also analysed.

# **Chapter 7**

### **Conclusion and Future Work**

Continuous and optimal monitoring of the load is a promising technique in improving the functioning of knee implants. This work presents a novel frontend electronic system for the triboelectric knee implant. The electronic system is powered only by the power generated by the triboelectric harvester. A summary of this research is provided in this chapter and several future directions are outlined.

### 7.1 Thesis Summary

This thesis demonstrates the design of a smart knee implant for total knee replacement (TKR), as shown in Fig. 7.1. The TKR with the smart knee implant is shown in Fig. 7.1(a). It consists of the package, the triboelectric harvesters and the frontend electronic system between the harvesters, as shown in the enlarged view in Fig. 7.1(b). The enlarged view of the electronic system prototype (which is the main focus of this research) is also shown in Fig. 7.1(c).

The triboelectric harvester converts mechanical energy from an applied axial load to electrical energy, which powers the electronic circuitry for load monitoring. The harvester has the ability to generate a voltage signal based on the triboelectric effect when it undergoes a cyclic loading from activities of daily living. The harvesters and the electronic system are placed inside the 3D package.



Figure 7.1: Total Knee Replacement (TKR) system: (a) TKR with the smart knee implant, (b) enlarged view of the smart knee implant, and (c) enlarged view of the frontend electronic system prototype to monitor the knee load.

The signal generated by the harvester changes as the applied force varies. The triboelectric harvester generates a power of 20  $\mu$ W under an equivalent gait load of 1500 N at the frequency of 1 Hz. The load digitization circuitry consumes approximately 5  $\mu$ W making it entirely self-powered. The circuit consists of a power and signal path since the harvester output signal acts both as power signal to be rectified and data signal to be digitized. The circuitry is designed to maximize power transfer along the power path.

In Chapter 3, the design of a PCB prototype of the frontend electronic system that is entirely powered by the harvested energy is presented. The measurement results with the triboelectric harvester are demonstrated in order to justify the functionality and feasibility of the proposed approach. The test results match the ORCAD simulation results with sufficient accuracy. This design, however, works only for a small range of input voltages and consists of passive devices with large form factor, making it unsuitable for implantable applications. Therefore, in Chapter 4, a PCB prototype of a modified frontend electronic system for a large range of input voltages (cyclic loads) is demonstrated. Moreover, smaller passive components are used, making it more feasible for implantable applications. For cyclic loads greater than 500 N, the harvester generates more power than the system power consumption of  $5.1 \,\mu$ W. Hence, triboelectric power generation is a viable technique for harvesting energy and power load sensing circuit for TKR applications.

In Chapter 5, a potential ASIC implementation of the design is described. It consists of supercapacitors for efficiently managing the input power from the harvester. There is also a feature extraction circuitry to extract important features (peak and pulse width) from the harvester signal in order to reduce the power and storage requirements. Finally, in Chapter 6, wireless power transfer through the knee implant is investigated for data transfer. The design process of the inductive link consisting of the primary and secondary coils for effective data transmission is discussed.

### 7.2 Proposed Future Work Directions

#### 7.2.1 Full ASIC Fabrication

The potential ASIC implementation discussed in Chapter 5 has been supported only with the simulation results. One of the future directions is to fabricate and test the design to experimentally validate the proposed approach. A small implantable prototype chip can be developed and the entire TKR system (triboelectric harvesters, electronic system, and 3D package) can be tested together.

### 7.2.2 Testing for Different Activities of Daily Living (ADL)

Another interesting direction for future work entails testing the designed TKR setup under simulated ADL profiles *in vivo* joint simulator for more accurate measurements. The implant and the circuit can then be reoptimized based on measurement results. This study would make the design more robust and accommodating to a wider range of realistic activities.

#### 7.2.3 Testing the Inductive Coils

The design of inductive coupling based wireless power transfer through the knee implant was shown in Chapter 6. The HFSS simulation results were presented for various parameters such as mutual inductance, coupling coefficients, power loss, and efficiency. One of the future steps can be to fabricate and test the designed primary and secondary coils. The experimental characterization of the fabricated link can then be performed by inserting meat slices of different thicknesses between the coils [102].

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