In-Package Spiral Inductor Characterization for High Efficiency Buck Converters

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***Abstract*—The applicability of package-embedded spiral inductors to switching buck converters is demonstrated. In the first step, the design and characterization process of package-embedded spiral inductors is investigated via comprehensive full wave electromagnetic simulations, while considering a realistic, multi-layer flip-chip package. An interleaved multi-phase buck converter with an *array of package-embedded spiral inductors* is developed in the second step. The converter produces an output voltage of 0.9 V from 1.2 V input voltage while supplying a load current of 1 A. The flexibility of the package is exploited to obtain a relatively high inductance, enabling a reduced switching frequency. Lower switching frequency minimizes the dynamic loss, thereby increasing the power efficiency. According to the extracted results of the overall layout, power efficiency of approximately 89% is achieved with 3% output ripple voltage.**

I. Introduction

High efficiency and low cost voltage converters and regulators are critical elements for most of the low power design strategies such as multi-voltage design [1], dynamic voltage frequency scaling [2], and low swing/voltage clocking [3]. The efficacy of these low power design methods highly depends upon the quality of the voltage regulator.

Three types of voltage converters exist [4]: 1) linear converters such as low-dropout (LDO) regulators, 2) switched-capacitor based DC-DC converters, and 3) switching buck converters. LDO regulators are cost effective and fast, but suffer from low power efficiency (typically less than 60%, which is exacerbated as the conversion ratio increases or output voltage decreases) [2]. Power efficiency is enhanced by switched capacitor converters at the expense of a slow regulation process. Obtaining multiple conversion ratios is also challenging [5]. Finally, switching buck regulators can achieve the highest efficiencies, but require a high quality inductor that is typically off-chip and discrete. Existing works have investigated the feasibility of increasing switching frequency to reduce the required inductance. In this case, however, the dynamic loss increases, thereby reducing the power efficiency [6].

An intermediary solution (between a fully on-chip inductance and an off-chip discrete inductance) is investigated in this paper where the inductor is built within a flip-chip package in a spiral fashion whereas all of the other components are integrated on-chip. Note that this approach is different from discrete inductors integrated into a package since in the proposed case, the inductor is built using existing metal interconnects within the package layers and fabricated at the same time as the package. Although package-embedded inductors have been discussed [7], the primary emphasis has been on building inductors and experimental characterization. The applicability to switching buck converters has not been investigated. As demonstrated in this work, a higher inductance with a reasonable quality factor is achieved by exploiting the greater flexibility of package as compared to die area. This package-embedded spiral inductor is connected to the die via low resistance controlled collapse chip connection (C4) bumps. Thus, the switching frequency of the buck regulator can be reduced to minimize dynamic power loss and enhance efficiency. Specifically, in this work, the frequency is 50 MHz, which is significantly lower than existing works with on-chip inductors (477 MHz in [6], 200 MHz in [8], 170 MHz in [9], and 300 MHz in [10]). Furthermore, an *array of package-embedded spiral inductors* can be developed for an interleaved multi-phase buck regulator architecture (see Fig. 1), further enhancing the efficiency and output ripple.

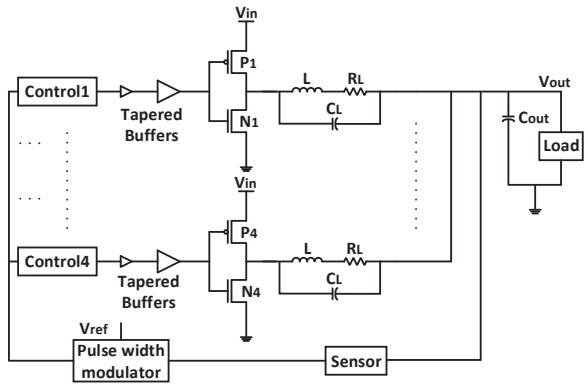

Fig. 1: **Interleaved multi-phase switching buck regulator topology.**

The rest of the paper is organized as follows. A brief background on switching buck converters is provided in Section II. The design and modeling process for package-embedded spiral inductors using a commercial field solver including the applicability of these inductors to an interleaved multi-phase buck regulator is described in Section III. Extracted simulation results are presented in Section IV. Finally, the paper is concluded in Section V.

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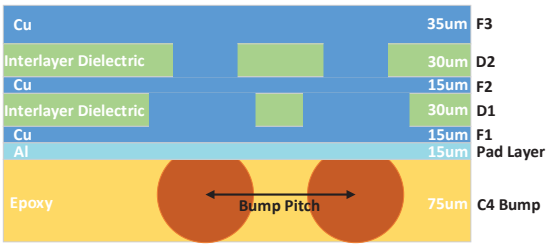

Fig. 2: **Cross-section of the multi-layer flip-chip package where spiral inductors are built.**

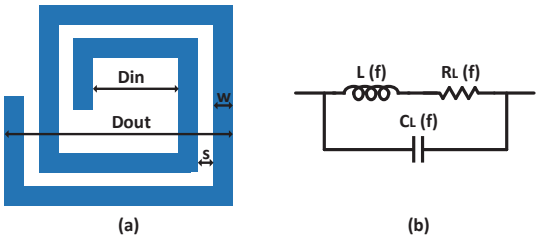

Fig. 3: **Typical spiral inductor: (a) physical characteristics, (b) equivalent electrical circuit.**

II. Background

A typical single-phase buck converter consists of 1) a switch network that generates an AC signal, 2) a second order low pass filter that passes the DC component of the AC signal to the output, and 3) feedback path that regulates the output voltage by changing the duty cycle of the AC signal [4]. The low pass filter, consisting of an inductor and capacitor, is a critical element since the output voltage characteristics depend upon the quality of this filter. The parasitic effective series resistance (ESR) of the inductor plays an important role in the resistive loss and the overall performance of the buck converter. A larger inductance (required to reduce ripple) typically produces a larger ESR, which in turn increases the resistive loss and causes a non-negligible voltage drop at the output, particularly if the load current is sufficiently high.

For a single phase buck converter, the required inductance L and the minimum required capacitor C_{out} can be determined by the following, assuming that the output voltage ripple cannot exceed 5% of the output voltage [4],

$$L = \frac{(V_{in} - V_{out})D}{2\Delta I_L f_s}, C_{out} \geq \frac{5(V_{in} - V_{out})D}{4V_{out}Lf_s^2}, \quad (1)$$

where V_{in} and V_{out} are, respectively, input and output voltages, D is duty cycle, ΔI_L is the current ripple (half of the peak-to-peak current), and f_s is switching frequency.

Single-phase buck converters are sufficient for applications with low load current, but power dissipation and efficiency suffer at higher currents due to large ripple. Thus, interleaved multi-phase buck converters have been considered for applications with high load current since peak ripple current can be effectively reduced [11]. The size of the individual inductors (and therefore ESR) and output capacitance can be reduced without increasing the output ripple, as shown in Fig. 1.

In a multi-phase buck converter, the normalized ripple current I_{Rip_norm} is determined by [12],

$$I_{Rip\_norm} = P \times \frac{[D - \frac{\lfloor m \rfloor}{P}] \times [\frac{1+\lfloor m \rfloor}{P} - D]}{(1-D) \times D}, \quad (2)$$

where D is the duty cycle, P is the number of phases, and $m = D \times P$. This equation is important to determine the number of phases based on the required ripple current, as further discussed in Section III-B1. Package-embedded spiral inductors provide a unique opportunity for interleaved architecture since an array of spiral inductors can be built using the package metal layers and fabricated as part of the package fabrication process.

III. Proposed Method

The design and characterization of package embedded spiral inductor using HFSS is described in Section III-A. The applicability of the package-embedded inductors to switching buck regulators is explained in Section III-B.

A. Package-Embedded Spiral Inductor Characterization

A multi-layer flip-chip package is assumed. Cross-section of the package illustrating each layer is shown in Fig. 2 [7]. Three copper metal layers exist with two different thicknesses. The top metal (F3) is 35 μm thick whereas the bottom two metal layers (F1 and F2) are 15 μm thick. There is an aluminum pad layer with 15 μm thickness. The dielectric layers (D1 and D2) are 30 μm thick and consist of flame retardant (FR4) epoxy. The inductor is built on layer F3 and is connected to the C4 bumps located at the bottommost layer filled with epoxy with 75 μm thickness [13]. The C4 bumps connect the inductor terminals to the on-chip components.

This package structure is modeled using a commercial finite element method (FEM) based full wave electromagnetic field solver ANSYS HFSS (high frequency structural simulator). The DC and low frequency characteristics are analyzed using ANSYS Q3D Extractor.

A conventional spiral inductor is illustrated in Fig. 3(a) where the important physical characteristics are highlighted such as internal diameter D_{in}, external diameter D_{out}, width w, and spacing s. The following relationship holds among these parameters, assuming that the number of turns T is an integer,

$$D_{in} = D_{out} - (2T+1) \times w - (2T-1) \times s. \quad (3)$$

An electrical equivalent circuit is shown in Fig. 3(b) assuming a one-terminal, two-port extraction. The frequency dependent $L(f)$, $C_L(f)$, and $R_L(f)$ refer, respectively, to the extracted inductance, capacitance, and effective series resistance (ESR). These frequency dependent components are extracted by analyzing the Y parameters from HFSS [14]. Specifically, Y_{11} is

$$Y_{11}(f) = \frac{1}{R_L(f) + j\omega L(f)} + j\omega C_L(f). \quad (4)$$

Assuming the series capacitance $C_L(f)$ varies only marginally with frequency [15] (this component can be extracted from Q3D Extractor at a low frequency), the extraction of $R_L(f)$ and $L(f)$ is performed using the following procedure:

- Subtract the admittance $C_L(f)$ from Y_{11} and convert the remaining term into impedance,

$$Z_{11_{RL}}(f) = R_L(f) + j\omega L(f). \quad (5)$$

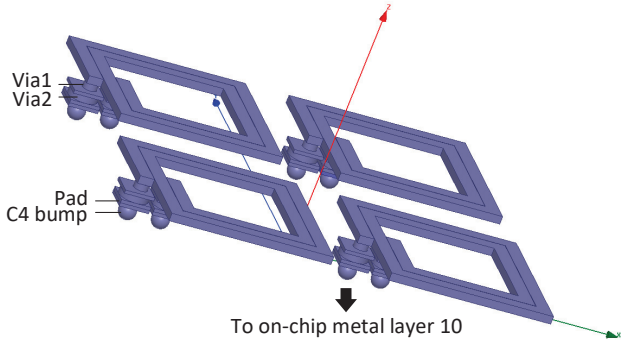

Fig. 4: **Array of package-embedded spiral inductors modeled in full wave electromagnetic simulator HFSS.**

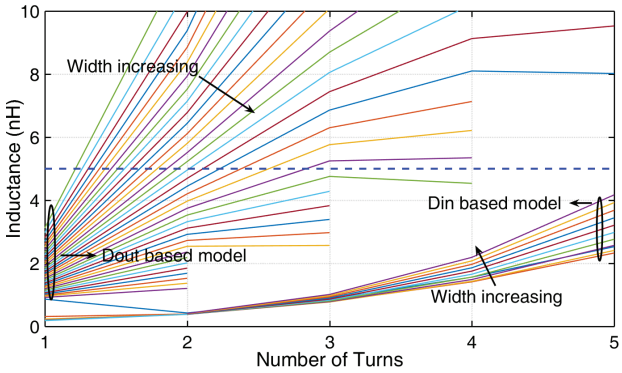

Fig. 5: **Design space of the package-embedded spiral inductor as a function of number of turns and width at constant spacing, thickness, and frequency.**

- Plot the real and imaginary parts of $Z_{11_{RL}}(f)$ at the frequency of interest to extract $R_L(f)$ and $L(f)$ from HFSS.

An array of four inductors modeled in HFSS considering the package structure described above is shown in Fig. 4. To determine the physical parameters of the package-embedded spiral inductor (T, D_{in}, D_{out}, w, s), the procedure described in [16] is used. Two methods are considered to maximize the quality factor:

- D_{in} based model: D_{in} is kept constant at 50 μm. The width is progressively increased until D_{out} reaches 1 mm, the available dimension for the package area.
- D_{out} based model: D_{out} is maintained constant at 1 mm. The width is progressively increased until D_{in} reaches the minimum allowable value. Note that according to (3), as width is increased, D_{in} is reduced.

For both techniques, spacing is constant at 2 μm to maintain the tight coupling of the magnetic field. Note that these analyses are achieved at different number of turns, producing a large design space, as illustrated in Fig. 5. From this design space, the inductors that satisfy the required inductance can be extracted (for example, see the dashed horizontal line at 5 nH). Here, every design point that intersects with the horizontal line satisfies the required inductance. It is important to note that for inductors in the range of several nanohenry and above, the minimum ESR occurs within the D_{out} based model since the D_{in} based model requires a large number of turns to reach the required inductance, which increases the ESR.

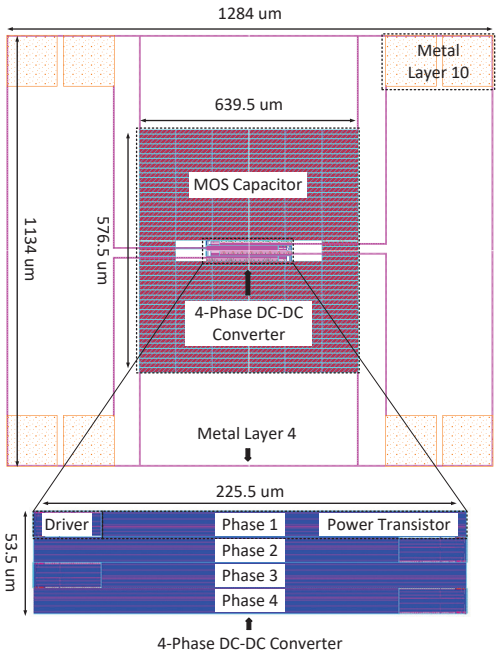

Fig. 6: **The on-chip layout of the 4-phase converter, illustrating the power transistors, drivers, MOS capacitors, and metal layer 10 for connection to the package-embedded inductors.**

B. Application to Interleaved Switching Buck Converter

1) Four-Phase Buck Converter Operation and Optimization: Package-embedded spiral inductors designed and characterized in the previous section are used for a switching DC-DC converter designed in the 45 nm technology. The converter converts an input voltage of 1.2 V to an output voltage of 0.9 V while supplying 1 A of load current. An interleaved four-phase buck converter is developed to reduce the inductor and therefore ESR without increasing the output ripple. Output capacitance can be significantly reduced with interleaving technology due to less ripple. Specifically, a 2.5 nF capacitor is used in this work and implemented as MOS-C, consuming an area of 0.37 mm^2. The layout of the MOS-C is carefully drawn to avoid a high ESR that would increase the output voltage ripple.

2) Physical Layout of the Proposed 4-Phase Buck Converter: The package-embedded inductors and the C4 bumps are implemented and characterized using HFSS. The C4 bumps connect the inductor terminals to on-chip metal layer 10, as shown in Fig. 6. The filter capacitance is implemented as MOS-C and located above and under the tapered buffers and power transistors. The overall area of the converter and on-chip MOS capacitor are 639.5 μm $\times$ 576.5 μm. After considering the area of top vias and overhead connections, the area occupied by the overall circuitry is 1284 μm $\times$ 1134 μm (see Fig. 6).

IV. Simulation Results

The four-phase DC-DC converter is designed to operate at a switching frequency of 50 MHz. The power efficiency of the converter as a function of inductor size is shown in Fig. 7. The highest efficiency of 88.32% is achieved when each inductor in the interleaved topology is approximately 5 nH.

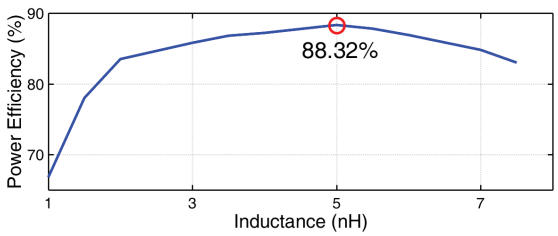

Fig. 7: **Power efficiency of an interleaved four-phase buck converter as a function of inductance.**

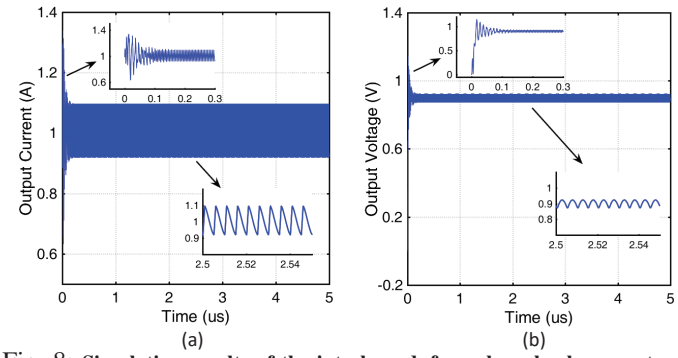

Fig. 8: **Simulation results of the interleaved, four-phase buck converter with package-embedded spiral inductors: (a) output current, (b) output voltage.**

Thus, *an array of package-embedded spiral inductors* is characterized in HFSS where each of the four inductors is 5 nH and occupies 1 mm^2 area (see Fig. 4). The overall area consumed in the package by spiral inductors is 4.076 mm^2. To determine the physical characteristics of the inductors, the procedure described in the previous section is followed. After the entire design space is obtained, as shown in Fig. 5, the number of turns and widths that produce the required inductance are analyzed for quality factor. The highest quality factor of 11.8 is achieved with a 2-turn spiral inductor and 64 μm width. The ESR and series capacitance are extracted, respectively, as 132 mΩ and 50.7 fF.

The four-phase interleaved buck converter is simulated in SPICE with the electrical model of the package-embedded spiral inductors after RC impedance extraction. The current ripple on each phase is 399 mA. The maximum and minimum output current in steady state are, respectively, 1.095 A and 0.919 A. Thus, the output current ripple is 95 mA, 9.5% of the output current, as depicted in Fig. 8(a). Note that the output current ripple is much smaller than the ripple on each phase due to the interleaved multi-phase topology.

The transient response time when current abruptly changes from 0 to 1 A is 0.1 μs, as shown in Fig. 8(a). The corresponding output voltage is plotted in Fig. 8(b). The overshoot when the load current abruptly falls to zero is 0.3 V. The output voltage ripple in the steady state is only 26.8 mV.

The simulation results are compared with several prior work, as listed in Table I. At comparable conversion ratios, this work achieves the highest power efficiency while supplying a load current of 1 A. The switching frequency is lowest due to the package-embedded spiral inductors.

TABLE I: Comparison of the proposed buck converter with existing approaches.

Parameter	[8]	[9]	[10]	This work
Inductor Type	glass epoxy, on-chip	stacked, on-chip	stacked, on-chip	spiral, in-package
Inductor value	22 nH	2 nH	2 nH	5 nH/phase
Conversion ratio	0.75	0.73	0.785	0.75
Output load	70 mA	190 mA	125 mA	1 A
Switching frequency	200 MHz	170 MHz	300 MHz	50 MHz
Power efficiency	71.3%	77.9%	74.5%	88.32%
Voltage ripple	10%	4.4%	1.17%	2.8%

V. Conclusion

An interleaved multi-phase switching buck converter with package-embedded spiral inductors has been proposed. Design and characterization process of the spiral inductors built within the flip-chip package has been demonstrated through comprehensive electromagnetic field simulations using HFSS. A high power efficiency of 88.32% is achieved since the switching frequency can be lowered by exploiting the greater flexibility of the package structure.

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