Energy Efficient AC Computing Methodology for Wirelessly Powered IoT Devices

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***Abstract*—Charge-recycling based AC computing has recently been proposed to significantly increase energy efficiency in wirelessly powered devices. The power consumption is reduced by 1) eliminating the rectification and regulation stages of traditional DC computing and 2) recycling charge through AC computing. An alternative charge-recycling mechanism is proposed in this paper that does not require a phase shifter or peak detector, thereby reducing the overhead power consumption. Simulation results in 45 nm technology demonstrate that an additional 60% reduction in power consumption can be achieved while operating at the same frequency. As compared to the traditional case, power consumption is reduced by more than an order of magnitude.**

I. Introduction

Energy harvesting has been studied to power traditional wireless sensor nodes, internet-of-things (IoT), and similar low power applications where energy autonomy is a critical challenge. Light, motion, and radio frequency (RF) signals are promising energy sources for emerging IoT devices [1], [2]. Extensive research literature exists on solar cells, kinetic and wireless energy harvesters [3], [4]. Despite the higher power densities, a primary issue in motion and light based energy harvesters is the significant temporal variation of the harvested power due to changing conditions of the power source. Alternatively, wireless/RF power harvesting has recently received considerable attention due to the ubiquity of RF energy around the worlds such as mobile phones, TV/radio broadcast, and mobile base stations [5], [6]. Dedicated wireless power sources have also been utilized as in RFIDs where the passive tag harvests wireless energy transmitted by the reader [7]. Despite the relatively low power densities, RF power harvesting can provide *continuous* energy. A primary issue in existing wireless power harvesting methods is the strong dependence of the harvested power on the distance between the source and load due to signal attenuation throughout the space.

Recently, charge-recycling based AC computing paradigm has been offered as a promising solution for wireless power harvesting, as depicted in Fig. 1 [8], [9]. In this approach, the wirelessly harvested signal is directly used for computation by leveraging charge-recycling theory. Specifically, efficient charge recovery logic (ECRL) has been used with a phase shifter and peak detector. An alternative mechanism based on pass transistor adiabatic logic (PAL) [10] is proposed in this paper for AC computing in wirelessly powered devices. Simulation results demonstrate 60% reduction in power consumption as compared to [8].

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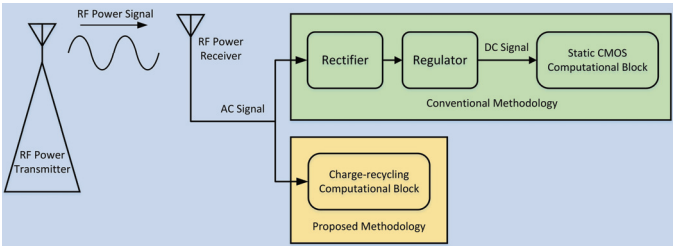

Fig. 1. **Leveraging charge-recycling based AC computing to increase energy efficiency in wirelessly powered devices.**

A rectifier-free RFID tag based on charge-recycling has also been recently developed [11]. The primary objective, however, is on footprint (and therefore cost) reduction rather than energy efficiency. The tag area is reduced by approximately 80% at the expense of an order of magnitude increase in power consumption [11].

The rest of the paper is organized as follows. A brief background is provided in Section II. The proposed approach to AC computing in wireless devices is described in Section III. Simulations results and power comparison are presented in Section IV. Finally, the paper is concluded in Section V.

II. Background

A traditional RF energy harvester receives the propagated electromagnetic wave with an antenna (or coupling coil) and converts the alternating power into a stable DC voltage for driving the computational units [12]. This step typically consists of a full wave rectifier, a voltage multiplier, and a regulator. When the harvested RF signal is converted to a DC supply voltage, significant energy is lost due to low power efficiencies of the rectification process. Additional power is lost during the regulation step [13]. Even with the state-of-the-art RF-DC converters, at least 30% of the power is lost during this stage [12].

An alternative approach is to eliminate the rectification and regulation steps, and directly use the received AC signal for computing, as proposed in [8]. This approach leverages efficient charge recovery logic (ECRL) [14], which unfortunately requires four AC signals with 90° phase difference. Furthermore, the bulk terminals of the PMOS transistors still require a DC voltage to ensure reverse biased source/drain

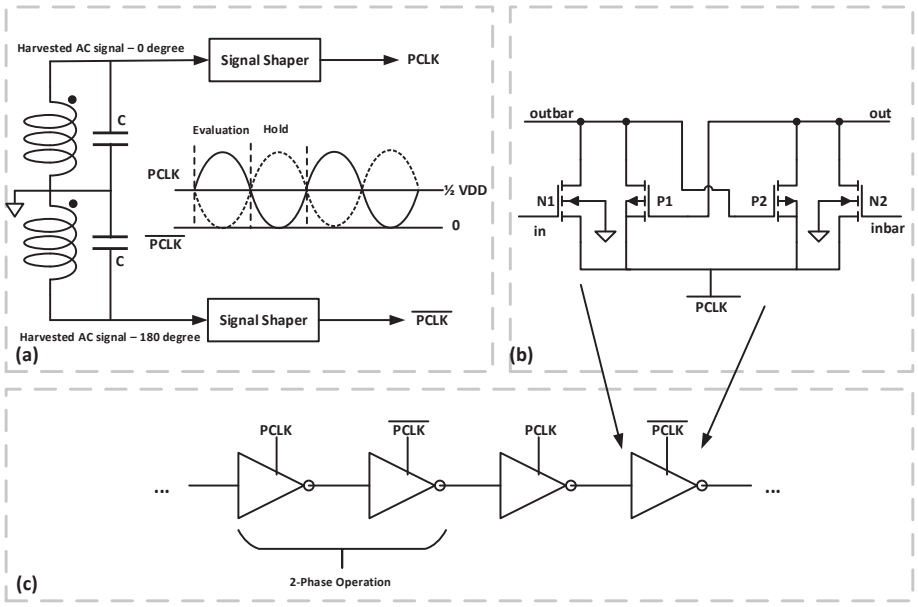

Fig. 2. **Proposed AC computing approach: (a) 2-phase AC power generation, (b) schematic of PAL based inverter cell, (c) consecutive PAL gates illustrating the two-phase operation.**

junctions. To mitigate these limitations, an LC phase shifter and a diode based peak detector have been proposed [8]. The phase shifter requires very high quality and large inductors (particularly at low frequencies) to minimize loss, which can be highly challenging to implement. These blocks also reduce the overall power savings achieved by AC computing. An alternative charge-recycling mechanism is proposed in this work, as described in the following section.

III. Proposed AC Computing Methodology

In the proposed method, pass-transistor adiabatic logic (PAL) [10] is used for AC computation with an additional block, referred to as signal shaper, as illustrated in Fig. 2. Similar to ECRL, a PAL gate consists of two NMOS transistors N1, N2, and a pair of cross-coupled charging/recovering PMOS transistors P1, P2. The primary advantage of PAL over ECRL is the ability to fully recycle charge since the NMOS transistors are connected to AC power supply (unlike ECRL where the NMOS transistors are connected to ground). Thus, a lower logic power consumption can be achieved. The operation of the PAL inverter shown in Fig. 2(b) can be summarized as follows. Assume that initially, input signal in is at logic high and AC supply $PCLK$ is rising. A conducting path is formed between $outbar$ and $PCLK$ since N1 is on. Thus, node $outbar$ follows the $PCLK$ whereas node out is floating. As the $PCLK$ reaches the threshold voltage, transistor P1 turns on and fully charges $outbar$. Finally, when the $PCLK$ is falling, the charge stored at $outbar$ node is fully recovered through both N1 and P1.

In addition, note that PAL is a two-phase logic where the AC supply of each consecutive gate is 180° out-of-phase, as depicted in Fig. 2(c). Thus, when one of the gates is at the "evaluation" phase, the preceding gate is at the "hold" phase, maintaining the input signals stable for the evaluating gate. This behavior is also a significant advantage over ECRL that requires four-phase operation. Thus, contrary to ECRL, in PAL based AC computing for wireless devices, a phase shifter is not needed within the receiver, thereby reducing the overhead power consumption. Note that the two inductors within the receiver are configured such that the two harvested AC signals have 180° phase difference, which is sufficient for PAL operation.

Despite these advantages, PAL cannot correctly operate with the harvested AC signal that has both positive and negative voltage components. To mitigate this limitation, a low complexity signal shaper is proposed, as shown in Fig. 3. The proposed signal shaper consists of a PMOS transistor with the bulk, gate, and one of the junctions shorted together. The input is the wirelessly harvested AC signal with -1 V to 1 V whereas the output is from 0 to approximately 1 V. The signal shaper lets the output approximately follow the shape of the input AC signal, but does not let the output fall below zero volt [see Fig. 3(b)]. Specifically, the transistor is sized to act as a voltage divider where the output signal is always positive. When the input voltage is higher than the output voltage (transistor is on), the voltage difference across the signal shaper is sufficiently low, thereby minimizing the power loss. Two signal shapers are required since there are two harvested AC signals with 180° phase difference. The simulated output waveform of a wirelessly powered inverter with and without signal shapers is illustrated in Fig. 4. As shown in this figure, the signal shaper eliminates the negative voltage components at the output that can be as high as -0.5 V when there is no signal shaper.

It is important to note that the proposed signal shaper can work bidirectionally and recover charge. Even when the transistor is off due to zero V_{GS}, the charge flows back to the AC power supply through relatively large gate-to-source and

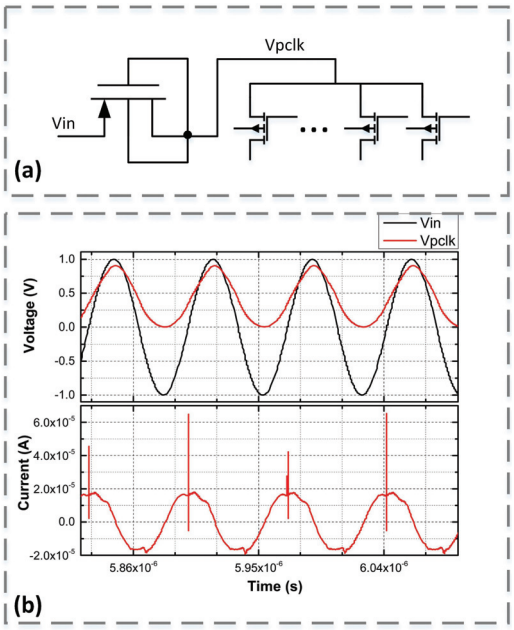

Fig. 3. **Signal shaper for wirelessly powered PAL based AC computing: (a) schematic, (b) simulated voltage and current waveforms.**

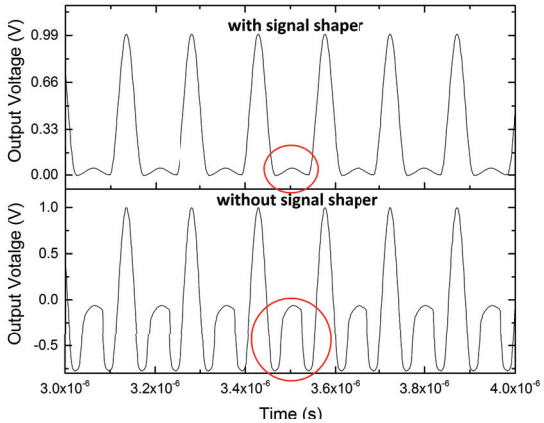

Fig. 4. **Simulated output waveform of a wirelessly powered inverter with and without signal shapers.**

gate-to-bulk capacitances since the junctions have AC signals (unlike static CMOS). Thus, full charge recovery is preserved [see negative current in Fig. 3(b)].

IV. Simulation Results

The proposed method is evaluated by designing a weakly coupled wireless link (see Section IV-A) and a 16-bit carry select adder (see Section IV-B), implemented in three different methods using 45 nm CMOS technology. In the first method, the adder is powered wirelessly by the method developed in [8]. In the second method, the approach proposed in this paper is used. Finally, in the third method, the harvested signal is rectified/regulated to obtain a DC voltage and conventional static CMOS based adder is used for computation. The power consumed by these three methods is compared. The transmission frequency (and therefore the frequency of operation for the computing unit) is 13.56 MHz, which is the standard frequency for silicon based item-level RF identification [15].

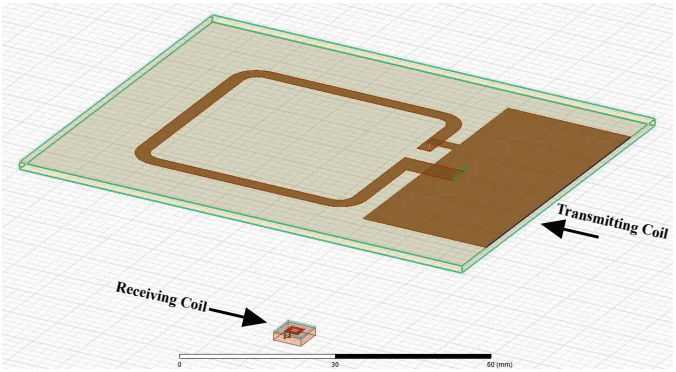

Fig. 5. **Transmitting and receiving coils used for the wireless link simulation using HFSS at 4 cm distance.**

A. Wireless Link

The wireless link consists of transmitting and receiving coils. The power transfer efficiency is determined by physical characteristics such as size of the coils, distance, and the electrical properties of the material between the coils. These key design parameters are determined by the specific application. For example, for wirelessly powered implantable devices, the receiving coil is required to have sufficiently small dimensions, making maximum achievable power efficiency a critical constraint. Thus, wirelessly powered biomedical devices are expected to significantly benefit from the proposed method. Considering this characteristic, implantable devices are investigated as a potential application. Transmitting and receiving coils are designed with a diameter of 50 mm and 3 mm, respectively. The power efficiency reaches -32 dB at 40 mm distance, assuming matching networks are available for transformation of load impedance to achieve optimum efficiency. The simulated setup is shown in Fig. 5. A commercial FEM (finite element method)-based full-wave electromagnetic field solver HFSS (high frequency structural simulator) is used to simulate and extract the equivalent RLC parameters of the wireless link. The Z parameters extracted from HFSS simulations along with Keysight Advanced Design System (ADS) simulations were used to determine the power efficiency of the wireless link.

B. Charge-Recycling 16-Bit Carry Select Adder

The wireless energy harvested by the link is used to power 16-bit carry select adder, designed in four blocks where each block consists of 4-bit carry ripple adders. The harvested AC signal swings from -1 V to +1 V. Similar to ECRL based approach proposed in [8], PAL is also inherently pipelined (due to consecutive gates having AC power with 180° phase difference). Thus, output signals should be synchronized by ensuring that the overall number of gates from inputs to each output is the same (which is 8 in this case). This condition is satisfied by inserting buffers along those paths with less number of gates. Since two consecutive gates complete one cycle, 4 AC cycles are required for the outputs to emerge. As an example, the simulated voltage waveform for the 16^{th} bit of the adder and the two out-of-phase AC power signals after the signal shaper are plotted in Fig. 6.

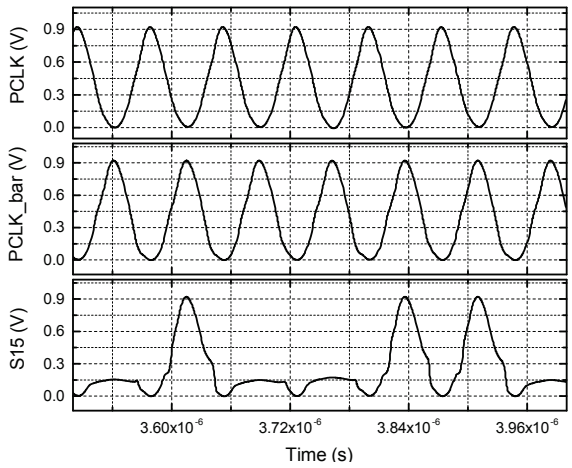

Fig. 6. **Simulated voltage waveforms for the 16^{th} bit of the adder and the two out-of-phase AC power signals after the signal shaper.**

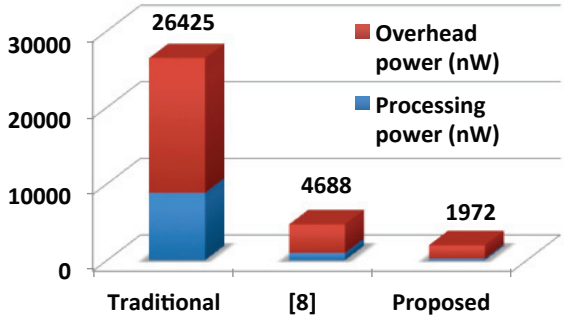

Fig. 7. **Comparison of the average power consumed by each method.**

The adder is also implemented with the ECRL based AC computing approach proposed in [8]. The same phase shifter structure is used to obtain four AC power signals with 90° phase difference. The overall number of gates from inputs to each output is also 8. The required number of cycles for the outputs to emerge, however, is 2 since four consecutive gates complete a cycle. Finally, the conventional approach is also implemented by designing a low complexity rectifier and regulator, similar to [8]. The adder in this case consists of D-type flip-flops at the primary inputs and outputs for synchronization. Note that minimum size transistors are used in each method since the operation frequency of 13.56 MHz is relatively low for the 45 nm technology.

C. Comparison of Power Consumption

The average power consumed by each method has been analyzed at the same low RFID frequency band of 13.56 MHz for 100 clock cycles with the same input data pattern. The results are shown in Fig. 7. According to this figure, the overall average power consumed by the conventional method (DC computing with rectifier and regulator) is approximately 26.4 μW. Alternatively, the power consumed by the proposed method is 1.97 μW, demonstrating 13.4× reduction. Compared to [8], approximately 60% reduction in power is achieved. Note that the power consists of two components: processing and overhead power. The processing power represents the logical power consumed by the 16-bit adder whereas the overhead power represents the power consumed by the supporting blocks. In conventional DC method, these supporting blocks include the rectifier and regulator, consuming 17.6 μW, approximately 67% of the overall power. In [8], the overhead power is due to two phase shifters (resistive loss) and a peak detector, consuming 3.7 μW. In the proposed method, the overhead power due to two signal shapers is 1.7 μW. These results demonstrate that in the proposed approach, both the processing and overhead power are significantly reduced.

V. Conclusion

AC computing brings a significant opportunity to enhance energy efficiency in wirelessly powered IoT devices. This improvement is achieved by eliminating rectifier and regulator circuitries of the DC computing and recycling charge during the computation. The proposed charge-recycling approach achieves more than an order of magnitude reduction in power as compared to traditional case and approximately 60% reduction as compared to previous work.

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