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Package-embedded spiral inductor characterization with application to switching buck converters

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ABSTRACT

The design and characterization process of a package-embedded spiral inductor is investigated in this paper via comprehensive electromagnetic simulations. A realistic, multi-layer flip-chip package is considered and modeled in a commercial, full wave electromagnetic simulator. At constant package area, parasitic resistance of a given inductance is minimized. The applicability of the proposed package-embedded spiral inductor to a DC-DC switching buck converter is demonstrated. The flexibility of the package is exploited to obtain a relatively high inductance, enabling a reduced switching frequency. Lower switching frequency minimizes the dynamic loss, thereby increasing the power efficiency. An interleaved multi-phase buck regulator with an *array of package-embedded spiral inductors* is developed. The extracted layout of the overall circuit is evaluated for performance and primary characteristics. The converter produces an output voltage of 0.9 V from 1.2 V input voltage while supplying a load current of 1 A. Power efficiency of approximately 89% is achieved with 3% output ripple voltage.

1. Introduction

Efficient voltage regulation and conversion are essential mechanisms in modern IC design process due to power management and heterogeneous computing [1]. Most of the existing low power design methods such as multi-voltage design, dynamic voltage frequency scaling, and low swing clocking require high efficiency and low cost regulators [2,3].

There are primarily three types of voltage converters: 1) linear converters such as low-dropout (LDO) regulators, 2) switched-capacitor based DC-DC converters, and 3) switching buck converters. LDO regulators are cost effective and have relatively fast transient response, but these regulators suffer from low power efficiency, less than 60% in most of the cases [4]. This limitation is exacerbated as the conversion ratio increases or output voltage decreases. Switched-capacitor converters exhibit enhanced power efficiency, but suffer from poor regulation capability since the switching frequency should be modified to regulate the output [5]. This process is slow since a voltage controlled oscillator is needed to vary the switching frequency, increasing the response time. Finally, switching buck converters can achieve high efficiency and large output current at the expense of a high quality inductor [6]. Since integrating a high quality inductor on-chip is highly costly, buck regulators typically consist of an external, discrete inductor. Existing work has also investigated the feasibility of increasing switching frequency to reduce the required inductance. In this case, however, the dynamic loss increases, thereby reducing the power efficiency [7]. For example, for inductance values in the low nanohenry range, the switching frequency should be increased to several hundreds of megahertz to obtain an acceptable current and voltage ripple at the output. The switching loss at these frequencies increases by two orders of magnitude as compared to high kilohertz or low megahertz operating frequencies (assuming constant transistor sizes) [8].

An intermediary solution (between a fully on-chip inductance and an off-chip discrete inductance) is investigated in this paper where the inductor is built within a flip-chip package in a spiral fashion whereas all of the other components are integrated on-chip. Note that this approach is different from discrete inductors integrated into a package (common practice in literature) since in the proposed case, the inductor is built using existing metal interconnects within the package layers and fabricated at the same time as the package.

In [9], existing wirebond inductance of a standard package (instead of spiral metals) has been utilized for a buck converter. Similarly, in [8], both the wirebond and lead frame inductance have been engineered to be used with an integrated buck converter. These approaches reduce the overall cost (since an existing package structure is leveraged for inductance) at the expense of higher inductance variability and reduced flexibility for the value of inductance. Thus, additional mechanisms such as extra calibration loops are required to

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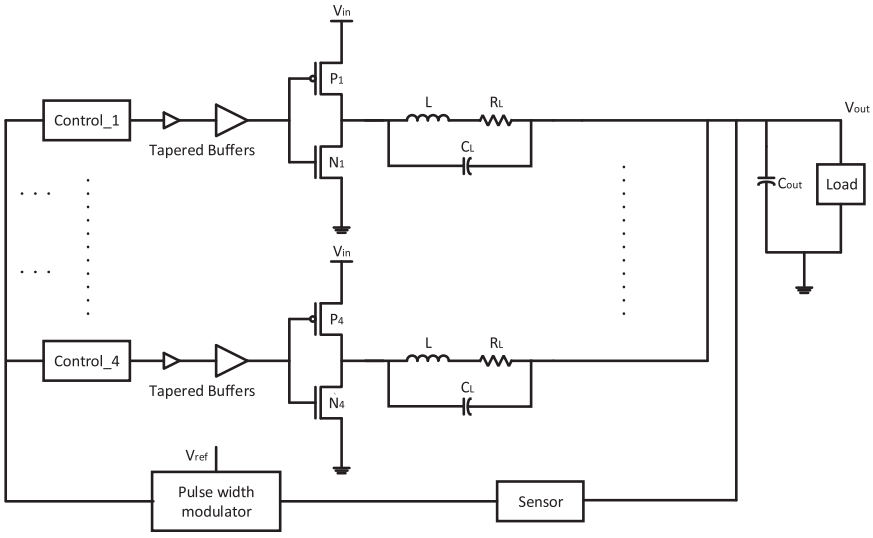

Fig. 1. An interleaved multi-phase switching buck regulator architecture.

alleviate these challenges [9]. In [10], package-embedded inductors have been discussed. The primary emphasis has been on building high-Q inductors within the routing layers of an organic package and experimental characterization. The applicability of this approach to switching buck converters has not been described.

As demonstrated in this paper, a higher inductance with a reasonable quality factor can be achieved by exploiting the greater flexibility of package area as compared to die area. This package-embedded spiral inductor is connected to the die via low resistance C4 bumps. Thus, the switching frequency of the buck regulator can be reduced to minimize dynamic power loss and enhance power efficiency. Specifically, in this work, the switching frequency is 50 MHz, which is significantly smaller than existing work with on-chip inductors (477 MHz [7], 200 MHz [11], 170 MHz [12], and 300 MHz [13]). Furthermore, package flexibility can be further utilized to develop an *array of package-embedded spiral inductors* for an interleaved multi-phase buck regulator architecture (see Fig. 1), as demonstrated in this paper. Thus, power efficiency and output ripple can be further enhanced.

The rest of the paper is organized as follows. A brief background on switching buck converters is provided in Section 2. The design and modeling process for package-embedded spiral inductors using a commercial field solver including the applicability of these inductors to an interleaved multi-phase buck regulator is described in Section 3. Extracted simulation results are presented in Section 4. Finally, the paper is concluded in Section 5.

2. Background

Switching buck converter is a step down DC-DC voltage regulator to supply power to various circuit modules such as a CPU core, memory core, or an accelerator module. A typical single-phase buck converter consists of 1) a switch network that generates an AC signal, 2) a second order low pass filter that passes the DC component of the AC signal to the output, and 3) feedback path that regulates the output voltage by changing the duty cycle of the AC signal [1].

2.1. Single-phase operation

Typical design specifications of a switching buck converter include input and output voltages, power efficiency, load current, voltage ripple, and transient response. The low pass filter, consisting of an inductor and capacitor, is a critical element within the buck converter since the output voltage characteristics depend upon the quality of this filter. The parasitic effective series resistance (ESR) of the inductor plays an important role in the resistive loss and the overall performance of the buck converter. A larger inductance (required to reduce ripple) typically produces a larger ESR, which in turn increases the resistive loss and causes a non-negligible voltage drop at the output, particularly if the load current is sufficiently high.

For a single phase buck converter, the required inductance can be determined by [1],

$$L = \frac{(V_{in} - V_{out})D}{2\Delta I_L f_s}, \tag{1}$$

where V_{in} and V_{out} are, respectively, input and output voltages, D is duty cycle, ΔI_L is the current ripple (half of the peak-to-peak current), and f_s is switching frequency. Assuming the output voltage ripple cannot exceed 5% of the output voltage, the minimum required capacitor C_{out} is determined by [1],

$$C_{out} \geq \frac{5(V_{in} - V_{out})D}{4V_{out}Lf_s^2} \tag{2}$$

Single-phase buck converters are sufficient for applications with low load current [14], but power dissipation and efficiency suffer at higher load currents. Thus, interleaved multi-phase buck converters have been considered for applications with high load current since peak ripple currents can be effectively reduced through this method [15,16].

2.2. Interleaved multi-phase operation

An interleaved multi-phase architecture has been commonly used to reduce the size of the individual inductors (and therefore ESR) without increasing the output ripple, as shown in Fig. 1 [17]. In this method, since the current through each stage is reduced, the constraint on inductor current is also relaxed, thereby permitting a smaller inductor per stage. The ripple due to each stage is partially canceled at the output. Thus, a smaller output capacitance can be sufficient.

In a multi-phase buck converter, the normalized ripple current $I_{Rip,norm}$ is determined by [14],

$$I_{Rip,norm} = P \times \frac{\left[D - \frac{\lfloor m \rfloor}{P}\right] \times \left[\frac{1+\lfloor m \rfloor}{P} - D\right]}{(1-D) \times D}, \tag{3}$$

where D is the duty cycle, P is the number of phases, and $m = D \times P$. This equation is important to determine the number of phases based on the required ripple current, as further discussed in Section 3.2.2.

In this case, multiple buck converters operate in a parallel fashion with a 90° phase difference. Each regulator has an individual inductor, but share the same output capacitor. Thus, the high ripple across each inductor is partially canceled at the output. Package-embedded spiral

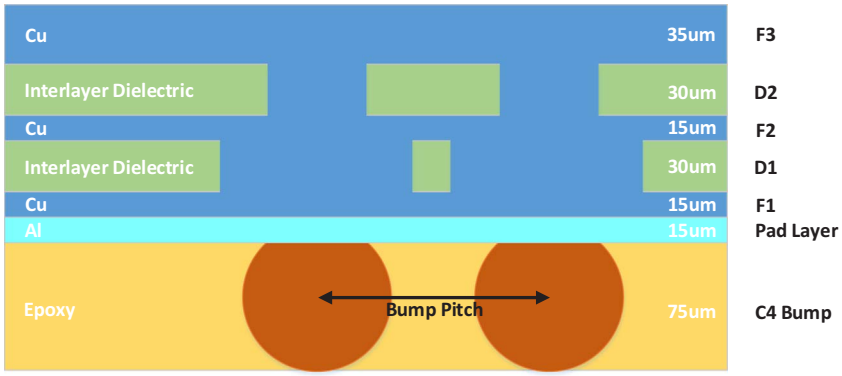

Fig. 2. Cross-section of the multi-layer flip-chip package where spiral inductors are built.

inductors provide a unique opportunity for interleaved architecture since an array of spiral inductors can be built using the package metal layers and fabricated as part of the package fabrication process.

3. Proposed method

The analysis of package embedded spiral inductor with detailed structure description and how this inductor works for switching buck converter are described, respectively, in Section 3.1 and Section 3.2.

3.1. Package-embedded spiral inductor characterization

A multi-layer flip-chip package is assumed. Cross-section of the package illustrating each layer is shown in Fig. 2 [10,18].

Three copper metal layers exist with two different thicknesses. The top metal (F3) is 35 μm thick whereas the bottom two metal layers (F1 and F2) are 15 μm thick. There is an aluminum pad layer with 15 μm thickness. The dielectric layers (D1 and D2) are 30 μm thick and consist of flame retardant (FR4) epoxy. The inductor is built on layer F3 and is connected to the C4 bumps located at the bottommost layer filled with epoxy with 75 μm thickness [19]. The C4 bumps connect the inductor terminals to the on-chip components (tapered buffers, power transistors and capacitance). This package structure is modeled using a commercial finite element method (FEM) based full wave electromagnetic field solver ANSYS HFSS (high frequency structural simulator). The DC and low frequency characteristics are analyzed using ANSYS Q3D Extractor.

A conventional spiral inductor is illustrated in Fig. 3(a) where the important physical characteristics are highlighted such as the number of turns T, internal diameter D_{in}, external diameter D_{out}, width w, and spacing s. The following relationship holds among these parameters, assuming that the number of turns T is an integer,

$$D_{in} = D_{out} - (2T + 1) \times w - (2T - 1) \times s. \tag{4}$$

An electrical equivalent circuit is shown in Fig. 3(b) assuming a one-terminal, two-port extraction [20]. The frequency dependent $L(f)$, $C_L(f)$, and $R_L(f)$ refer, respectively, to the extracted inductance, capacitance, and effective series resistance (ESR).

These frequency dependent components are extracted by analyzing the Y parameters from HFSS [21]. Specifically, Y_{11} is

$$Y_{11}(f) = \frac{1}{R_L(f) + j\omega L(f)} + j\omega C_L(f). \tag{5}$$

Assuming the series capacitance $C_L(f)$ varies only marginally with frequency [20] (this component can be extracted from Q3D Extractor at a low frequency), the extraction of $R_L(f)$ and $L(f)$ is performed using the following procedure:

- Subtract the admittance $C_L(f)$ from Y_{11} and convert the remaining term into impedance,

$$Z_{11_{RL}}(f) = R_L(f) + j\omega L(f). \tag{6}$$

- Plot the real and imaginary parts of $Z_{11_{RL}}(f)$ at the frequency of interest to extract $R_L(f)$ and $L(f)$ from HFSS.

An array of four inductors modeled in HFSS considering the package structure described above is shown in Fig. 4. In this example, each inductor occupies an area of 1 mm × 1 mm. To determine the physical parameters of the package-embedded spiral inductor (T, D_{in}, D_{out}, w, s), the procedure described in [22] is used.

Two methods are considered to determine the physical characteristics of the inductor and maximize the quality factor:

- D_{in} based model: D_{in} is kept constant at 50 μm. The width is progressively increased (with a step size of 1 or 4 μm, depending on required accuracy) until D_{out} reaches 1 mm, the available dimension for the package area.
- D_{out} based model: D_{out} is maintained constant at 1 mm. The width is progressively increased (with a step size of 1 or 4 μm) until D_{in} reaches the minimum allowable value. Note that according to (4), as

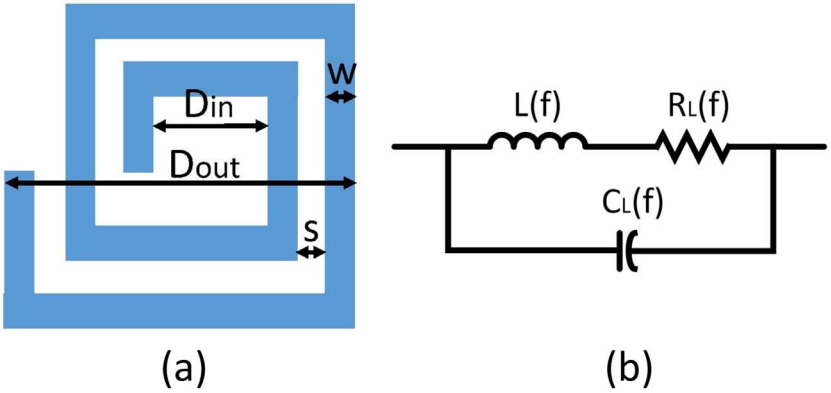

Fig. 3. Typical spiral inductor: (a) physical characteristics, (b) equivalent electrical circuit.

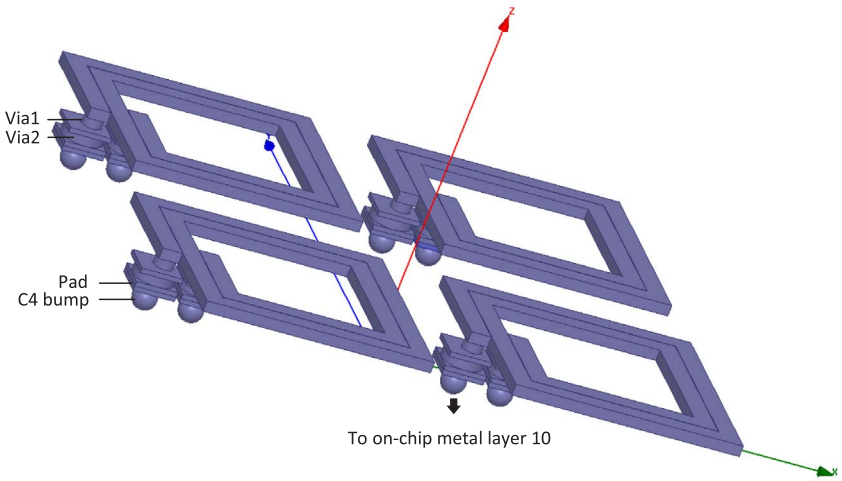

Fig. 4. Array of package-embedded spiral inductors modeled in full wave electromagnetic simulator HFSS.

width is increased, D_{in} is reduced.

For both analysis modes, spacing is constant at 2 μm to maintain the tight coupling of the magnetic field. Note that these analyses are achieved at different number of turns, producing a large design space, as illustrated in Figs. 5 and 6. Also note that the frequency is constant at 50 MHz.

From this design space, the inductors that satisfy the required inductance can be extracted (for example, see the dashed horizontal line at 5 nH). Here, every design point that intersects with the horizontal line satisfies the required inductance. Thus, the point that achieves the highest quality factor (minimum ESR) can be chosen. It is important to note that for inductors in the range of several nano henry and above, the minimum ESR occurs within the D_{out} based model since the D_{in} based model requires a large number of turns to reach the required inductance, which increases the ESR. Thus, for minimum ESR, a good design practice is to choose a small number of turns at a sufficiently high width that can achieve the required inductance.

3.2. Application to interleaved switching buck converter

3.2.1. Implementation of a single-phase converter

Package-embedded spiral inductors designed and characterized in the previous section are used for a switching DC-DC converter, designed in 45 nm technology. The converter converts an input voltage of 1.2 V to an output voltage of 0.9 V while supplying 1 A of load current. Referring to Fig. 1, P_1 and N_1 are two large power transistors driven by a 5-stage tapered buffer, followed by a low pass filter. The switching frequency is 50 MHz (lower than existing buck regulators with on-chip inductor [7,11–13]) since the flexibility of the package is utilized. Duty

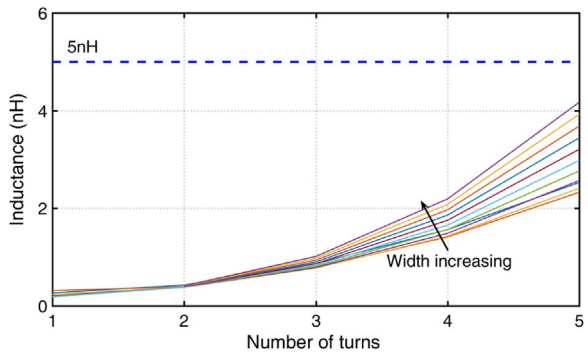

Fig. 5. Design space of the package-embedded spiral inductor as a function of number of turns and width at constant spacing, thickness, and frequency (D_{in} based model).

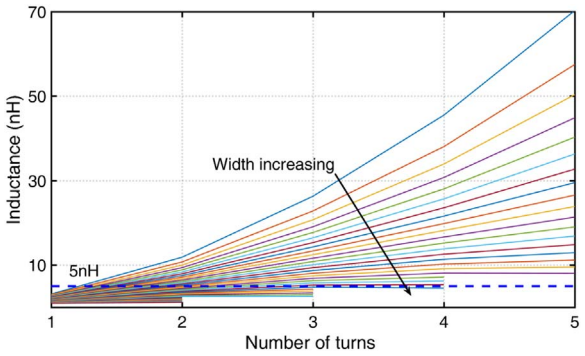

Fig. 6. Design space of the package-embedded spiral inductor as a function of number of turns and width at constant spacing, thickness, and frequency (D_{out} based model).

cycle is 0.79 that is slightly larger than the conversion ratio (0.75) to compensate for the voltage drop across the ESR of the inductor [23]. Substituting these values to Eqs. (1) and (2) L is determined as 7.9 nH, the minimum required capacitor C_{out} is calculated as 16.7 nF, taking approximately 2.5 mm^2 on-chip area in 45 nm technology. If 7.9 nH of inductance is characterized and extracted by HFSS (within an area of 1 mm^2), the output voltage of the converter exhibits a significant drop due to relatively large ESR. Thus, for these specifications, a multi-phase buck converter is required, as described in the following section. Note that a multi-phase architecture is particularly applicable to the proposed package-embedded inductors since multiple inductors need to be implemented.

3.2.2. Four-phase converter operation and optimization

An interleaved four-phase buck converter is developed to reduce the inductor and therefore ESR without increasing the output ripple. The optimal number of phases can be calculated through Eq. (3) mentioned in the previous section. Since the duty cycle is 0.75, ripple can be canceled completely with four phases with 90° phase difference.

As mentioned before, output capacitance can be significantly reduced with interleaving technology. The only output capacitor is a 2.5 nF capacitor implemented as MOS-C and integrated on-chip with 0.37 mm^2 area occupation. Note however that the MOS-C should be designed carefully to avoid a high ESR that would cause high output voltage ripple.

3.2.3. Physical layout of the proposed 4-Phase buck converter

The layout is implemented in a 45 nm technology. The package-embedded inductors and the C4 bumps are implemented and characterized using HFSS. The C4 bumps connect the inductor terminals to

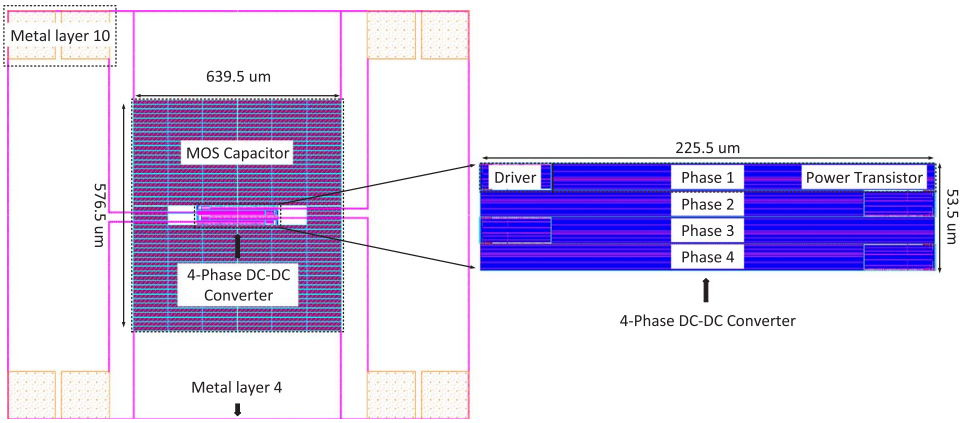

Fig. 7. The on-chip layout of the 4-phase converter, illustrating the power transistors, drivers, MOS capacitors, and metal layer 10 for connection to the package-embedded inductors.

on-chip metal layer 10, as shown in Fig. 7. The filter capacitance is implemented as MOS-C and located above and under the tapered buffers and power transistors. The guidelines from [24] were followed to obtain a proper layout with sufficiently small parasitic impedances.

The overall area of the converter and on-chip MOS capacitor is 639.5 μm × 576.5 μm. After considering the area of top vias and overhead connections, the area occupied by the overall circuitry is 1284 μm × 1134 μm (see Fig. 7).

4. Simulation results

The four-phase dc-dc converter is designed to operate at a switching frequency of 50 MHz. The power efficiency of the converter as a function of inductor is shown in Fig. 8. The highest efficiency of 88.32% is achieved when each inductor in the interleaved topology is approximately 5 nH.

Thus, *an array of package-embedded spiral inductors* is characterized in HFSS where each of the four inductors is 5 nH and occupies 1 mm^2 area (see Fig. 4). The overall area consumed in the package by spiral inductors is 4.076 mm^2. To determine the physical characteristics of the inductors, the procedure described in the previous section is followed. After the entire design space is obtained, as shown in Figs. 5 and 6, the number of turns and widths that produce the required inductance are analyzed for quality factor. The highest quality factor of 11.8 is achieved (at the switching frequency of 50 MHz) with a 2-turn spiral inductor and 64 μm width, as depicted in Fig. 9. Main related spiral inductor dimensions for this highest quality factor inductor are listed in Table 1. The ESR and series capacitance are extracted, respectively, as 132 mΩ and 50.7 fF. The four-phase interleaved buck converter (after *RC* impedance extraction of the layout) is simulated in SPICE with the electrical model of the package-embedded spiral inductors (extracted from HFSS at 50 MHz). The current ripple on each phase is 399 mA (see Fig. 10). The maximum and minimum output current in steady state are, respectively, 1.095 A and 0.919 A. Thus, the output current ripple

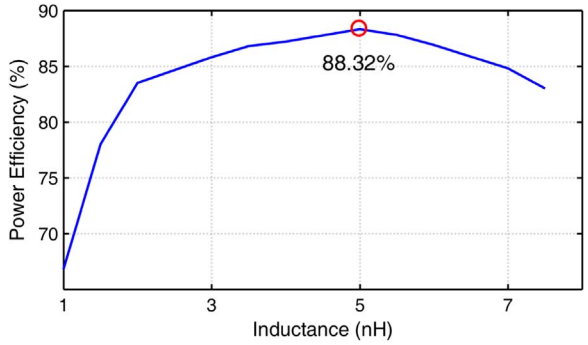

Fig. 8. Power efficiency of an interleaved four-phase buck converter as a function of inductance.

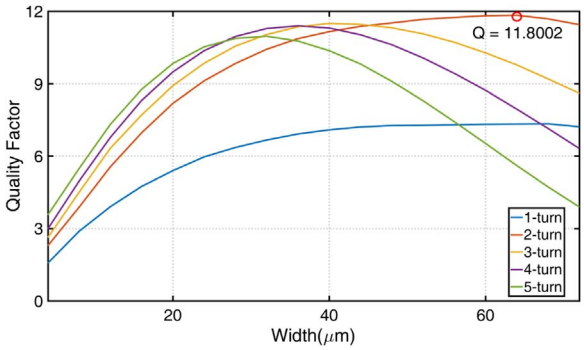

Fig. 9. The dependence of inductor quality factor on the number of turns and width at a switching frequency of 50 MHz.

Table 1
Physical characteristics of the package-embedded inductor.

Parameter	Value
Turn	2
din	608 μm
dout	1 mm
Width (w)	64 μm
Space (s)	2 μm
Thickness (t)	35 μm
Bump thickness	75 μm
Bump diameter	80 μm
Bump pitch	150 μm

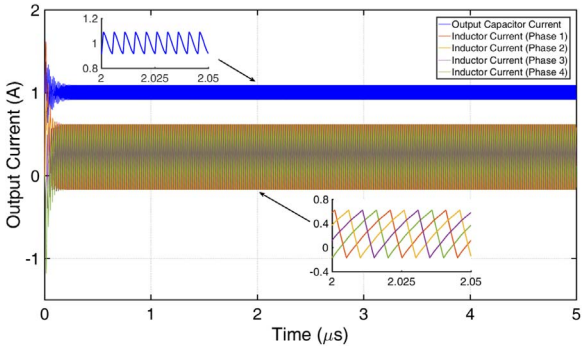

Fig. 10. Cancellation of inductor ripple current with D = 75%.

is 95 mA, 9.5% of the output current, as depicted in Fig. 11(a). Note that the output current ripple is much smaller than the ripple on each phase due to the interleaved multi-phase topology.

The transient response time when current abruptly changes from 0

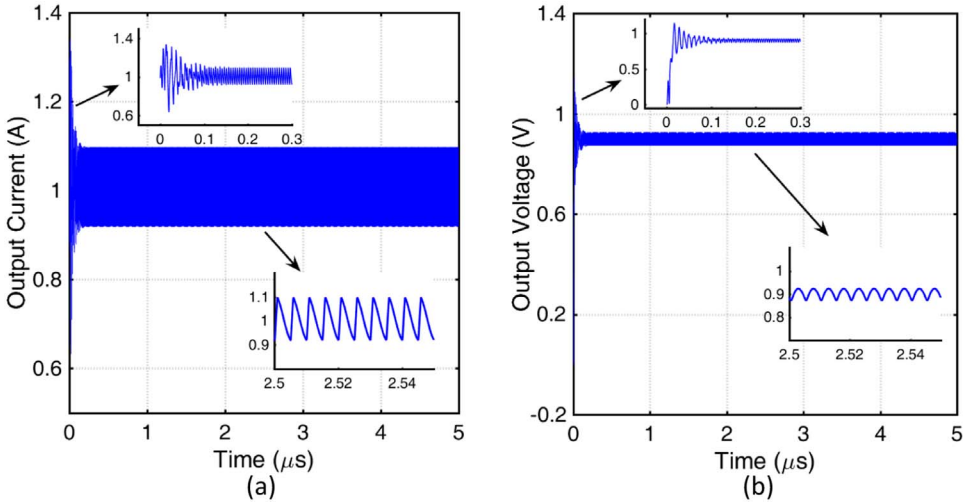

Fig. 11. Simulation results of the interleaved, four-phase buck converter with package-embedded spiral inductors: (a) output current, (b) output voltage.

Table 2
Primary performance characteristics of the switching buck converter with package-embedded spiral inductors.

Technology	45 nm CMOS
Single inductor area	1 mm × 1 mm
Number of phase	4
Inductor	5 nH
Filter capacitor	2.5 nF
V_{in}	1.2 V
V_{out}	0.9 V
$V_{out\,ripple}$	26.8 mV
I_{out}	1 A
I_{ripple}	95 mA
Switching frequency	50 MHz
Transient response time	0.1 μs
Power efficiency	88.32%

to 1 A is 0.1 μs, as shown in Fig. 11(a). The corresponding output voltage is plotted in Fig. 11(b). The overshoot when the load current abruptly falls to zero is 0.3 V. The output voltage ripple in the steady state is only 26.8 mV. Note that the results shown in this figure represent an open-loop response since no feedback exists between the output node and power transistors. The switching buck converter performance is summarized in Table 2.

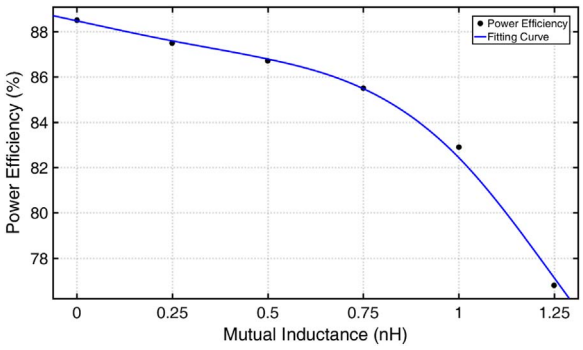

Fig. 13. The effect of mutual inductance among the package-embedded spiral inductors on power efficiency.

One of the issues related with interleaved topology is the mutual coupling among the inductors. This effect is investigated, assuming that the mutual inductance is less than 30% of the self-inductance [1,27,28]. Specifically, the mutual inductance is varied from 0.25 nH (5% of the self-inductance in each phase) to 1.25 nH (25% of the self-inductance in each phase) with a step size of 0.25 nH. These analyses demonstrate the effect of mutual coupling among spiral inductors on the ripple (see Fig. 12) and power efficiency (see Fig. 13). According to these figures,

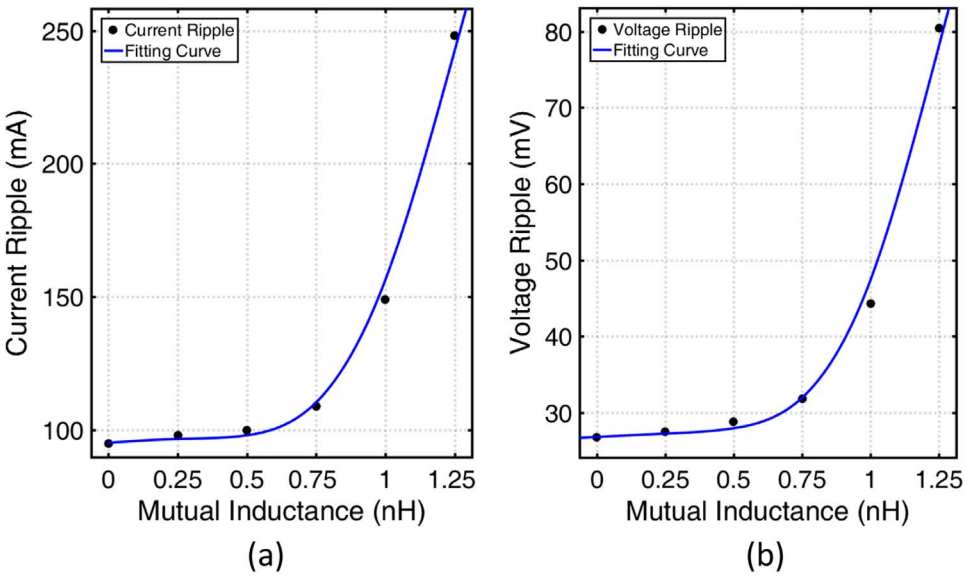

Fig. 12. The effect of mutual inductance among the package-embedded spiral inductors on ripple: (a) maximum output current ripple, (b) maximum of output voltage ripple.

Table 3
Comparison of the proposed buck converter with existing approaches.

	[12] Measured	[13]	[25]	[26]	[8]	[9]	This work Simulated
Technology/nm	130	130	130	150	130	130	45
Integration level	on-chip	on-chip	on-chip	on-chip magnetic	in-package bonding wire lead frame	in-package bonding wire	in-package spiral
Switching frequency /MHz	170	300	250	150	50	100	50
Output capacitor/nF	3.1	5	7	70	3.4	9.8	2.5
Inductor/nH	2	2	4.5	N/A	19.9	7	5
Input voltage/V	1.2	1.2	1.2	1.66	3.3 V/2.5 V	1.2	1.2
Output voltage/V	0.9	0.88	0.9	0.83	2.0 V/1.8 V	0.9	0.9
Load current/A	0.35	0.35	0.172	0.39	0.3	0.37	1
Peak efficiency/%	77.9	77	80	82	76.8	84.7	88.3
Chip area/mm^2	27	1.59	3.92	N/A	10.08	2.25	1.46

mutual inductance has negligible effect until approximately 0.6 nH (12% of the self-inductance). Beyond this value, both the ripple and power efficiency degrade. Since the spiral inductors are embedded within the package, there is significantly more flexibility to increase the spacing among the inductors (as compared to on-chip implementations) to ensure that the mutual coupling is within the tolerable range.

The simulation results are compared with several prior work, as listed in Table 3. At comparable conversion ratios, this work achieves the highest power efficiency while supplying a load current of 1 A. The switching frequency is lowest due to the package-embedded spiral inductors. These results demonstrate the applicability and advantages of built-in, package-embedded spiral inductors for DC-DC switching buck converters.

5. Conclusion

Design and characterization of built-in package-embedded spiral inductors have been investigated in this paper through comprehensive electromagnetic field simulations using HFSS. A detailed and realistic flip-chip package has been considered. An array of spiral inductors have been characterized with application to an interleaved switching buck converter. The greater flexibility of the package area has been utilized to lower the switching frequency, thereby increasing power efficiency. The proposed buck converter outperforms existing buck converters, demonstrating the benefits of package-embedded spiral inductors for switching regulators.

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