6 Power and Signal Integrity Challenges in 3D Systems-on-Chip

Emre Salman

CONTENTS

ABSTRACT

A significant physical design challenge in both high-performance 3D integrated circuits and low-power 3D systems-on-chip is to guarantee system-wide power and signal integrity. This chapter provides an overview of these challenges with emphasis on through-silicon via (TSV)-based 3D ICs. Different TSV types and their implications to power/signal integrity are first discussed. In the next section, power distribution methodology for a 9-plane processor-memory stack is described. Different decoupling capacitor topologies are also investigated for power-gated 3D ICs. The following section focuses on TSV-to-transistor noise coupling as an important signal integrity issue. A compact model is also proposed to achieve efficient noise coupling analysis in 3D ICs. Finally,

a case study is described to analyze signal integrity in a 3D integrated SoC with application to bioelectronics.

6.1 INTRODUCTION

Three-dimensional (3D) integration is a promising technology that maintains the benefits of miniaturization by utilizing the vertical dimension rather than decreasing the size of the devices in two dimensions [1–7]. Utilizing the vertical dimension not only increases the integration density (thereby reducing cost), but also reduces the length and number of global interconnects. This reduction enhances system performance (due to reduced interconnect delay) while lowering the power consumption (due to reduced switching capacitance). These advantages have attracted significant attention in the past decade to develop high-performance computing systems such as many-core processors with embedded memory, as illustrated in Figure 6.1a [8–11]. 3D technologies alleviate the existing gap between logic blocks and memory units in high-performance microprocessors by utilizing vertically embedded dynamic random access memory (DRAM), thereby significantly increasing the memory bandwidth and reducing memory access time.

In addition to facilitating high-performance computing systems, 3D technologies provide a unique opportunity for heterogeneous integration of diverse functions onto a monolithic chip, as depicted in Figure 6.1b. Heterogeneous integration expands the application domain of 3D-integrated circuits from high-performance computing to relatively lower power systems-on-chips (SoCs) consisting of, for example, sensors, analog interface circuit, memory, digital processing blocks, and RF wireless transmission circuitry. The ability to merge disparate circuits and technologies is essential for multifunctional systems since each plane can be optimized according to the requirements of that particular function. This advantage also supports the concept of *More-than-Moore* that targets the scaling of a system by incorporating nondigital portions into the same monolithic IC [12,13]. 3D integration of diverse functions is expected to enable exciting opportunities in a variety of fields including energy-efficient mobile computing, health care, and environmental control. For example, The Semiconductors Electronics Division of the National Institute of Standards and Technology

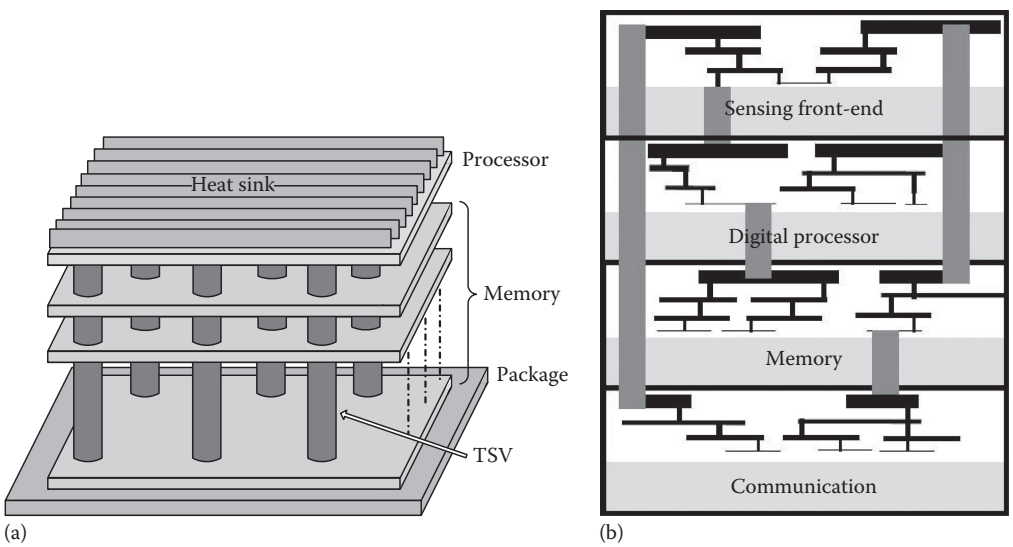

FIGURE 6.1 Two primary applications of TSV-based 3D integration technology: (a) many-core processors with embedded memory for high-performance computing and (b) heterogeneous 3D SoC with application to low-power mobile computing, health care, and environmental control.

(NIST) identifies 3D technology as one of the fundamental enabling technologies for "extremely scaled intelligent bio-electronic micro-systems for *in vivo* operations" [14].

A significant circuit- and physical-level challenge in both high-performance 3D computing systems and relatively low-power 3D SoCs is to ensure *system-wide power and signal integrity*, as explored in this chapter. Power integrity refers to the quality of the power supply voltage delivered to each transistor within a 3D stack, whereas signal integrity refers to the quality of both analog and high-speed digital data signals that are subject to different types of noise. These issues are investigated in the following sections with particular emphasis on wafer-level 3D integration technologies where multiple wafers are thinned, aligned, and vertically bonded. Communication among the dies is achieved by high-density Through-Silicon-Vias (TSVs). Global interconnect length is therefore reduced, lowering the overall power dissipation and latency. TSVs achieve significantly higher interconnection density among the planes of a 3D stack as compared to other vertical interconnects such as through hole vias in a system-in-package (SiP) [3].

The rest of the chapter is organized as follows. The primary characteristics of the three TSV fabrication technologies are summarized in Section 6.2. The issues of power integrity and signal integrity in TSV-based 3D systems are discussed in Sections 6.3 and 6.4, respectively. The chapter is concluded in Section 6.5.

6.2 TSV TECHNOLOGIES AND IMPLICATIONS TO POWER/SIGNAL INTEGRITY

As illustrated in Figure 6.2, existing efforts in 3D-ICs can be broadly classified under three primary categories: (1) transistor-level 3D integration, (2) system-in-package (SiP) and system-on-package (SoP), and (3) wafer-level TSV-based 3D integration. In transistor-level 3D integration [15], active devices within a logic gate are fabricated on different layers, but only a single substrate exists. The upper layer devices are formed on a recrystallized silicon obtained by laser heating or rapid thermal annealing [16]. Polysilicon and single crystal silicon films are also used to host upper layer transistors. Despite the highest density of vertical interconnects, transistor-level 3D integration suffers significantly from thermal challenges and high-defect density [17]. The upper layer silicon should be formed with sufficiently low temperatures to not damage the metal interconnects and devices at the bottom layers. Due to this limitation, the existing research in transistor-level 3D integration primarily focuses on material development and novel fabrication methods.

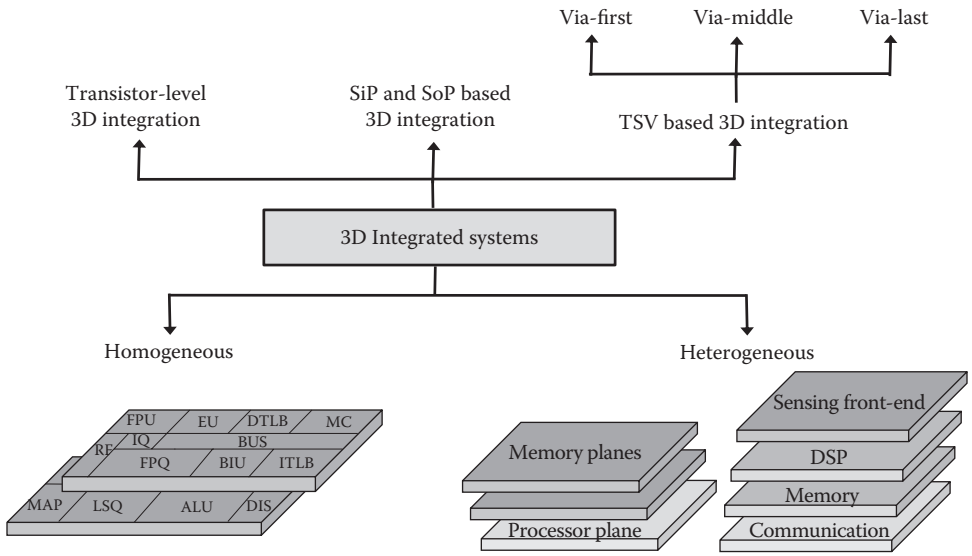

FIGURE 6.2 Broad classification of 3D circuits.

SiP- and SoP-based 3D integration [18–20] are relatively more mature, and commonly encountered in commercial electronic devices where multiple dies are packaged by utilizing (1) wire bonding, (2) low-density vertical interconnects, and (3) area–array-based C4 (controlled collapse chip connection) bumps. Comprising a primary practical concern, the length of these interconnects are typically in the range of several millimeters, significantly degrading the reliability and packaging efficiency in addition to preventing dense integration and causing high power consumption.

In wafer-level 3D integration [21–23], as depicted in Figure 6.1, entire wafers are bonded to produce a 3D stack where TSVs are utilized for interplane communication. This method not only achieves higher interconnect density, but also lower cost per connection due to greater alignment accuracy and enhanced surface planarization [24]. Furthermore, greater flexibility is provided to implement *in-stack* passive devices that are highly important in analog and RF functions. Thus, wafer-level 3D integration is considered to be one of the most promising approaches to realize dense and heterogeneous ICs in the nanoscale era [25–27].

Despite the ongoing research to further optimize 3D fabrication steps, no fundamental limitation exists. For example, alignment accuracy of one micrometer has already been demonstrated [26]. Multiple bonding techniques have also been developed such as adhesive [28,29], oxide [30], and metal bonding [31]. The wafer thinning capability varies from hundreds of nanometers to several hundred micrometers, depending upon whether bulk silicon or silicon-on-insulator is utilized [32,33]. Finally, several distinct TSV fabrication methods exist depending upon when the TSVs are formed [34]. These methods are (1) via-first [35], (2) via-middle [36,37], and (3) via-last TSVs [38]. Note that each TSV type exhibits significantly different electrical characteristics, and therefore require distinct design guidelines, as described in the following subsections.

6.2.1 Via-First TSV Technology

In a via-first method, TSVs are fabricated before the transistors are patterned in silicon, that is, prior to front-end-of-line (FEOL) [35,39–41]. Thus, TSVs fabricated with the via-first technique do not pass through the metallization layers, as depicted in Figure 6.3a. The TSV of a plane is connected between the first metal layer of the current plane and the top most metal layer of the previous plane. Polysilicon is typically used as the filling material due to its ability to withstand high temperatures [35,39–41]. Via-first TSVs are less sensitive to contamination since both the filling and substrate materials are the same [42]. The physical dimensions of via-first TSVs are smaller than via-last TSVs [43]. Via-first TSVs, however, are highly resistive and have a lower filling throughput due to the use of polysilicon as the filling material [42,44].

6.2.2 Via-Middle TSV Technology

In a via-middle process, TSVs are fabricated after FEOL, but before the metallization layers are patterned, that is, prior to back-end-of-line (BEOL) [36–38,42,45]. Similar to via-first TSVs, via-middle TSVs connect the first metal layer of a plane with the last metal layer of the previous plane, as illustrated in Figure 6.3b. Since the high-temperature FEOL process precedes TSV fabrication steps, via-middle process permits the use of tungsten (or possibly copper) as the filling material, which is significantly less resistive as compared to doped polysilicon. Tungsten can be used as the filling material due to low thermal expansion coefficient (4.6 ppm/K) as compared to copper (17 ppm/K) [37]. A material with low sensitivity to temperature is required since the TSV fabrication step is followed by a moderately high temperature BEOL process. Note however that copper-filled via-middle TSVs have also been demonstrated [46].

Via-middle TSVs require a relatively large (12:1 or higher) aspect ratio [36–38,45]. Thus, the width of via-middle TSVs is comparable to the width of via-first TSVs, whereas the height is comparable to via-last TSVs. This characteristic produces a relatively high inductive behavior. Also note that the fabrication process of via-middle TSVs is relatively more challenging. For example,

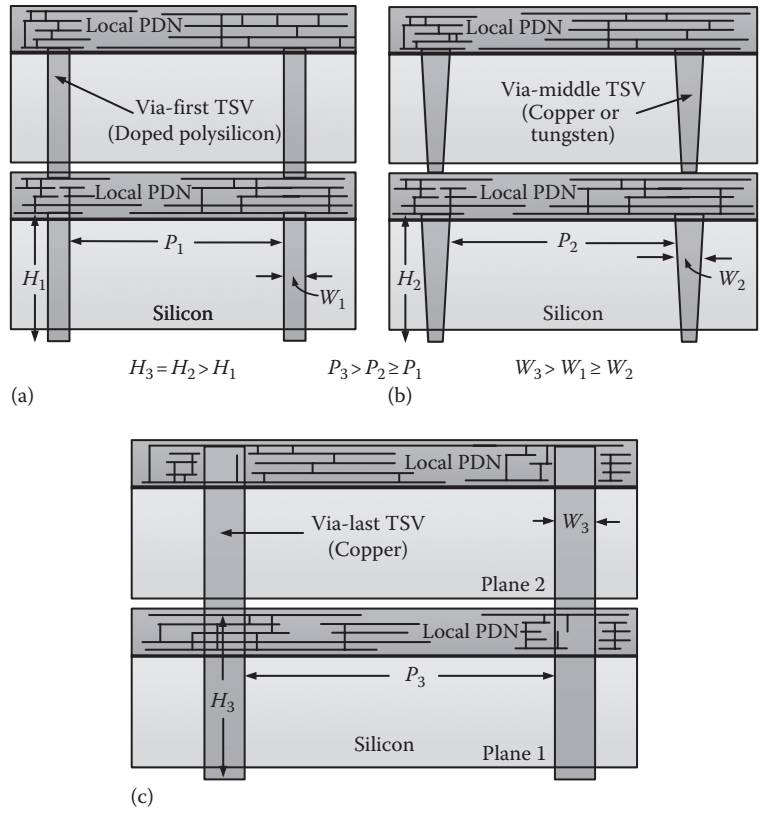

FIGURE 6.3 Illustration of the three primary TSV technologies: (a) via-first, (b) via-middle, and (c) via-last.

a conformal barrier process is required for the tungsten to adhere to the dielectric in the cavity. A 20-nm titanium nitride (TiN) layer is typically deposited using metal organic chemical vapor deposition (MOCVD) [36]. TiN is a hard, dense, refractory material with sufficiently low electrical resistivity (22 μΩ cm) [47].

Another challenge is the high level of stress during the deposition of the oxide layer, which is exacerbated when a conformal layer is required. This challenge is partially negated with the use of a tapered TSV structure that progressively shrinks in size [36,37]. This structure is illustrated in Figure 6.3b. Other challenges include sensitivity to contamination and the requirement to maintain the temperature within 500°C [42]. Novel deposition techniques such as atomic layer deposition (ALD) and time-modulated deposition alleviate some of these issues [36,48].

From the design perspective, via-middle technology is an interesting compromise between a highly resistive via-first and a low resistive, but highly inductive via-last TSVs. Furthermore, similar to via-first TSVs, via-middle TSVs do not cause metal routing blockages. The Semiconductor Manufacturing Technology (SEMATECH) consortium has chosen via-middle TSVs as a primary focus area [49].

6.2.3 Via-Last TSV Technology

In the via-last approach, TSV formation occurs after the metallization layers are fabricated, that is, after BEOL [39,42,43]. Thus, as opposed to via-first and via-middle TSVs, via-last TSVs pass through the metal layers, causing metal routing blockages, as depicted in Figure 6.3c [43,50]. A lower resistivity filling material such as copper is used since high temperature FEOL and BEOL processes are performed before the via formation [39,42]. The use of copper as a filling material

makes the process sensitive to both temperature (should be maintained less than 230°C) and contamination [42]. Despite exhibiting relatively low resistance, the inductive characteristics of via-last TSVs are relatively more significant than via-first TSVs due to greater dimensions [43]. The physical connection between the TSV and metal layers is typically achieved at the top most metal layer. Note that process technologies to manufacture TSVs are currently under investigation based on recent research results on wafer thinning, alignment accuracy, mechanical stress, and bonding methods. Thus, TSV geometries for a certain TSV type may vary depending upon the foundry.

6.3 SYSTEM-WIDE 3D POWER INTEGRITY

A significant circuit- and physical-level challenge in a TSV-based 3D-IC is to design a robust power distribution network that achieves reliable power delivery to each die. Maintaining the power network impedance smaller than a target impedance (i.e. satisfying the power supply noise) is a difficult task due to reduced operating voltages, increased current magnitudes, and the existence of multiple dies and TSVs. A conservatively large number of power/ground TSVs can significantly increase the area overhead in addition to producing highly inductive characteristics due to a smaller damping factor.

A case study is described in Section 6.3.1 where the power integrity characteristics of a nine-plane processor-DRAM system are investigated. A design space is developed to satisfy power supply noise while minimizing the physical area consumed by the TSVs and decoupling capacitors [51].

3D-ICs are expected to be heavily power-gated due to the importance of subthreshold leakage current in nanoscale bulk CMOS technologies. Furthermore, with heterogeneous integration, the switching activity factor of different blocks/planes is expected to significantly vary, emphasizing the need for power gating. Power gating, however, significantly affects the system-wide power integrity of a 3D-IC, particularly in the presence of decoupling capacitors [52,53]. Various decoupling capacitor topologies are discussed in Section 6.3.2 to enhance power integrity in the power-gated 3D-ICs. Advantages of a reconfigurable decoupling capacitor topology are emphasized [54].

6.3.1 Case Study: Power Distribution in a Nine-Plane 3D Processor-DRAM Stack

6.3.1.1 Architecture

A 3D system in a 32-nm CMOS technology consisting of eight memory planes and one plane for the processor is considered. Each plane contains nine metal layers where the metal thickness and aspect ratio are determined according to 32-nm technology parameters [55]. The power supply voltage is equal to 1 V. Each plane occupies an area of 120 mm^2, excluding the TSVs and the intentional decoupling capacitance. The system has 1 GB of DRAM spread uniformly across eight memory planes. Each memory plane has 1 gigabit (GB) DRAM divided into 32 modules of equal size, where each module has 32 MB memory. Similarly, the processor plane is also divided into 32 modules. Each of these modules consume an area of $1500 \times 2500\ \mu m^2$. This topology is depicted in Figure 6.4. For via-first and via-middle technologies, the TSVs are placed beneath the active circuit, as illustrated in Figure 6.4a whereas in via-last technology, the power and ground TSVs are distributed on both sides of each module, as depicted in Figure 6.4b.

6.3.1.2 Power Distribution Network Model

An equivalent electrical model corresponding to the power distribution network of one of the 32 modules is illustrated in Figure 6.5. This model consists of the TSVs (R_{TSV}, C_{TSV}, and L_{TSV}), substrate (R_{Si} and C_{Si}), power distribution network within a plane ($R_{Network}$, $R_{Vertical}$, and R_{M1}), switching load circuit, and decoupling capacitance C_{decap}. Note that in addition to these on-chip impedances, the parasitic package resistance and inductance are, respectively, 3 mΩ and 100 pH at both the power and ground supplies, assuming an organic flip-chip package [56]. The primary characteristics of the three TSV technologies are listed in Table 6.1.

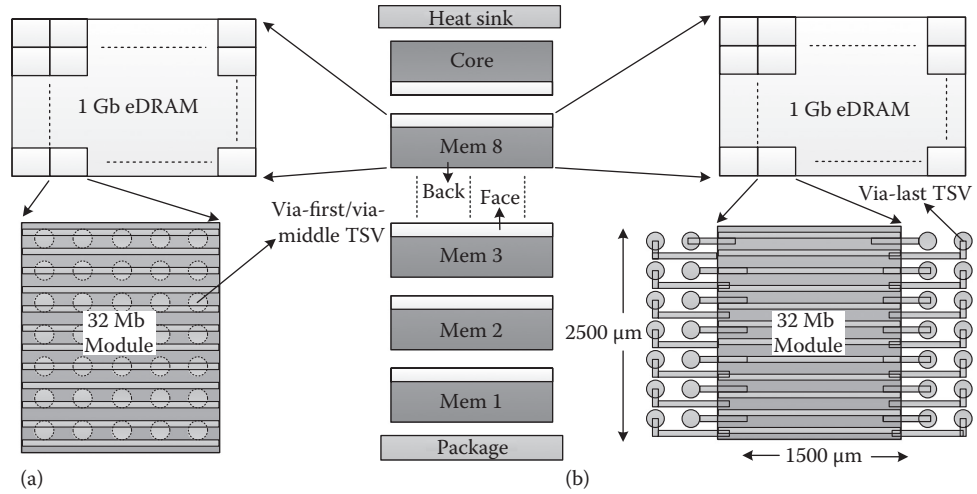

FIGURE 6.4 3D processor-memory stack: (a) via-first and via-middle TSVs and (b) via-last TSVs.

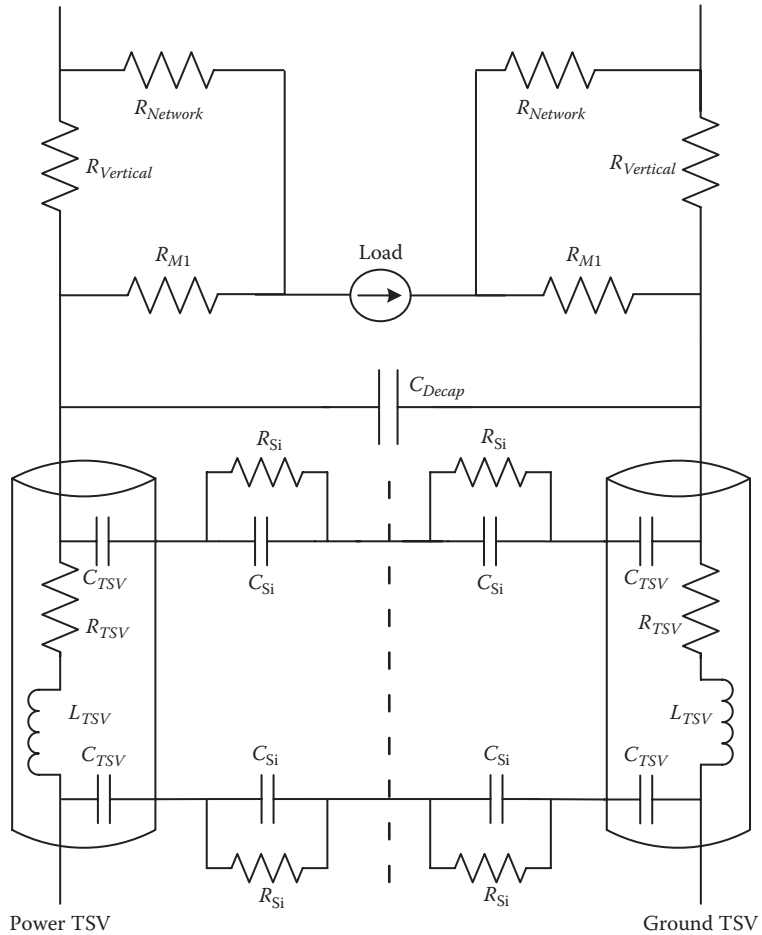

FIGURE 6.5 Equivalent power distribution network of each module within a plane.

TABLE 6.1
Primary Characteristics of Via-First (Filled with Polysilicon), Via-Middle (Filled with Tungsten), and Via-Last (Filled with Copper) TSVs

Parameter	Via-First	Via-Middle	Via-Last
Diameter, W	4 μm	4–2.66 μm	10 μm
Height, H	10 μm	60 μm	60 μm
Pitch, P	8 μm	8–9.34 μm	20 μm
Oxide thickness, t_{ox}	0.2 μm	0.2 μm	0.2 μm
TSV resistance, R_{TSV}	5.7 Ω	858.36 mΩ	20 mΩ
TSV inductance, L_{TSV}	4.18 pH	49.76 pH	34.94 pH
TSV capacitance, C_{TSV}	23 fF	117.81 fF	283 fF

AQ2 *Sources:* Agarwal, A. et al., Polysilicon interconnections (FEOL): Fabrication and characterization, in: *Proceedings of the IEEE Electronics Packaging Technology Conference*, December 2009, pp. 317–320; Katti, G. et al., *IEEE Trans. Electr. Devices*, 57(1), 256, January 2010; Pares, G. et al., Through silicon via technology using tungsten metallization, in: *Proceedings of the IEEE International Conference on IC Design and Technology*, pp. 1–4, May 2011.

The DRAM consumes 3 W, uniformly distributed across the eight stacks [57]. Alternatively, the processor consumes 90 W. Thirty percent of the overall power is due to static power dissipation whereas the remaining portion is due to dynamic power consumption [57]. A triangular current waveform is assumed with 400 ps period, 100 ps rise time, and 150 ps fall time. The DC current and peak current are determined based on, respectively, the static and dynamic power consumption.

6.3.1.3 Results

In 3D power distribution networks, it is important to determine the appropriate number of TSVs and decoupling capacitance that satisfy the constraint on power supply noise. From this design space, a valid pair that minimizes the physical area overhead is chosen. Note that this specific design point is dependent upon the implementation of the decoupling capacitance. Three methods are considered: (1) metal-oxide-semiconductor (MOS) capacitance in a 32-nm technology node with a capacitance density of 39.35 fF/μm^2 as determined from the equivalent oxide thickness (EOT) of the technology [55], (2) deep trench capacitance with a density of 140 fF/μm^2 [58], and metal-insulator-metal (MIM) capacitance with a density of 8 fF/μm^2 [59,60].

As an illustrative example, results for via-middle TSVs (filled with tungsten) are shown. The peak noise surface as a function of decoupling capacitance and number of TSVs is plotted in Figure 6.6a. As illustrated in this figure, the power supply noise monotonically decreases as the number of TSVs and decoupling capacitance increase. The noise contour at 100 mV (power supply noise constraint) is illustrated in Figure 6.6b. Any point on (and above) this curve satisfies the noise constraint. The physical area overhead for each of these points is depicted in Figure 6.7 for three different decoupling capacitance densities, as mentioned above. A specific design point exists where the physical area overhead is minimized. For example, if MOS capacitance is used, this design point is at 620 TSVs and 0.6 nF of decoupling capacitance.

A similar procedure is followed for via-first and via-last TSVs. The design points that minimize the physical area overhead while satisfying the power supply noise constraint are summarized in Table 6.2. The following important conclusions can be made based on these results:

- Highly resistive via-first TSVs (filled with polysilicon) can be used to deliver power at the expense of approximately 9% area overhead as compared to less than 2% area overhead in via-middle (filled with tungsten) and via-last (filled with copper) technologies.

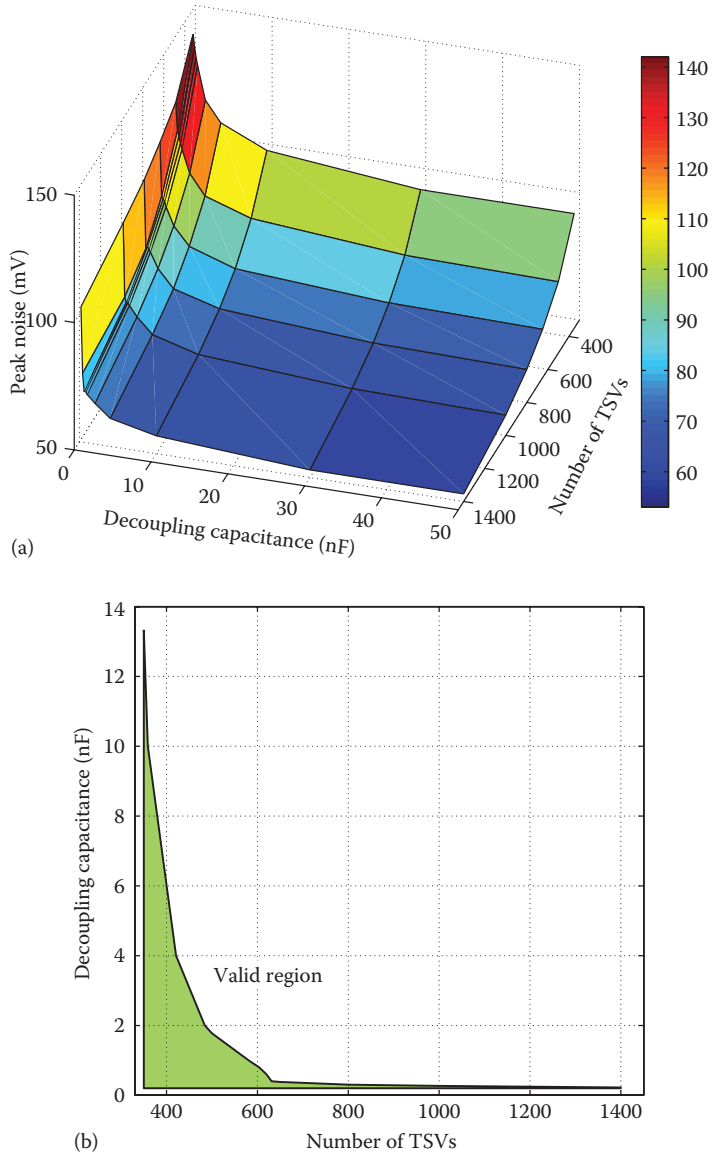

FIGURE 6.6 Peak noise characteristics as a function of number of TSVs and decoupling capacitance in via-middle TSV technology: (a) surface plot and (b) contour plot at 100 mV.

- Despite the higher area requirement, a power distribution network with via-first TSVs is typically overdamped and the issue of resonance is alleviated.
- For via-middle and via-last TSV technologies, the impedance at the resonant frequency should be sufficiently small. This issue is exacerbated for a via-last based power distribution network since the TSV resistance is significantly lower, and therefore the network is typically underdamped.

6.3.2 Decoupling Capacitors for Power-Gated 3D-ICs

In traditional topologies, the decoupling capacitance of a power-gated block (or plane) cannot provide charge to neighboring planes since these capacitors are typically connected to a virtual power

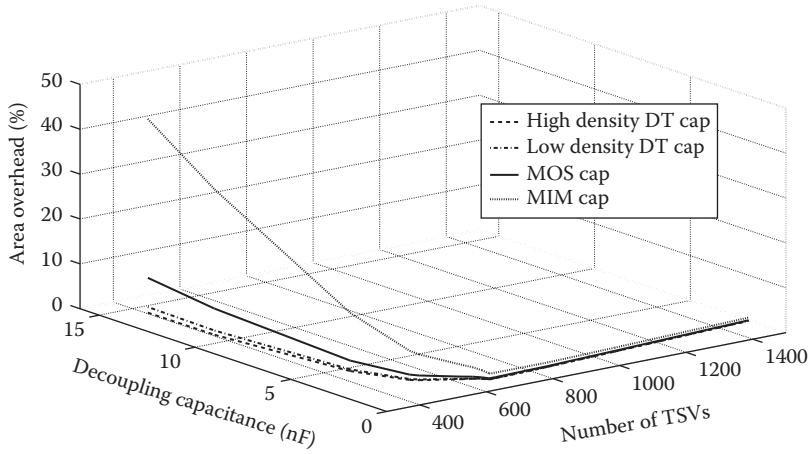

FIGURE 6.7 Area overhead in via-middle technology. Note that each point on the curve satisfies the target power supply noise.

AQ3

TABLE 6.2
Valid Design Points that Satisfy the Peak Power Supply Noise While Minimizing the Area Overhead for each TSV Technology

Cap Type	Cap Density (fF/μm²)	Area Overhead (%)	Number of TSVs	Decoupling Capacitance (nF)	Power Loss (%)	Peak Noise (mV)
Via-First						
MOS-C	39.35	9.06	2750	2.7	8.3	33.42
MIM	8	11.83	3437	0.8	7.3	23.5
Via-Middle						
MOS-C	39.35	1.96	620	0.60	6.7	63.56
DT	140	1.68	484	2	7.6	45.13
MIM	8	3.01	631	0.4	6.6	67.5
Via-Last						
MOS-C	39.35	1.54	76	0.385	4	134.72
DT	140	1.21	30	3.74	4.9	134.67
MIM	8	2.56	76	0.385	4	134.72

DT refers to deep trench.

network that is closer to the switching circuit [53]. Placing the decoupling capacitors sufficiently close to the switching load is helpful in reducing the power supply noise [61,62]. However, if the block or plane is power-gated, those capacitors that provide charge to the block (or plane) are disconnected from the global power network, making these capacitors ineffective for the neighboring planes. Since system-wide power integrity is a critical challenge in 3D-ICs, effective use of intentional decoupling capacitance is crucial, even when power gating is adopted.

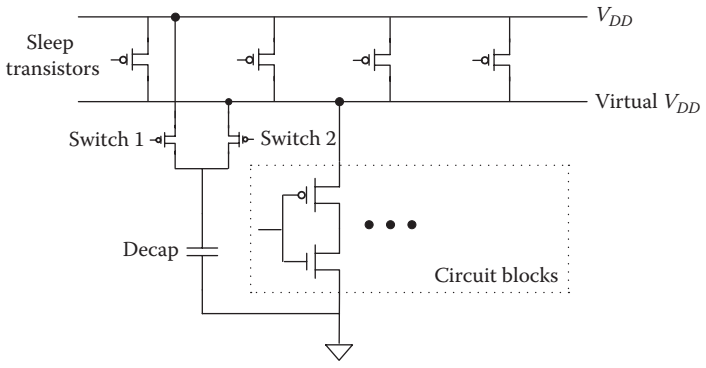

FIGURE 6.8 Conceptual representation of the reconfigurable decoupling capacitor topology with power gating.

It has been observed that the effective range of a decoupling capacitor exceeds single plane in 3D-ICs with low-resistance TSVs [63]. This phenomenon is important particularly when block- or plane-level power gating is performed due to significant decoupling capacitance that cannot provide charge to the remaining, active planes. Thus, when one or more number of planes is power-gated, power supply noise in one of the remaining active planes may increase and violate the constraint despite a reduction in the overall switching current drawn from the power supply. It is therefore highly critical to ensure that the decoupling capacitors within the power-gated planes are not ineffective for the remaining planes. A reconfigurable decoupling capacitor topology is described in the following section to alleviate this issue [53].

6.3.2.1 Reconfigurable Topology

In the reconfigurable topology, two switches are used to form a configurable decoupling capacitor, as conceptually illustrated in Figure 6.8 [64]. If a certain plane is active, the decoupling capacitors on that plane are connected to the virtual V_{DD} grid through switch 2, thereby reducing the power supply noise on that plane. Alternatively, if the plane is power-gated (sleep transistors are turned off), the decoupling capacitors are connected to the global V_{DD} grid, bypassing the sleep transistors. Thus, even if the plane is power-gated, the decoupling capacitors are effective for the remaining planes. The overhead of this topology includes the reconfigurable switches, metal resources required to route the related control signals, and a possible increase in overall power consumption depending upon how the capacitors are implemented, as discussed in the following section.

6.3.2.2 Evaluation Setup

A power distribution network for a three-plane 3D-IC with via-last TSVs is developed, as conceptually illustrated in Figure 6.9 for a single plane [53]. A 45-nm CMOS technology with 10 available metal layers in each plane is adopted [65]. A portion of the power network with an area of 1 mm × 1 mm is analyzed. Each plane consists of a global power network, virtual power network, distributed PMOS sleep transistors, distributed decoupling capacitance (implemented as MOS capacitors), and distributed switching load circuit consisting of inverter gates, as depicted in Figure 6.9. Top two metal layers (9 and 10) on each plane are dedicated to global power distribution network with an interdigitated grid of 11 × 11. Metal layers 8 and 7 are used as the virtual power network represented by an interdigitated grid of 21 × 21 [66]. Power gating is achieved using a distributed method where the sleep transistors that control a plane are placed within that plane [67]. Note that the top plane also consists of C4 bumps to connect the on-chip grid with the flip-chip substrate.

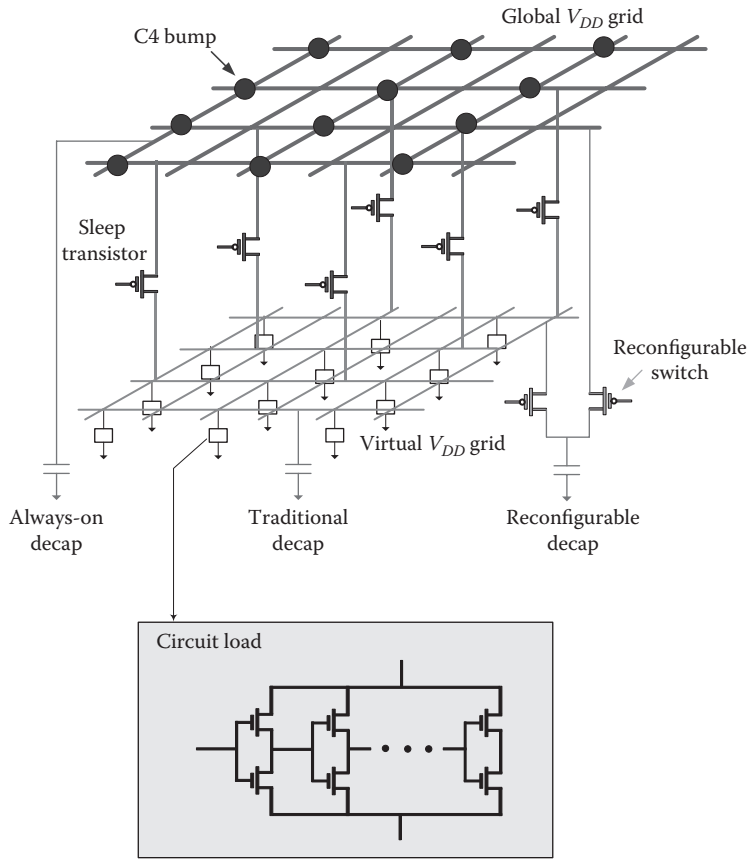

FIGURE 6.9 Plane-level power network illustrating distributed sleep transistors, decoupling capacitors (traditional and proposed topologies), switching load circuits (gates with active devices), and the C4 bumps (for the top plane only).

Similar to [68], inverter pairs with varying number and size are used to model the switching load circuit. The overall area is divided into 30 sub-areas and a switching circuit is connected to each sub-area to consider the spatial heterogeneity of the current loads. The spatial load current distribution and power densities are based on [69] where the peak power density reaches 40W/cm^2, comparable to the power density in modern processors [70]. All of the decoupling capacitors are implemented as MOS capacitors in the 45-nm technology with an oxide thickness of 1 nm [65].

6.3.2.3 Results

The efficacy of the reconfigurable decoupling capacitor placement topology is evaluated by comparing the methodology with the traditional topology where the capacitors are connected to a virtual power grid. Both power supply noise and power gating noise are analyzed. Three power gating scenarios are considered:

- *Scenario 1*: All of the three planes are active, representing the greatest workload.
- *Scenario 2*: The top and bottom planes are active, while the middle plane is power-gated.
- *Scenario 3*: Only the bottom plane is active, while the middle and top planes are power-gated.

Power supply noise results are listed in Table 6.3 for each scenario. As listed in this table, when some of the planes are power-gated (scenarios 2 and 3), the reconfigurable topology achieves less power

TABLE 6.3
Power Supply Noise Obtained from Each Scenario and Noise Reduction Achieved by Reconfigurable Topology

				Power Supply Noise (mV)					
	Power Status			Traditional		Reconfigurable			
	Top	Mid	Btm	Peak	RMS	Peak	Redtn. (%)	RMS	Redtn. (%)
Scenario 1	On	On	On	50	30.27	50	N/A	28.33	6.4
Scenario 2	On	Off	On	48.94	23.41	42.90	12.3	16.79	28.3
Scenario 3	Off	Off	On	52.86	17.53	38.34	27.4	9.39	46.4

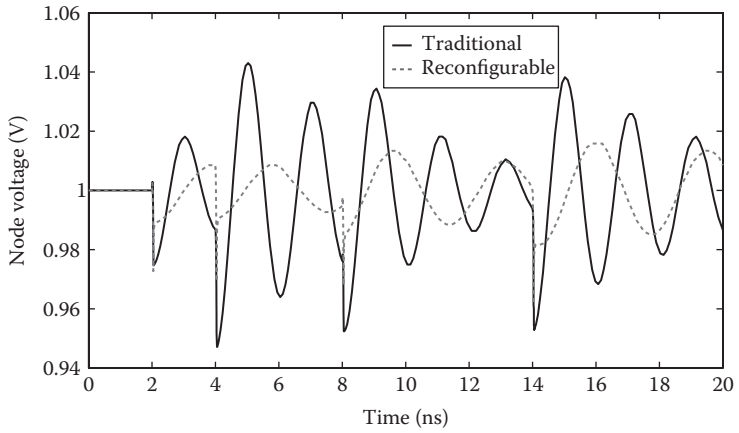

FIGURE 6.10 Transient behavior of voltage noise at a specific node within the bottom plane for each topology for scenario 3.

supply noise by exploiting the capacitors of the power-gated plane(s). For example, in scenario 3 where two planes are power-gated, the reduction in peak noise is approximately 27%, whereas the reduction in RMS noise is approximately 46%. Note that in the traditional topology, the peak noise in scenario 3 exceeds 50 mV despite the reduction in overall switching current due to power gating. This characteristic is due to less decoupling in the power network since the decoupling capacitors in the power-gated planes cannot behave as charge reservoirs for the remaining, active planes. This observation justifies the need for reconfigurable capacitors. Transient behavior of voltage noise at a specific node within the bottom plane is also depicted in Figure 6.10 for scenario 3, demonstrating the reduction in peak and RMS noise.

To investigate power gating noise, the power-gated middle plane transitions from inactive to active state in scenarios 2 and 3, and the voltage fluctuation due to in-rush current during the wake-up process is analyzed. Peak power gating noise is observed at the bottom plane. Results are listed in Table 6.4. The reconfigurable topology achieves more than 80% reduction in peak and RMS power gating noise. In traditional topology, a significant amount of in-rush current flows not only for the activated circuit, but also to charge the associated decoupling capacitors. Alternatively, in the reconfigurable topology, the decoupling capacitors are connected to the global V_{DD} grid when the plane is power-gated. Thus, even if the plane is power-gated, these capacitors remain charged (significantly reducing in-rush current) and can behave as charge reservoir once the plane transitions to active state. The transient behavior of the power gating noise is illustrated in Figure 6.11 for scenario 3 where the transition happens at 1 ns.

TABLE 6.4
Power Gating Noise Obtained from Each Scenario and Noise Reduction Achieved by Reconfigurable Topology

				Power Gating Noise (mV)					
	Power Status			Traditional		Reconfigurable			
	Top	Mid	Btm	Peak	RMS	Peak	Redtn. (%)	RMS	Redtn. (%)
Scenario 1	On	On	On	N/A			N/A		
Scenario 2	On	Off	On	90.73	72.83	15.55	82.8	11.46	84.2
Scenario 3	Off	Off	On	103.2	78.76	15.66	84.8	11.57	85.3

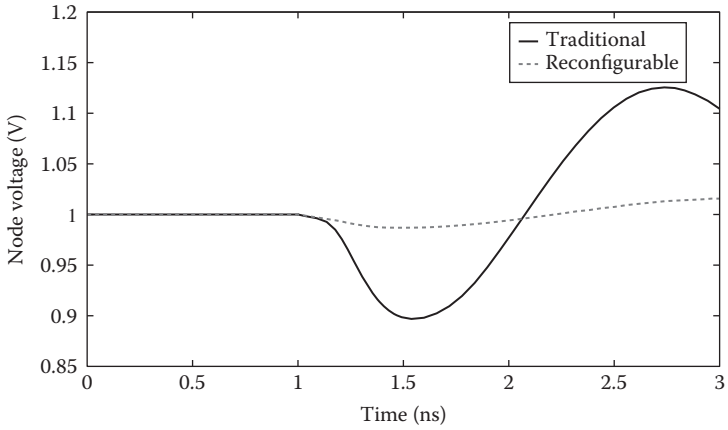

FIGURE 6.11 Transient behavior of power gating noise at a specific node within the bottom plane for each topology for scenario 3.

In the reconfigurable topology, the physical area overhead increases by only 1.55% due to reconfigurable switches and higher decoupling capacitance required to compensate for the shielding effect of the reconfigurable switches. This slight increase in the physical area significantly enhances power integrity when one or more planes are power-gated, as described above.

To quantify the power overhead of the reconfigurable topology, both topologies are simulated for each scenario and the overall average power consumption is determined. All of the decoupling capacitors are implemented as MOS capacitors to consider MOS-C leakage. It is observed that the maximum power (drawn in scenario 1) increases by only 1.36% due to increased capacitance and switches. This power overhead can be further reduced if low leakage decoupling capacitor implementations are adopted such as metal-insulator-metal (MIM) capacitors.

6.4 SYSTEM-WIDE 3D SIGNAL INTEGRITY

In addition to traditional noise coupling and propagation mechanisms such as crosstalk, power supply noise, and substrate coupling, 3D-ICs suffer from TSV-induced noise coupling [71–73]. Specifically, during a signal transition within a TSV, noise couples from TSV into the substrate due to both dielectric and depletion capacitances. The coupling noise propagates throughout the substrate and affects the reliability of nearby transistors [74]. This issue is exacerbated for TSVs that carry signals with high switching activity factors and fast transitions such as clock signals.

Analog/RF blocks and memory cells are among the most sensitive circuits to substrate noise coupling [75–78]. For example, in [79], experimental data demonstrate that the signal-to-noise-plus-distortion ratio (SNDR) of a delta-sigma modulator is reduced by more than 20 dB due to substrate noise. Note that in heterogeneous 3D systems, the front-end circuitry consisting of analog/RF blocks is typically located at the top plane (closer to the I/O pads) to reduce the overall impedance between the pads and analog inputs. In this floorplan, TSVs are required to transmit the digital signals (including the clock signal) to the data processing plane. Thus, TSV-induced noise becomes an important issue for the reliability of the analog/RF blocks. Digital transistors are also affected by TSV-induced noise if the physical distance between the TSV and device is sufficiently short [80]. TSV-induced noise changes the drain current characteristics of both an on and off transistor, as observed in [81].

A methodology is described in Section 6.4.1 to efficiently analyze TSV-to-transistor noise coupling in 3D-ICs. A case study is presented in Section 6.4.2 to better understand noise propagation paths within a 3D environment.

6.4.1 Efficient Analysis of TSV-to-Transistor Noise Coupling

To characterize TSV-induced noise coupling, the physical structure depicted in Figure 6.12 is used. This structure consists of a noise injector (TSV), noise transmitter (substrate), and a noise receptor (victim transistor). Substrate contacts are also included to bias the substrate. Note that the number and placement of substrate contacts between the TSV and victim transistor play an important role in the noise coupling analysis. To analyze this physical structure, several approaches have been adopted such as using an electromagnetic field solver, device simulator, and a highly distributed model using 3D transmission line matrix (TLM) method [82–84], as described in the following subsection.

6.4.1.1 Distributed Model

In the distributed model, the physical structure is discretized into unit cells (for both TSV and substrate) and each unit cell is modeled with lumped parasitic impedances. Both the measurement and 3D field solver results demonstrate that the 3D-TLM model can accurately model the 3D physical structure including a TSV, substrate contact, and victim transistor [82,85]. Despite the reasonable accuracy achieved by the distributed model, the computational complexity is significantly high, particularly when the dimensions of the unit cells are small. This issue is exacerbated as the distance between the TSV and victim transistor increases. Furthermore, the number and location of the substrate contacts play an important role in characterizing the TSV safe zone. Re-analysis of the distributed structure when these characteristics change is computationally prohibitive. Therefore, a compact model is needed to alleviate these limitations, as described in the following section. This highly distributed model is used as a reference to validate the compact model and closed-form expressions.

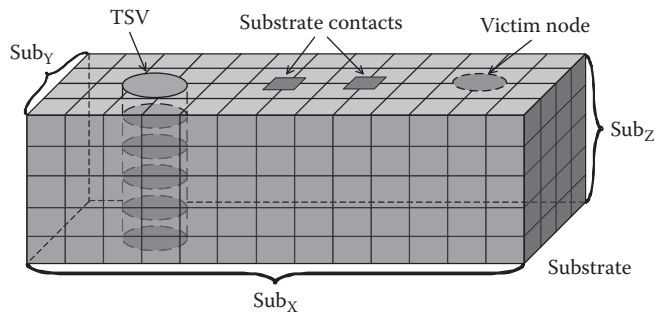

FIGURE 6.12 Physical structure used to analyze TSV-induced noise coupling.

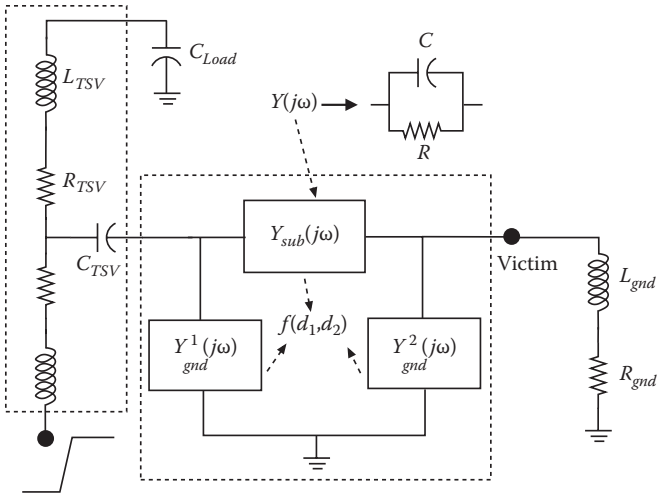

FIGURE 6.13 Compact π model to efficiently estimate the noise at the victim node in the presence of a TSV and substrate contacts.

6.4.1.2 Compact Model

A two-port, linear time-invariant network can be generally characterized with four admittances: $Y_{11}(j\omega)$, $Y_{12}(j\omega)$, $Y_{21}(j\omega)$, and $Y_{22}(j\omega)$. Utilizing this characteristic, the proposed compact model consists of a single TSV cell and an equivalent two-port π network to model noise propagation, as depicted in Figure 6.13 [73]. Each electrical element within the π network consists of a parallel *RC* circuit, producing an admittance $(1/R) + j\omega C$. These admittances can be obtained from the distributed mesh (based on 3D-TLM method), as described in the previous section. Specifically, the four $Y(j\omega)$ parameters of the distributed mesh are obtained through an AC analysis. The resistances and capacitances within the π network are determined such that the four $Y(j\omega)$ parameters of the compact π network are equal to the respective $Y(j\omega)$ parameters of the distributed mesh. According to this procedure, the admittances within the π network $Y_{sub}(j\omega)$, $Y^1_{gnd}(j\omega)$, and $Y^2_{gnd}(j\omega)$ are determined as follows:

- $Y_{sub}(j\omega) = (1/R_{sub}) + j\omega C_{sub} = Y_{21}(j\omega)$: represents the equivalent substrate admittance between the TSV and victim transistor.
- $Y^1_{gnd}(j\omega) = (1/R^1_{gnd}) + j\omega C^1_{gnd} = Y_{11}(j\omega) - Y_{21}(j\omega)$: represents the equivalent substrate admittance between the TSV and ground node.
- $Y^2_{gnd}(j\omega) = (1/R^2_{gnd}) + j\omega C^2_{gnd} = Y_{22}(j\omega) - Y_{21}(j\omega)$: represents the equivalent substrate admittance between the victim node and ground node.

In the next step, each resistive and capacitive element within each $Y(j\omega)$ of the π network are characterized as a function of d_1 and d_2, where d_1 and d_2 are depicted in Figure 6.14. Via-first and via-last TSVs are separately analyzed. To evaluate the dependencies of *R* and *C* on d_1 and d_2, AC analyses of the distributed mesh (based on 3D-TLM) described in the previous section are performed with different values of d_1 and d_2. The data obtained in this step are used to generate a 3D surface for each resistance and capacitance within $Y_{sub}(j\omega)$, $Y^1_{gnd}(j\omega)$, and $Y^2_{gnd}(j\omega)$. This surface is approximated with a logarithmic function using a 3D least square regression analysis. The logarithmic function $F(d_1, d_2)$ used to approximate the admittances of the π network as a function of the physical distances d_1 and d_2 is

$$F(d_1, d_2) = A + Bd_1 + Cd_2 + D\ln d_2 + E\ln d_1, \tag{6.1}$$

where *A*, *B*, *C*, *D*, and *E* are fitting coefficients. These fitting coefficients are determined such that the resistor/capacitor value obtained from this expression reasonably approximates the actual

resistor/capacitor value (in the compact π model) that is obtained from the highly distributed 3D TLM model. Note that both the resistance (in kΩ s) and capacitance (in attoFarads) of each $Y(j\omega)$ within the π network are represented by the function *F*. Also note that the distances d_1 and d_2 are in μm. Since the π network has three admittances each consisting of a parallel *RC* circuit, six logarithmic functions are developed for via-first and via-last TSVs, producing a total of 12 functions. The fitting coefficients for each function are listed in Table 6.5.

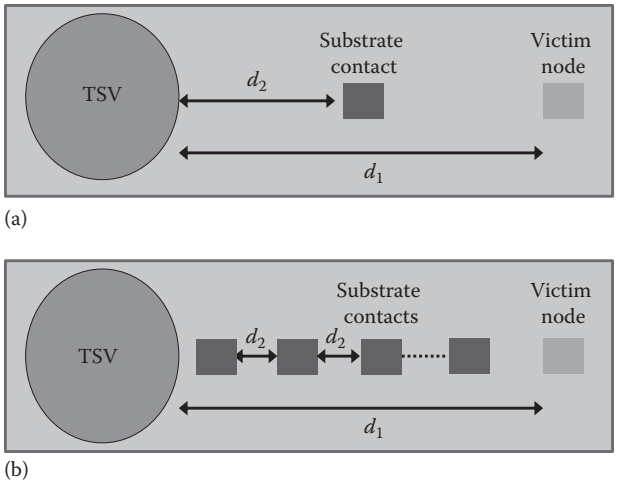

FIGURE 6.14 Substrate contact between TSV and victim node. AQ4

TABLE 6.5
Fitting Coefficients for the Function *F* that Approximates the Admittances within the Compact Model (see Figure 6.13) for Via-First and Via-Last TSVs

		Fitting Coefficients					
Cases	**Admittances**	***A***	***B***	***C***	***D***	***E***	**Error (%)**
	$R_{sub} = 1000/F$	27.09	0	0	−0.98	−5.11	6.6
	$C_{sub} = F$	326.7	0.41	0.48	−17.26	−67.55	2.8
Via-first	$R^1_{gnd} = 1000/F$	28.31	0	0	−8.14	1.98	1.9
	$C^1_{gnd} = F$	301.3	−0.28	0.66	−96.94	30.09	1.6
	$R^2_{gnd} = F$	45.91	2.30	3.08	−218.3	154.9	9.6
	$C^2_{gnd} = 1000/F$	8.05	0.28	0.29	−20.39	12.49	10.4
	$R_{sub} = 1000/F$	27.35	−0.082	0.036	−2.11	−1.12	2.4
	$C_{sub} = F$	296.6	−0.89	0.83	−20.78	−13.12	1.9
Via-last	$R^1_{gnd} = 1000/F$	36.16	0.028	0.39	−10.16	1.18	2.4
	$C^1_{gnd} = F$	235.6	−1.18	−2.16	−61.86	51.91	6.9
	$R^2_{gnd} = 1000/F$	11.57	0.11	−0.19	4.43	−5.86	11.6
	$C^2_{gnd} = F$	129.1	1.18	−2.22	49.1	−65.23	10.9

The function *F* is given by Equation 6.1. All resistances are in kΩ s and all capacitances are in attoFarads.

6.4.1.3 Results and Design Guidelines

The compact π model contains only 11 number of elements for both via-first and via-last TSVs where each element is represented by Equation 6.1 with five fitting coefficients. Alternatively, the number of circuit elements in the distributed model (based on 3D-TLM) can exceed a million when the unit cell dimension is 1 μm.

According to Table 6.5, maximum average error is slightly over 10% for certain resistances and capacitances. This error, however, does not significantly affect the electrical characteristics (and noise estimation at the victim node) since the maximum error occurs at the extreme cases when the resistance is sufficiently large and capacitance is sufficiently small. Also note that the average error over via-first and via-last TSVs is approximately 6%.

The compact model illustrated in Figure 6.13, Equation 6.1, and fitting parameters listed in Table 6.5 can be used to investigate the effect of various design and fabrication parameters such as placement of substrate contacts and TSV type. As an example, the effect of increasing d_1 (placing the victim farther from the TSV) on peak noise is investigated for both via-first and via-last TSVs. The results are shown in Figure 6.15. According to this figure, placing the victim transistor farther from the switching TSV is an effective method for via-first TSVs. Alternatively, for via-last TSVs, the noise exhibits low sensitivity to the distance between TSV and victim transistor. This phenomenon can be explained by longer height (therefore smaller substrate resistances) and larger diameter (therefore larger capacitances) of via-last TSVs.

6.4.2 Case Study: SI Analysis of a 3D-Integrated SoC

The primary objective of this study is to evaluate the signal integrity characteristics of a 3D-integrated mixed-signal circuit and compare the results with a 2D implementation. It is typically assumed that the noise performance of a 3D circuit is superior than a 2D system since the aggressor and victim blocks can be placed on separate planes, thereby enhancing signal isolation [5,7]. The validity of this assumption is evaluated by developing a comprehensive electrical model for both 2D and 3D versions of the same circuit. The circuit functionality, architecture, and signal integrity modeling approach are described in the following subsections.

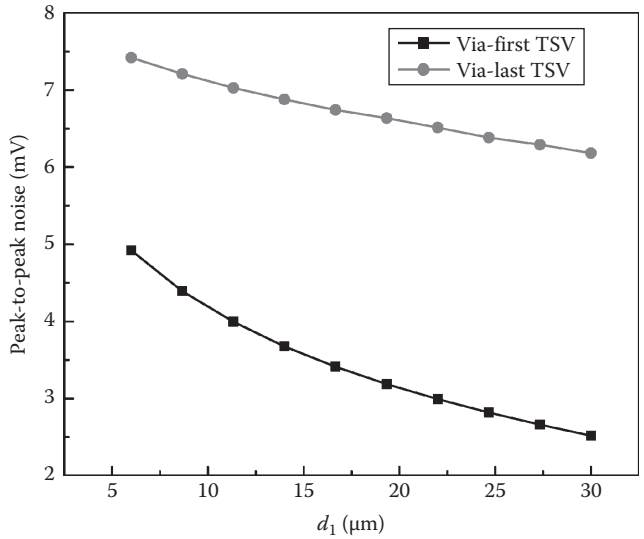

FIGURE 6.15 TSV-induced switching noise at the victim node as a function of d_1 at constant d_2 for via-first and via-last TSVs.

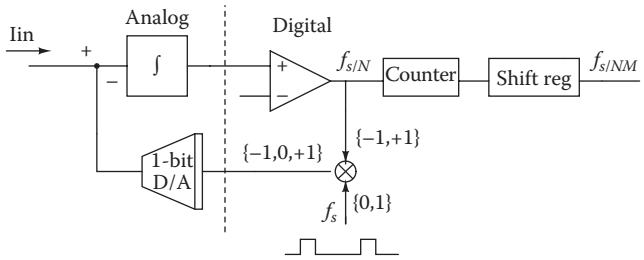

FIGURE 6.16 System level diagram of a single channel of the potentiostat. (From Stanacevic, M. et al. *IEEE Trans. Biomed. Circ. Syst*., 1(1), 63, March 2007; Genov, R. et al., *IEEE Trans. Circ. Syst. I: Regular Pap*., 53(11), 2371, November 2006.)

6.4.2.1 Potentiostat Architecture

A 16-channel VLSI potentiostat chip, designed and fabricated in 0.5 μm CMOS technology, simultaneously records neurotransmitter levels from multiple neurons [86,87]. The detection of the neurotransmitters is critical for neural pathways and the etiology of neurological diseases like epilepsy and stroke [88]. High sensitivity and wide dynamic range are critical design objectives since the measured currents are in the picoampere range. Thus, an accurate evaluation of signal integrity is critical.

To manage computational complexity, the proposed signal integrity analysis focuses on a single channel that consists of a first-order delta-sigma modulator, counter for decimation, and shift register, as depicted in Figure 6.16 [86,87]. Delta-sigma modulator consists of a current integrator, comparator, and switched-current 1-bit D/A converter in the feedback loop. The counter is the primary aggressor whereas the sense amplifier within the current integrator is identified as one of the primary victim blocks. The switching noise that couples from the counter to the sense amplifier is analyzed for different scenarios, as described in the following subsections.

6.4.2.2 3D Signal Integrity Modeling

Highly distributed 3D electrical models based on TLM method (as described in Section 6.4.1) are utilized to analyze signal integrity. Both the substrate and TSVs are discretized using unit cells consisting of *RLC* impedances, and an entire electrical model for a single channel of a neurotransmitter chip is generated in both 2D and 3D technologies.

In the 3D-integrated potentiostat, the aggressor (counter) and victim (delta-sigma modulator) are placed on separate planes. Specifically, the top plane (closer to the I/O pads) is dedicated to the victim block whereas the bottom plane (closer to the heat sink) is dedicated to the aggressor block. A conceptual representation of the electrical model is depicted in Figure 6.17. The bulk nodes within the schematic are connected to the corresponding nodes on the substrate. Two separate substrates exist: (1) substrate of the bottom plane where the bulks of the counter are connected, and (2) substrate of the upper plane where the bulks of the delta-sigma modulator are connected. As depicted in Figure 6.17, a face-to-face bonding technology is assumed with via-first fabrication technique. In this technique, the TSVs go through the upper (analog) substrate and reaches the metal layers of the analog plane. The topmost metal layer of the analog plane is connected to the topmost metal layer of the digital plane using bumps. Since only a single channel of the device is modeled, eight TSVs are required: five for the clock signals (each at 1 MHz), two for power supply voltage (3 V), and one for data signal. Signal integrity results are described in the following subsection.

6.4.2.3 Results

A transient analysis is performed and the noise at the bulk of the victim device is observed. Peak noise is illustrated in Figure 6.18 for two different cases: (1) nonideal TSVs with practical capacitance values, (2) ideal TSVs with zero capacitance value. Note that the result of the 2D analysis is also included for comparison. As depicted in this figure, the 3D system with practical TSVs, despite

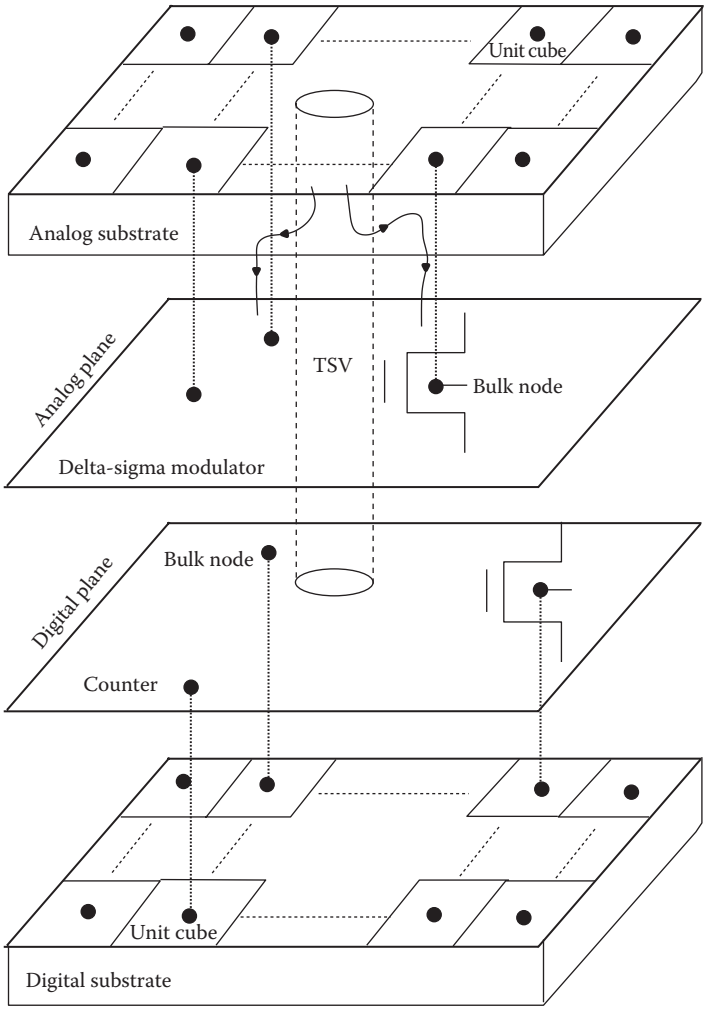

FIGURE 6.17 Conceptual representation of the overall model to analyze signal integrity in a 3D potentiostat.

having separate substrates for aggressor and victim, exhibit significantly higher noise (positive peak noise exceeds 6 mV) than the 2D system.

To determine the primary noise source, the TSV capacitance C_{TSV} of the clock TSVs is removed, producing an ideal clock TSV with no coupling into the substrate. In this case, the peak noise is significantly reduced (to approximately 2 mV) and is smaller than the 2D system. Thus, in a 3D system, significant noise couples into the substrate through clock TSVs. The same conclusion is validated by observing the RMS noise over 10 μs, as listed in Table 6.6 for all of the cases. The RMS noise is reduced by more than 50% only if the TSVs are ideal, that is, TSV-to-substrate noise coupling is prevented.

For applications such as the neurotransmitter sensing as described in this section, the top plane of a 3D-IC should be dedicated to the highly sensitive frontend circuits due to physical proximity to the pads. In this case, however, clock TSVs with short rise times inject significant noise into the substrate of the analog plane since these signals need to reach the bottom plane where the digital circuit is placed. This coupling mechanism is due to the TSV-to-substrate capacitance C_{TSV} of the TSVs. Thus, the distance between an aggressor TSV and a victim device should be carefully considered. Efficient and 3D-specific signal isolation strategies should also be developed.

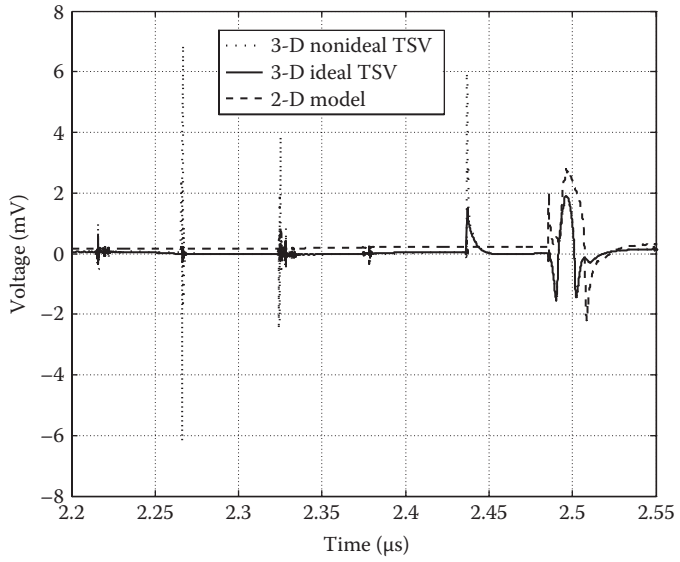

FIGURE 6.18 Transient analysis results illustrating peak noise at the bulk node of a victim device for two different cases in a 3D integrated potentiostat.

TABLE 6.6
RMS Value of the Noise at the Bulk Node over 10 μs for Different Cases

Case	RMS Noise at the Bulk Node of the Victim Block (μV)
2D potentiostat	232
3D potentiostat with nonideal TSV	242
3D potentiostat with ideal TSV	107

6.5 SUMMARY AND CONCLUSIONS

TSV-based 3D technologies facilitate higher and heterogeneous integration, enable enhanced performance while reducing the overall power consumption. Despite various challenges at the fabrication level (such as developing low cost and high aspect ratio vertical vias and reliable bonding technologies at lower temperatures), no fundamental limitations exist. A similar argument applies to the design process where significant research has been conducted during the past decade. TSV-based 3D-ICs enable exciting opportunities not only for high-performance computing systems, but also for low-power SoCs with application to mobile computing, life sciences, and environment control.

This chapter has focused on two important issues encountered during the physical design process of 3D SoCs: power and signal integrity. An overview of existing TSV technologies was first provided to better understand the implications of each TSV technology on power delivery and signal integrity. A case study was described to illustrate power distribution in a nine-plane 3D processor-DRAM stack. According to the International Technology Roadmap for Semiconductors, processor-memory stacks are expected to be one of the early applications of TSV-based 3D-ICs where the issue of power integrity is exacerbated [89].

Next, the importance of power gating has been emphasized for 3D-ICs. It was shown that conventional decoupling capacitor topologies can degrade power integrity when one or more planes are power-gated. A reconfigurable decoupling capacitor topology was discussed to alleviate this

issue and significantly enhance power integrity with relatively small overhead in physical area and power consumption.

An important concern, particularly in heterogeneous 3D integration with sensitive analog/RF blocks, is TSV-to-transistor noise coupling. This signal integrity concern was described and two approaches (that exhibit distinct accuracy versus complexity tradeoffs) were presented to analyze noise coupling in 3D-ICs. Finally, another case study of a 3D-IC with application to bio-electronics (neurotransmitter sensing) was discussed with emphasis on 3D signal integrity. It was demonstrated that the expected signal isolation advantages of 3D-ICs are possible if TSV-to-substrate noise coupling is significantly reduced.

REFERENCES

AQ5

1. R. J. Gutmann et al. Three-dimensional (3D) ICs: A technology platform for integrated systems and opportunities for new polymeric adhesives. In *Proceedings of the IEEE International Conference on Polymers and Adhesives in Microelectronics and Photonics*, pp. 173–180, October 2001.
2. A. W. Topol et al. Three-dimensional integrated circuits. *IBM Journal of Research and Development*, 50(4/5):491–506, July/September 2006.

AQ6

3. E. Salman and E. G. Friedman. *High Performance Integrated Circuit Design*, 1st edn. McGraw-Hill, September 2012.
4. J. U. Knickerbocker et al. Three dimensional silicon integration. *IBM Journal of Research and Development*, 52(6):553–569, November 2008.
5. K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat. 3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration. *Proceedings of the IEEE*, 89(5):602–633, May 2001.
6. V. F. Pavlidis and E. G. Friedman. Interconnect-based design methodologies for three-dimensional integrated circuits. *Proceedings of the IEEE*, 97(1):123–140, January 2009.
7. V. F. Pavlidis and E. G. Friedman. *Three-Dimensional Integrated Circuit Design*. Morgan Kaufmann, 2009.
8. C. Liu, I. Ganusov, M. Burtscher, and S. Tiwari. Bridging the processor-memory performance gap with 3D IC technology. *IEEE Design and Test of Computers*, 22(6):556–564, November–December 2005.
9. G. Loh. 3D-stacked memory architectures for multi-core processors. In *Proceedings of the International Symposium on Computer Architecture*, pp. 453–464, June 2008.
10. Q. Wu, K. Rose, J.-Q. Lu, and T. Zhang. Impacts of through-dram vias in 3D processor-dram integrated systems. In *Proceedings of IEEE International Conference on 3D System Integration*, pp. 1–6, September 2009.
11. U. Kang et al. 8 Gb 3-d ddr3 dram using through-silicon-via technology. *IEEE Journal of Solid-State Circuits*, 45(1):111–119, January 2010.
12. A. B. Kahng. Scaling: More than Moore's Law. *IEEE Design and Test of Computers*, 27(3):86–87, May–June 2010.
13. G. Q. Zhang, M. Graef, and F. van Roosmalen. The rationale and paradigm of More than Moore. In *Proceedings of the IEEE International Conference on Electronic Components and Technology*, pp. 151–157, May–June 2006.
14. G. M. Walker, J. M. Ramsey, R. K. Cavin, D. J. C. Herr, C. I. Merzbacher, and V. Zhirnov. A framework for bioelectronics discovery and innovation. Technical report, The Semiconductors Electronics Division, National Institute of Standards and Technology, February 2009.
15. S. Wong, A. El-Gamal, P. Griffin, Y. Nishi, F. Pease, and J. Plummer. Monolithic 3D integrated circuits. In *Proceedings of the IEEE International Symposium on VLSI Technology, Systems and Applications*, pp. 23–25, April 2007.
16. P. Batude et al. GeOI and SOI 3D monolithic cell integrations for high density applications. In *Proceedings of the IEEE International Symposium on VLSI Technology*, June 2009.
17. M. Vinet et al. 3D monolithic integration: Technological challenges and electrical results. *Microelectronic Engineering*, 88(4):331–335, April 2011.
18. E. Beyne. The rise of the 3rd dimension for system integration. In *Proceedings of the IEEE International Conference on Interconnect Technology*, pp. 1–5, June 2006.
19. J. Miettinen, M. Mantysalo, K. Kaija, and E.O. Ristolainen. System design issues for 3D system-in-package (sip). In *Proceedings of the IEEE Electronic Components and Technology Conference*, pp. 610–615, June 2004.

20. W. J. Howell et al. Area array solder interconnection technology for the three-dimensional silicon cube. In *Proceedings of the IEEE Electronic Components and Technology Conference*, pp. 1174–1178, May 1995.
21. C. L. Chen et al. Wafer-scale 3D integration of silicon-on-insulator RF amplifiers. In *Proceedings of the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 1–4, January 2009.
22. S. Koester et al. Wafer-level 3D integration technology. *IBM Journal of Research and Development*, 52(6):583–597, November 2008.
23. A. Zeng, J. Lu, K. Rose, and R. J. Gutmann. First-order performance prediction of cache memory with wafer-level 3D integration. *IEEE Design and Test of Computers*, 22(6):548–555, November-December 2005.
24. R. S. Patti. Three-dimensional integrated circuits and the future of system-on-chip designs. *Proceedings of the IEEE*, 94(6):1214–1224, June 2006.
25. J. Burns et al. three-dimensional integrated circuits for low-power, high-bandwidth systems on a chip. In *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 268–269, February 2001.
26. J.-Q. Lu. 3-D hyperintegration and packaging technologies for micro–nano systems. *Proceedings of the IEEE*, 97(1):18–30, January 2009.
27. T. Zhang et al. 3-D data storage, power delivery, and RF/optical transceiver—Case studies of 3-D integration from system design perspectives. *Proceedings of the IEEE*, 97(1):161–174, January 2009.
28. F. Niklaus, G. Stemme, J.-Q. Lu, and R. Gutmann. Adhesive wafer bonding. *Journal of Applied Physics*, 99(3):101.1–101.28, February 2006.
29. J.-Q. Lu et al. Stacked chip-to-chip interconnections using wafer bonding technology with dielectric bonding glues. In *Proceedings of the IEEE International Conference on Interconnect Technology*, pp. 219–221, June 2001.
30. K. Warner et al. Low-temperature oxide-bonded three-dimensional integrated circuits. In *Proceedings of the IEEE International SOI Conference*, pp. 123–124, October 2002.
31. P. R. Morrow, C.-M. Park, S. Ramanathan, M. J. Kobrinsky, and M. Harmes. Three-dimensional wafer stacking via Cu–Cu bonding integrated with 65-nm strained-Si/low-k CMOS technology. *IEEE Electron Device Letters*, 27(5):335–337, May 2006.
32. S. Halder et al. Metrology and inspection for process control during bonding and thinning of stacked wafers for manufacturing 3D SIC's. In *Proceedings of the IEEE Electronic Components and Technology Conference*, pp. 999–1002, May–June 2011.
33. Y. S. Kim et al. Ultra thinning 300-mm wafer down to 7-μm for 3D wafer integration on 45-nm node CMOS using strained silicon and Cu/low-K interconnects. In *Proceedings of the IEEE International Electron Devices Meeting*, pp. 1–4, December 2009.
34. S. M. Satheesh and E. Salman. Power distribution in TSV-based 3-D processor-memory stacks. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2(4):692–703, December 2012.
35. C. Laviron et al. Via first approach optimization for through silicon via applications. In *Proceedings of the IEEE Electronic Components and Technology Conference*, pp. 14–19, May 2009.
36. G. Pares et al. Mid-process through silicon vias technology using tungsten metallization: Process optimization and electrical results. In *Proceedings of the IEEE Electronics Packaging Technology Conference*, pp. 772–777, December 2009.
37. G. Pares et al. Through silicon via technology using tungsten metallization. In *Proceedings of the IEEE International Conference on IC Design and Technology*, pp. 1–4, May 2011.
38. S. Ramaswami et al. Process integration considerations for 300 mm TSV manufacturing. *IEEE Transactions on Device and Materials Reliability*, 9(4):524–528, December 2009.
39. A. Agarwal, R. B. Murthy, V. Lee, and G. Viswanadam. Polysilicon interconnections (FEOL): Fabrication and characterization. In *Proceedings of the IEEE Electronics Packaging Technology Conference*, pp. 317–320, December 2009.
40. M. Kawano et al. A 3D packaging technology for 4 Gbit stacked DRAM with 3 Gbps data transfer. In *Proceedings of the IEEE International Electron Devices Meeting*, pp. 1–4, December 2006.
41. M. Puech, J. M. Thevenoud, J. M. Gruffat, N. Launay, N. Arnal, and P. Godinat. DRIE achievements for TSV covering via first and via last strategies. Technical report, ALCATEL Micro Machining Systems.
42. M. Kawano et al. Three-dimensional packaging technology for stacked DRAM with 3-Gb/s data transfer. *IEEE Transactions on Electron Devices*, 55(7):1614–1620, July 2008.
43. D. H. Kim, S. Mukhopadhyay, and S. K. Lim. Through-silicon-via aware interconnect prediction and optimization for 3D stacked ICs. In *Proceedings of the International Workshop on System Level Interconnect Prediction*, pp. 85–92, September 2009.
44. S. M. Satheesh and E. Salman. Effect of TSV fabrication technology on power distribution in 3D ICs. In *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 287–292, May 2013.

45. T. Dao et al. Thermo-mechanical stress characterization of tungsten-fill through-silicon-via. In *Proceedings of the IEEE International Symposium on VLSI Design Automation and Test*, pp. 7–10, April 2010.
46. N. Kumar et al. Robust TSV via-middle and via-reveal process integration accomplished through characterization and management of sources of variation. In *Proceedings of the IEEE Electronic Components and Technology Conference*, pp. 787–793, May–June 2012.
47. J. W. Elam et al. Surface chemistry and film growth during TiN atomic layer deposition using TDMAT and NH_3. *Thin Solid Films*, 436(2):145–156, July 2003.
48. H. Kikuchi et al. Tungsten through-silicon via technology for three-dimensional LSIs. *Japanese Journal of Applied Physics*, 47(4):2801–2806, April 2008.
49. S. Arakalgud. 3D TSV interconnect program—An overview. In *Presented at SEMATECH Symposium Korea*, October 2010.
50. V. F. Pavlidis and G. De Micheli. Power distribution paths in 3-D ICs. In *Proceedings of the IEEE/ACM Great Lakes Symposium on VLSI*, pp. 263–268, May 2009.
51. S. M. Satheesh and E. Salman. Design space exploration for robust power delivery in TSV based 3-D systems-on-chip. In *Proceedings of the IEEE International System-on-Chip Conference*, pp. 307–311, September 2012.
52. H. Wang and E. Salman. Resource allocation methodology for through silicon vias and sleep transistors in 3D ICs. In *Proceedings of the IEEE International Symposium on Quality Electronic Design*, March 2015.
AQ7 53. H. Wang and E. Salman. Decoupling capacitor topologies for TSV-based 3D ICs with power gating. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, in press.
54. H. Wang and E. Salman. Enhancing system-wide power integrity in 3D ICs with power gating. In *Proceedings of the IEEE International Symposium on Quality Electronic Design*, March 2015.
55. S. Natarajan et al. A 32 nm logic technology featuring 2nd-generation high-k + metal-gate transistors, enhanced channel strain and 0.171 μm^2 SRAM cell size in a 291 Mb array. In *Proceedings of the IEEE International Electron Devices Meeting*, pp. 1–3, December 2008.
56. R. Tatikola, M. Chowdhury, R. Chen, and J. Zhao. Simulation study of power delivery performance on flip-chip substrate technologies. In *Proceedings of the IEEE Electronic Components and Technology Conference*, pp. 1862–1865, June 2004.
57. Q. Wu and T. Zhang. Design techniques to facilitate processor power delivery in 3-D processor-DRAM integrated systems. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, 19(9):1655–1666, September 2011.
58. B. Dang et al. 3D chip stack with integrated decoupling capacitors. In *Proceedings of the IEEE International Electronic Components and Technology Conference*, pp. 1–5, June 2009.
59. P. Zhou, K. Sridharan, and S. S. Sapatnekar. Congestion-aware power grid optimization for 3D circuits using MIM and CMOS decoupling capacitors. In *Proceedings of the ACM/IEEE Asia and South Pacific Design Automation Conference*, pp. 179–184, 2009.
60. P. Zhou, K. Sridharan, and S. S. Sapatnekar. Optimizing decoupling capacitors in 3D circuits for power grid integrity. *IEEE Design and Test of Computers*, 26(5):15–25, September 2009.
61. M. Popovich, M. Sotman, A. Kolodny, and E.G. Friedman. Effective radii of on-chip decoupling capacitors. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, 16(7):894–907, July 2008.
62. E. Salman, E.G. Friedman, R.M. Secareanu, and O.L. Hartin. Worst case power/ground noise estimation using an equivalent transition time for resonance. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 56(5):997–1004, May 2009.
63. A. Todri et al. A study of tapered 3-D TSVs for power and thermal integrity. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, 21(2):306–319, February 2013.
64. T. Xu, P. Li, and B. Yan. Decoupling for power gating: Sources of power noise and design strategies. In *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 1002–1007, June 2011.
AQ8 65. North Carolina State University. FreePDK45.
66. P. Ji and E. Salman. Quantifying the effect of local interconnects on on-chip power distribution. *Microelectronics Journal*, 46(3):258–264, March 2015.
67. H. Wang and E. Salman. Power gating methodologies in TSV based 3D integrated circuits. In *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 327–328, May 2013.
68. X. Zhang et al. Characterizing and evaluating voltage noise in multi-core near-threshold processors. In *Proceedings of International Symposium on Low Power Electronics and Design*, pp. 82–87, September 2013.
69. Q.K. Zhu. *Power Distribution Network Design for VLSI*. Wiley, 2004.

70. H. Wei et al. Cooling three-dimensional integrated circuits using power delivery networks. In *Proceedings of the IEEE International Electron Devices Meeting*, pp. 14.2.1–14.2.4, December 2012.
71. E. Salman. Noise coupling due to through silicon vias (TSVs) in 3-D integrated circuits. In *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1411–1414, May 2011.
72. E. Salman, M. H. Asgari, and M. Stanacevic. Signal integrity analysis of a 2-D and 3-D integrated potentiostat for neurotransmitter sensing. In *Proceedings of the IEEE Biomedical Circuits and Systems Conference*, pp. 17–20, November 2011.
73. H. Wang, M. H. Asgari, and E. Salman. Compact model to efficiently characterize TSV-to-transistor noise coupling in 3D ICs. *Integration, the VLSI Journal*, 47(3):296–306, June 2014.
74. H. Wang, M. H. Asgari, and E. Salman. Efficient characterization of TSV-to-transistor noise coupling in 3D ICs. In *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 71–76, May 2013.
75. E. Salman, E. G. Friedman, and R. M. Secareanu. Substrate and ground noise interactions in mixed-signal circuits. In *Proceedings of the IEEE International SoC Conference*, pp. 293–296, September 2006.
76. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin. Identification of dominant noise source and parameter sensitivity for substrate coupling. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, 17(10):1559–1564, October 2009.
77. E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin. Methodology for efficient substrate noise analysis in large scale mixed-signal circuits. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, 17(10):1405–1418, October 2009.
78. Z. Gan, E. Salman, and M. Stanacevic. Figures-of-merit to evaluate the significance of switching noise in analog circuits. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, in press.
79. M. S. Peng and H.-S. Lee. Study of substrate noise and techniques for minimization. *IEEE Journal of Solid-State Circuits*, 39(11):2080–2086, 2004.
80. P. LeDuc et al. Enabling technologies for 3D chip stacking. In *Proceedings of the IEEE International Symposium on VLSI Technology, Systems and Applications*, pp. 76–78, April 2008.
81. H. Chaabouni et al. Investigation on TSV impact on 65 nm CMOS devices and circuits. In *Proceedings of the IEEE International Electron Devices Meeting*, pp. 6–8, December 2010.
82. J. Cho et al. Guard ring effect for through silicon via (TSV) noise coupling reduction. In *Proceedings of the IEEE CPMT Symposium*, pp. 1–4, August 2010.
83. M. Brocard et al. Characterization and modeling of Si-substrate noise induced by RF signal propagating in TSV of 3D-IC stack. In *Proceedings of the IEEE Electronic Components and Technology Conference*, pp. 665–672, 2012.
84. P. Saguet. The 3D transmission-line matrix method: Theory and comparison of the processes. *International Journal of Numerical Modeling: Electronic Networks, Devices and Fields*, 2(4):191–201, 1989.
85. J. Cho et al. Modeling and analysis of through-silicon via (TSV) noise coupling and suppression using a guard ring. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 1(2):220–233, February 2011.
86. M. Stanacevic, K. Murari, A. Rege, G. Cauwenberghs, and N. Thakor. VLSI potenstiostat array with oversampling gain modulation for wide-range neurotransmitter sensing. *IEEE Transactions on Biomedical Circuits and Systems*, 1(1):63–72, March 2007.
87. R. Genov, M. Stanacevic, M. Naware, G. Cauwenberghs, and N. Thakor. 16-Channel integrated potentiostat for distributed neurochemical sensing. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 53(11):2371–2376, November 2006.
88. T. Wichmann and M.R. DeLong. Pathophysiology of Parkinsonian motor abnormalities. *Advances in Neurology*, 60:53–61, 1993.
89. http://www.itrs.net. AQ9
90. G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene. Electrical modeling and characterization of through silicon via for three-dimensional ICs. *IEEE Transactions on Electron Devices*, 57(1):256–262, January 2010.