# Power and Signal Integrity Challenges in 3D Systems-on-Chip

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## ABSTRACT

A significant physical design challenge in both high-performance 3D integrated circuits and low-power 3D systems-on-chip is to guarantee system-wide power and signal integrity. This chapter provides an overview of these challenges with emphasis on through-silicon via (TSV)-based 3D ICs. Different TSV types and their implications to power/signal integrity are first discussed. In the next section, power distribution methodology for a 9-plane processor-memory stack is described. Different decoupling capacitor topologies are also investigated for power-gated 3D ICs. The following section focuses on TSV-to-transistor noise coupling as an important signal integrity issue. A compact model is also proposed to achieve efficient noise coupling analysis in 3D ICs. Finally,
a case study is described to analyze signal integrity in a 3D integrated SoC with application to bioelectronics.

6.1 INTRODUCTION

Three-dimensional (3D) integration is a promising technology that maintains the benefits of miniaturization by utilizing the vertical dimension rather than decreasing the size of the devices in two dimensions [1–7]. Utilizing the vertical dimension not only increases the integration density (thereby reducing cost), but also reduces the length and number of global interconnects. This reduction enhances system performance (due to reduced interconnect delay) while lowering the power consumption (due to reduced switching capacitance). These advantages have attracted significant attention in the past decade to develop high-performance computing systems such as many-core processors with embedded memory, as illustrated in Figure 6.1a [8–11]. 3D technologies alleviate the existing gap between logic blocks and memory units in high-performance microprocessors by utilizing vertically embedded dynamic random access memory (DRAM), thereby significantly increasing the memory bandwidth and reducing memory access time.

In addition to facilitating high-performance computing systems, 3D technologies provide a unique opportunity for heterogeneous integration of diverse functions onto a monolithic chip, as depicted in Figure 6.1b. Heterogeneous integration expands the application domain of 3D-integrated circuits from high-performance computing to relatively lower power systems-on-chips (SoCs) consisting of, for example, sensors, analog interface circuit, memory, digital processing blocks, and RF wireless transmission circuitry. The ability to merge disparate circuits and technologies is essential for multifunctional systems since each plane can be optimized according to the requirements of that particular function. This advantage also supports the concept of More-than-Moore that targets the scaling of a system by incorporating nondigital portions into the same monolithic IC [12,13]. 3D integration of diverse functions is expected to enable exciting opportunities in a variety of fields including energy-efficient mobile computing, health care, and environmental control. For example, The Semiconductors Electronics Division of the National Institute of Standards and Technology

![Figure 6.1](image-url)
Power and Signal Integrity Challenges in 3D Systems-on-Chip

(NIST) identifies 3D technology as one of the fundamental enabling technologies for “extremely scaled intelligent bio-electronic micro-systems for in vivo operations” [14].

A significant circuit- and physical-level challenge in both high-performance 3D computing systems and relatively low-power 3D SoCs is to ensure system-wide power and signal integrity, as explored in this chapter. Power integrity refers to the quality of the power supply voltage delivered to each transistor within a 3D stack, whereas signal integrity refers to the quality of both analog and high-speed digital data signals that are subject to different types of noise. These issues are investigated in the following sections with particular emphasis on wafer-level 3D integration technologies where multiple wafers are thinned, aligned, and vertically bonded. Communication among the dies is achieved by high-density Through-Silicon-Vias (TSVs). Global interconnect length is therefore reduced, lowering the overall power dissipation and latency. TSVs achieve significantly higher interconnection density among the planes of a 3D stack as compared to other vertical interconnects such as through hole vias in a system-in-package (SiP) [3].

The rest of the chapter is organized as follows. The primary characteristics of the three TSV fabrication technologies are summarized in Section 6.2. The issues of power integrity and signal integrity in TSV-based 3D systems are discussed in Sections 6.3 and 6.4, respectively. The chapter is concluded in Section 6.5.

6.2 TSV TECHNOLOGIES AND IMPLICATIONS TO POWER/SIGNAL INTEGRITY

As illustrated in Figure 6.2, existing efforts in 3D-ICs can be broadly classified under three primary categories: (1) transistor-level 3D integration, (2) system-in-package (SiP) and system-on-package (SoP), and (3) wafer-level TSV-based 3D integration. In transistor-level 3D integration [15], active devices within a logic gate are fabricated on different layers, but only a single substrate exists. The upper layer devices are formed on a recrystallized silicon obtained by laser heating or rapid thermal annealing [16]. Polysilicon and single crystal silicon films are also used to host upper layer transistors. Despite the highest density of vertical interconnects, transistor-level 3D integration suffers significantly from thermal challenges and high-defect density [17]. The upper layer silicon should be formed with sufficiently low temperatures to not damage the metal interconnects and devices at the bottom layers. Due to this limitation, the existing research in transistor-level 3D integration primarily focuses on material development and novel fabrication methods.
SiP- and SoP-based 3D integration [18–20] are relatively more mature, and commonly encountered in commercial electronic devices where multiple dies are packaged by utilizing (1) wire bonding, (2) low-density vertical interconnects, and (3) area–array-based C4 (controlled collapse chip connection) bumps. Comprising a primary practical concern, the length of these interconnects are typically in the range of several millimeters, significantly degrading the reliability and packaging efficiency in addition to preventing dense integration and causing high power consumption.

In wafer-level 3D integration [21–23], as depicted in Figure 6.1, entire wafers are bonded to produce a 3D stack where TSVs are utilized for interplane communication. This method not only achieves higher interconnect density, but also lower cost per connection due to greater alignment accuracy and enhanced surface planarization [24]. Furthermore, greater flexibility is provided to implement in-stack passive devices that are highly important in analog and RF functions. Thus, wafer-level 3D integration is considered to be one of the most promising approaches to realize dense and heterogeneous ICs in the nanoscale era [25–27].

Despite the ongoing research to further optimize 3D fabrication steps, no fundamental limitation exists. For example, alignment accuracy of one micrometer has already been demonstrated [26]. Multiple bonding techniques have also been developed such as adhesive [28,29], oxide [30], and metal bonding [31]. The wafer thinning capability varies from hundreds of nanometers to several hundred micrometers, depending upon whether bulk silicon or silicon-on-insulator is utilized [32,33]. Finally, several distinct TSV fabrication methods exist depending upon when the TSVs are formed [34]. These methods are (1) via-first [35], (2) via-middle [36,37], and (3) via-last TSVs [38]. Note that each TSV type exhibits significantly different electrical characteristics, and therefore require distinct design guidelines, as described in the following subsections.

6.2.1 Via-First TSV Technology

In a via-first method, TSVs are fabricated before the transistors are patterned in silicon, that is, prior to front-end-of-line (FEOL) [35,39–41]. Thus, TSVs fabricated with the via-first technique do not pass through the metallization layers, as depicted in Figure 6.3a. The TSV of a plane is connected between the first metal layer of the current plane and the top most metal layer of the previous plane. Polysilicon is typically used as the filling material due to its ability to withstand high temperatures [35,39–41]. Via-first TSVs are less sensitive to contamination since both the filling and substrate materials are the same [42]. The physical dimensions of via-first TSVs are smaller than via-last TSVs [43]. Via-first TSVs, however, are highly resistive and have a lower filling throughput due to the use of polysilicon as the filling material [42,44].

6.2.2 Via-Middle TSV Technology

In a via-middle process, TSVs are fabricated after FEOL, but before the metallization layers are patterned, that is, prior to back-end-of-line (BEOL) [36–38,42,45]. Similar to via-first TSVs, via-middle TSVs connect the first metal layer of a plane with the last metal layer of the previous plane, as illustrated in Figure 6.3b. Since the high-temperature FEOL process precedes TSV fabrication steps, via-middle process permits the use of tungsten (or possibly copper) as the filling material, which is significantly less resistive as compared to doped polysilicon. Tungsten can be used as the filling material due to low thermal expansion coefficient (4.6 ppm/K) as compared to copper (17 ppm/K) [37]. A material with low sensitivity to temperature is required since the TSV fabrication step is followed by a moderately high temperature BEOL process. Note however that copper-filled via-middle TSVs have also been demonstrated [46].

Via-middle TSVs require a relatively large (12:1 or higher) aspect ratio [36–38,45]. Thus, the width of via-middle TSVs is comparable to the width of via-first TSVs, whereas the height is comparable to via-last TSVs. This characteristic produces a relatively high inductive behavior. Also note that the fabrication process of via-middle TSVs is relatively more challenging. For example,
A conformal barrier process is required for the tungsten to adhere to the dielectric in the cavity. A 20-nm titanium nitride (TiN) layer is typically deposited using metal organic chemical vapor deposition (MOCVD) [36]. TiN is a hard, dense, refractory material with sufficiently low electrical resistivity (22 $\mu\Omega$ cm) [47].

Another challenge is the high level of stress during the deposition of the oxide layer, which is exacerbated when a conformal layer is required. This challenge is partially negated with the use of a tapered TSV structure that progressively shrinks in size [36,37]. This structure is illustrated in Figure 6.3b. Other challenges include sensitivity to contamination and the requirement to maintain the temperature within 500°C [42]. Novel deposition techniques such as atomic layer deposition (ALD) and time-modulated deposition alleviate some of these issues [36,48].

From the design perspective, via-middle technology is an interesting compromise between a highly resistive via-first and a low resistive, but highly inductive via-last TSVs. Furthermore, similar to via-first TSVs, via-middle TSVs do not cause metal routing blockages. The Semiconductor Manufacturing Technology (SEMATECH) consortium has chosen via-middle TSVs as a primary focus area [49].

### 6.2.3 Via-Last TSV Technology

In the via-last approach, TSV formation occurs after the metallization layers are fabricated, that is, after BEOL [39,42,43]. Thus, as opposed to via-first and via-middle TSVs, via-last TSVs pass through the metal layers, causing metal routing blockages, as depicted in Figure 6.3c [43,50]. A lower resistivity filling material such as copper is used since high temperature FEOL and BEOL processes are performed before the via formation [39,42]. The use of copper as a filling material
makes the process sensitive to both temperature (should be maintained less than 230°C) and contamination [42]. Despite exhibiting relatively low resistance, the inductive characteristics of via-last TSVs are relatively more significant than via-first TSVs due to greater dimensions [43]. The physical connection between the TSV and metal layers is typically achieved at the top most metal layer. Note that process technologies to manufacture TSVs are currently under investigation based on recent research results on wafer thinning, alignment accuracy, mechanical stress, and bonding methods. Thus, TSV geometries for a certain TSV type may vary depending upon the foundry.

6.3 SYSTEM-WIDE 3D POWER INTEGRITY

A significant circuit- and physical-level challenge in a TSV-based 3D-IC is to design a robust power distribution network that achieves reliable power delivery to each die. Maintaining the power network impedance smaller than a target impedance (i.e. satisfying the power supply noise) is a difficult task due to reduced operating voltages, increased current magnitudes, and the existence of multiple dies and TSVs. A conservatively large number of power/ground TSVs can significantly increase the area overhead in addition to producing highly inductive characteristics due to a smaller damping factor.

A case study is described in Section 6.3.1 where the power integrity characteristics of a nine-plane processor-DRAM system are investigated. A design space is developed to satisfy power supply noise while minimizing the physical area consumed by the TSVs and decoupling capacitors [51].

3D-ICs are expected to be heavily power-gated due to the importance of subthreshold leakage current in nanoscale bulk CMOS technologies. Furthermore, with heterogeneous integration, the switching activity factor of different blocks/planes is expected to significantly vary, emphasizing the need for power gating. Power gating, however, significantly affects the system-wide power integrity of a 3D-IC, particularly in the presence of decoupling capacitors [52,53]. Various decoupling capacitor topologies are discussed in Section 6.3.2 to enhance power integrity in the power-gated 3D-ICs. Advantages of a reconfigurable decoupling capacitor topology are emphasized [54].

6.3.1 CASE STUDY: POWER DISTRIBUTION IN A NINE-PLANE 3D PROCESSOR-DRAM STACK

6.3.1.1 Architecture

A 3D system in a 32-nm CMOS technology consisting of eight memory planes and one plane for the processor is considered. Each plane contains nine metal layers where the metal thickness and aspect ratio are determined according to 32-nm technology parameters [55]. The power supply voltage is equal to 1 V. Each plane occupies an area of 120 mm², excluding the TSVs and the intentional decoupling capacitance. The system has 1 GB of DRAM spread uniformly across eight memory planes. Each memory plane has 1 gigabit (GB) DRAM divided into 32 modules of equal size, where each module has 32 MB memory. Similarly, the processor plane is also divided into 32 modules. Each of these modules consume an area of 1500 × 2500 μm². This topology is depicted in Figure 6.4. For via-first and via-middle technologies, the TSVs are placed beneath the active circuit, as illustrated in Figure 6.4a whereas in via-last technology, the power and ground TSVs are distributed on both sides of each module, as depicted in Figure 6.4b.

6.3.1.2 Power Distribution Network Model

An equivalent electrical model corresponding to the power distribution network of one of the 32 modules is illustrated in Figure 6.5. This model consists of the TSVs (R_{TSV}, C_{TSV}, and L_{TSV}), substrate (R_s and C_s), power distribution network within a plane (R_{Network}, R_{Vertical}, and R_{ML}), switching load circuit, and decoupling capacitance C_{decap}. Note that in addition to these on-chip impedances, the parasitic package resistance and inductance are, respectively, 3 mΩ and 100 pH at both the power and ground supplies, assuming an organic flip-chip package [56]. The primary characteristics of the three TSV technologies are listed in Table 6.1.
Power and Signal Integrity Challenges in 3D Systems-on-Chip

FIGURE 6.4 3D processor-memory stack: (a) via-first and via-middle TSVs and (b) via-last TSVs.

FIGURE 6.5 Equivalent power distribution network of each module within a plane.
The DRAM consumes 3 W, uniformly distributed across the eight stacks [57]. Alternatively, the processor consumes 90 W. Thirty percent of the overall power is due to static power dissipation whereas the remaining portion is due to dynamic power consumption [57]. A triangular current waveform is assumed with 400 ps period, 100 ps rise time, and 150 ps fall time. The DC current and peak current are determined based on, respectively, the static and dynamic power consumption.

6.3.1.3 Results

In 3D power distribution networks, it is important to determine the appropriate number of TSVs and decoupling capacitance that satisfy the constraint on power supply noise. From this design space, a valid pair that minimizes the physical area overhead is chosen. Note that this specific design point is dependent upon the implementation of the decoupling capacitance. Three methods are considered: (1) metal-oxide-semiconductor (MOS) capacitance in a 32-nm technology node with a capacitance density of 39.35 fF/μm² as determined from the equivalent oxide thickness (EOT) of the technology [55], (2) deep trench capacitance with a density of 140 fF/μm² [58], and metal-insulator-metal (MIM) capacitance with a density of 8 fF/μm² [59,60].

As an illustrative example, results for via-middle TSVs (filled with tungsten) are shown. The peak noise surface as a function of decoupling capacitance and number of TSVs is plotted in Figure 6.6a. As illustrated in this figure, the power supply noise monotonically decreases as the number of TSVs and decoupling capacitance increase. The noise contour at 100 mV (power supply noise constraint) is illustrated in Figure 6.6b. Any point on (and above) this curve satisfies the noise constraint. The physical area overhead for each of these points is depicted in Figure 6.7 for three different decoupling capacitance densities, as mentioned above. A specific design point exists where the physical area overhead is minimized. For example, if MOS capacitance is used, this design point is at 620 TSVs and 0.6 nF of decoupling capacitance.

A similar procedure is followed for via-first and via-last TSVs. The design points that minimize the physical area overhead while satisfying the power supply noise constraint are summarized in Table 6.2. The following important conclusions can be made based on these results:

- Highly resistive via-first TSVs (filled with polysilicon) can be used to deliver power at the expense of approximately 9% area overhead as compared to less than 2% area overhead in via-middle (filled with tungsten) and via-last (filled with copper) technologies.
Despite the higher area requirement, a power distribution network with via-first TSVs is typically overdamped and the issue of resonance is alleviated.

For via-middle and via-last TSV technologies, the impedance at the resonant frequency should be sufficiently small. This issue is exacerbated for a via-last based power distribution network since the TSV resistance is significantly lower, and therefore the network is typically underdamped.

### 6.3.2 Decoupling Capacitors for Power-Gated 3D-ICs

In traditional topologies, the decoupling capacitance of a power-gated block (or plane) cannot provide charge to neighboring planes since these capacitors are typically connected to a virtual power...
Placing the decoupling capacitors sufficiently close to the switching load is helpful in reducing the power supply noise [61,62]. However, if the block or plane is power-gated, those capacitors that provide charge to the block (or plane) are disconnected from the global power network, making these capacitors ineffective for the neighboring planes. Since system-wide power integrity is a critical challenge in 3D-ICs, effective use of intentional decoupling capacitance is crucial, even when power gating is adopted.

**FIGURE 6.7** Area overhead in via-middle technology. Note that each point on the curve satisfies the target power supply noise.

**TABLE 6.2**
Valid Design Points that Satisfy the Peak Power Supply Noise While Minimizing the Area Overhead for each TSV Technology

<table>
<thead>
<tr>
<th>Cap Type</th>
<th>Cap Density (fF/μm²)</th>
<th>Area Overhead (%)</th>
<th>Number of TSVs</th>
<th>Decoupling Capacitance (nF)</th>
<th>Power Loss (%)</th>
<th>Peak Noise (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Via-First</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOS-C</td>
<td>39.35</td>
<td>9.06</td>
<td>2750</td>
<td>2.7</td>
<td>8.3</td>
<td>33.42</td>
</tr>
<tr>
<td>MIM</td>
<td>8</td>
<td>11.83</td>
<td>3437</td>
<td>0.8</td>
<td>7.3</td>
<td>23.5</td>
</tr>
<tr>
<td><strong>Via-Middle</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOS-C</td>
<td>39.35</td>
<td>1.96</td>
<td>620</td>
<td>0.60</td>
<td>6.7</td>
<td>63.56</td>
</tr>
<tr>
<td>DT</td>
<td>140</td>
<td>1.68</td>
<td>484</td>
<td>2</td>
<td>7.6</td>
<td>45.13</td>
</tr>
<tr>
<td>MIM</td>
<td>8</td>
<td>3.01</td>
<td>631</td>
<td>0.4</td>
<td>6.6</td>
<td>67.5</td>
</tr>
<tr>
<td><strong>Via-Last</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOS-C</td>
<td>39.35</td>
<td>1.54</td>
<td>76</td>
<td>0.385</td>
<td>4</td>
<td>134.72</td>
</tr>
<tr>
<td>DT</td>
<td>140</td>
<td>1.21</td>
<td>30</td>
<td>3.74</td>
<td>4.9</td>
<td>134.67</td>
</tr>
<tr>
<td>MIM</td>
<td>8</td>
<td>2.56</td>
<td>76</td>
<td>0.385</td>
<td>4</td>
<td>134.72</td>
</tr>
</tbody>
</table>

DT refers to deep trench.
It has been observed that the effective range of a decoupling capacitor exceeds single plane in 3D-ICs with low-resistance TSVs [63]. This phenomenon is important particularly when block- or plane-level power gating is performed due to significant decoupling capacitance that cannot provide charge to the remaining, active planes. Thus, when one or more number of planes is power-gated, power supply noise in one of the remaining active planes may increase and violate the constraint despite a reduction in the overall switching current drawn from the power supply. It is therefore highly critical to ensure that the decoupling capacitors within the power-gated planes are not ineffective for the remaining planes. A reconfigurable decoupling capacitor topology is described in the following section to alleviate this issue [53].

6.3.2.1 Reconfigurable Topology

In the reconfigurable topology, two switches are used to form a configurable decoupling capacitor, as conceptually illustrated in Figure 6.8 [64]. If a certain plane is active, the decoupling capacitors on that plane are connected to the virtual \( V_{DD} \) grid through switch 2, thereby reducing the power supply noise on that plane. Alternatively, if the plane is power-gated (sleep transistors are turned off), the decoupling capacitors are connected to the global \( V_{DD} \) grid, bypassing the sleep transistors. Thus, even if the plane is power-gated, the decoupling capacitors are effective for the remaining planes. The overhead of this topology includes the reconfigurable switches, metal resources required to route the related control signals, and a possible increase in overall power consumption depending upon how the capacitors are implemented, as discussed in the following section.

6.3.2.2 Evaluation Setup

A power distribution network for a three-plane 3D-IC with via-last TSVs is developed, as conceptually illustrated in Figure 6.9 for a single plane [53]. A 45-nm CMOS technology with 10 available metal layers in each plane is adopted [65]. A portion of the power network with an area of 1 mm × 1 mm is analyzed. Each plane consists of a global power network, virtual power network, distributed PMOS sleep transistors, distributed decoupling capacitance (implemented as MOS capacitors), and distributed switching load circuit consisting of inverter gates, as depicted in Figure 6.9. Top two metal layers (9 and 10) on each plane are dedicated to global power distribution network with an interdigitated grid of 11 × 11. Metal layers 8 and 7 are used as the virtual power network represented by an interdigitated grid of 21 × 21 [66]. Power gating is achieved using a distributed method where the sleep transistors that control a plane are placed within that plane [67]. Note that the top plane also consists of C4 bumps to connect the on-chip grid with the flip-chip substrate.
Similar to [68], inverter pairs with varying number and size are used to model the switching load circuit. The overall area is divided into 30 sub-areas and a switching circuit is connected to each sub-area to consider the spatial heterogeneity of the current loads. The spatial load current distribution and power densities are based on [69] where the peak power density reaches 40W/cm², comparable to the power density in modern processors [70]. All of the decoupling capacitors are implemented as MOS capacitors in the 45-nm technology with an oxide thickness of 1 nm [65].

6.3.2.3 Results

The efficacy of the reconfigurable decoupling capacitor placement topology is evaluated by comparing the methodology with the traditional topology where the capacitors are connected to a virtual power grid. Both power supply noise and power gating noise are analyzed. Three power gating scenarios are considered:

- **Scenario 1**: All of the three planes are active, representing the greatest workload.
- **Scenario 2**: The top and bottom planes are active, while the middle plane is power-gated.
- **Scenario 3**: Only the bottom plane is active, while the middle and top planes are power-gated.

Power supply noise results are listed in Table 6.3 for each scenario. As listed in this table, when some of the planes are power-gated (scenarios 2 and 3), the reconfigurable topology achieves less power...
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Supply noise by exploiting the capacitors of the power-gated plane(s). For example, in scenario 3 where two planes are power-gated, the reduction in peak noise is approximately 27%, whereas the reduction in RMS noise is approximately 46%. Note that in the traditional topology, the peak noise in scenario 3 exceeds 50 mV despite the reduction in overall switching current due to power gating. This characteristic is due to less decoupling in the power network since the decoupling capacitors in the power-gated planes cannot behave as charge reservoirs for the remaining, active planes. This observation justifies the need for reconfigurable capacitors. Transient behavior of voltage noise at a specific node within the bottom plane is also depicted in Figure 6.10 for scenario 3, demonstrating the reduction in peak and RMS noise.

To investigate power gating noise, the power-gated middle plane transitions from inactive to active state in scenarios 2 and 3, and the voltage fluctuation due to in-rush current during the wake-up process is analyzed. Peak power gating noise is observed at the bottom plane. Results are listed in Table 6.4. The reconfigurable topology achieves more than 80% reduction in peak and RMS power gating noise. In traditional topology, a significant amount of in-rush current flows not only for the activated circuit, but also to charge the associated decoupling capacitors. Alternatively, in the reconfigurable topology, the decoupling capacitors are connected to the global VDD grid when the plane is power-gated. Thus, even if the plane is power-gated, these capacitors remain charged (significantly reducing in-rush current) and can behave as charge reservoir once the plane transitions to active state. The transient behavior of the power gating noise is illustrated in Figure 6.11 for scenario 3 where the transition happens at 1 ns.

### TABLE 6.3

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<td>Mid</td>
<td>Btm</td>
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<td>On</td>
<td>On</td>
</tr>
<tr>
<td>Scenario 2</td>
<td>On</td>
<td>Off</td>
</tr>
<tr>
<td>Scenario 3</td>
<td>Off</td>
<td>Off</td>
</tr>
</tbody>
</table>

**FIGURE 6.10** Transient behavior of voltage noise at a specific node within the bottom plane for each topology for scenario 3.
In the reconfigurable topology, the physical area overhead increases by only 1.55% due to recon-
figurable switches and higher decoupling capacitance required to compensate for the shielding
effect of the reconfigurable switches. This slight increase in the physical area significantly enhances
power integrity when one or more planes are power-gated, as described above.

To quantify the power overhead of the reconfigurable topology, both topologies are simulated
for each scenario and the overall average power consumption is determined. All of the decoupling
 capacitors are implemented as MOS capacitors to consider MOS-C leakage. It is observed that the
maximum power (drawn in scenario 1) increases by only 1.36% due to increased capacitance and
switches. This power overhead can be further reduced if low leakage decoupling capacitor imple-
mentations are adopted such as metal-insulator-metal (MIM) capacitors.

### 6.4 SYSTEM-WIDE 3D SIGNAL INTEGRITY

In addition to traditional noise coupling and propagation mechanisms such as crosstalk, power
supply noise, and substrate coupling, 3D-ICs suffer from TSV-induced noise coupling [71–73].
Specifically, during a signal transition within a TSV, noise couples from TSV into the substrate due
to both dielectric and depletion capacitances. The coupling noise propagates throughout the sub-
strate and affects the reliability of nearby transistors [74]. This issue is exacerbated for TSVs that
carry signals with high switching activity factors and fast transitions such as clock signals.

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Power Status</th>
<th>Traditional Peak</th>
<th>Traditional RMS</th>
<th>Reconfigurable Peak</th>
<th>Reconfigurable RMS</th>
<th>Peak Redtn. (%)</th>
<th>RMS Redtn. (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scenario 1</td>
<td>On On On</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Scenario 2</td>
<td>On Off On</td>
<td>90.73</td>
<td>72.83</td>
<td>15.55</td>
<td>82.8</td>
<td>11.46</td>
<td>84.2</td>
</tr>
<tr>
<td>Scenario 3</td>
<td>Off Off On</td>
<td>103.2</td>
<td>78.76</td>
<td>15.66</td>
<td>84.8</td>
<td>11.57</td>
<td>85.3</td>
</tr>
</tbody>
</table>

FIGURE 6.11 Transient behavior of power gating noise at a specific node within the bottom plane for each
topology for scenario 3.
Analog/RF blocks and memory cells are among the most sensitive circuits to substrate noise coupling [75–78]. For example, in [79], experimental data demonstrate that the signal-to-noise-plus-distortion ratio (SNDR) of a delta-sigma modulator is reduced by more than 20 dB due to substrate noise. Note that in heterogeneous 3D systems, the front-end circuitry consisting of analog/RF blocks is typically located at the top plane (closer to the I/O pads) to reduce the overall impedance between the pads and analog inputs. In this floorplan, TSVs are required to transmit the digital signals (including the clock signal) to the data processing plane. Thus, TSV-induced noise becomes an important issue for the reliability of the analog/RF blocks. Digital transistors are also affected by TSV-induced noise if the physical distance between the TSV and device is sufficiently short [80]. TSV-induced noise changes the drain current characteristics of both an on and off transistor, as observed in [81].

A methodology is described in Section 6.4.1 to efficiently analyze TSV-to-transistor noise coupling in 3D-ICs. A case study is presented in Section 6.4.2 to better understand noise propagation paths within a 3D environment.

### 6.4.1 Efficient Analysis of TSV-to-Transistor Noise Coupling

To characterize TSV-induced noise coupling, the physical structure depicted in Figure 6.12 is used. This structure consists of a noise injector (TSV), noise transmitter (substrate), and a noise receptor (victim transistor). Substrate contacts are also included to bias the substrate. Note that the number and placement of substrate contacts between the TSV and victim transistor play an important role in the noise coupling analysis. To analyze this physical structure, several approaches have been adopted such as using an electromagnetic field solver, device simulator, and a highly distributed model using 3D transmission line matrix (TLM) method [82–84], as described in the following subsection.

#### 6.4.1.1 Distributed Model

In the distributed model, the physical structure is discretized into unit cells (for both TSV and substrate) and each unit cell is modeled with lumped parasitic impedances. Both the measurement and 3D field solver results demonstrate that the 3D-TLM model can accurately model the 3D physical structure including a TSV, substrate contact, and victim transistor [82,85]. Despite the reasonable accuracy achieved by the distributed model, the computational complexity is significantly high, particularly when the dimensions of the unit cells are small. This issue is exacerbated as the distance between the TSV and victim transistor increases. Furthermore, the number and location of the substrate contacts play an important role in characterizing the TSV safe zone. Re-analysis of the distributed structure when these characteristics change is computationally prohibitive. Therefore, a compact model is needed to alleviate these limitations, as described in the following section. This highly distributed model is used as a reference to validate the compact model and closed-form expressions.
6.4.1.2 Compact Model

A two-port, linear time-invariant network can be generally characterized with four admittances: $Y_{11}(j\omega)$, $Y_{12}(j\omega)$, $Y_{21}(j\omega)$, and $Y_{22}(j\omega)$. Utilizing this characteristic, the proposed compact model consists of a single TSV cell and an equivalent two-port $\pi$ network to model noise propagation, as depicted in Figure 6.13 [73]. Each electrical element within the $\pi$ network consists of a parallel $RC$ circuit, producing an admittance $(1/R) + j\omega C$. These admittances can be obtained from the distributed mesh (based on 3D-TLM method), as described in the previous section. Specifically, the four $Y(j\omega)$ parameters of the distributed mesh are obtained through an AC analysis. The resistances and capacitances within the $\pi$ network are determined such that the four $Y(j\omega)$ parameters of the compact $\pi$ network are equal to the respective $Y(j\omega)$ parameters of the distributed mesh. According to this procedure, the admittances within the $\pi$ network $Y_{\text{sub}}(j\omega)$, $Y_{\text{gnd}}^{1}(j\omega)$, and $Y_{\text{gnd}}^{2}(j\omega)$ are determined as follows:

- $Y_{\text{sub}}(j\omega) = (1/R_{\text{sub}}) + j\omega C_{\text{sub}} = Y_{21}(j\omega)$: represents the equivalent substrate admittance between the TSV and victim transistor.
- $Y_{\text{gnd}}^{1}(j\omega) = (1/R_{\text{gnd}}^{1}) + j\omega C_{\text{gnd}}^{1} = Y_{11}(j\omega) - Y_{21}(j\omega)$: represents the equivalent substrate admittance between the TSV and ground node.
- $Y_{\text{gnd}}^{2}(j\omega) = (1/R_{\text{gnd}}^{2}) + j\omega C_{\text{gnd}}^{2} = Y_{22}(j\omega) - Y_{11}(j\omega)$: represents the equivalent substrate admittance between the victim node and ground node.

In the next step, each resistive and capacitive element within each $Y(j\omega)$ of the $\pi$ network are characterized as a function of $d_{1}$ and $d_{2}$, where $d_{1}$ and $d_{2}$ are depicted in Figure 6.14. Via-first and via-last TSVs are separately analyzed. To evaluate the dependencies of $R$ and $C$ on $d_{1}$ and $d_{2}$, AC analyses of the distributed mesh (based on 3D-TLM) described in the previous section are performed with different values of $d_{1}$ and $d_{2}$. The data obtained in this step are used to generate a 3D surface for each resistance and capacitance within $Y_{\text{sub}}(j\omega)$, $Y_{\text{gnd}}^{1}(j\omega)$, and $Y_{\text{gnd}}^{2}(j\omega)$. This surface is approximated with a logarithmic function using a 3D least square regression analysis. The logarithmic function $F(d_{1}, d_{2})$ used to approximate the admittances of the $\pi$ network as a function of the physical distances $d_{1}$ and $d_{2}$ is

\[
F(d_{1}, d_{2}) = A + Bd_{1} + Cd_{2} + D \ln d_{2} + E \ln d_{1},
\]  

(6.1)

where $A$, $B$, $C$, $D$, and $E$ are fitting coefficients. These fitting coefficients are determined such that the resistor/capacitor value obtained from this expression reasonably approximates the actual
resistor/capacitor value (in the compact $\pi$ model) that is obtained from the highly distributed 3D TLM model. Note that both the resistance (in k$\Omega$) and capacitance (in attoFarads) of each $Y_{ij}(j\omega)$ within the $\pi$ network are represented by the function $F$. Also note that the distances $d_1$ and $d_2$ are in $\mu$m. Since the $\pi$ network has three admittances each consisting of a parallel $RC$ circuit, six logarithmic functions are developed for via-first and via-last TSVs, producing a total of 12 functions. The fitting coefficients for each function are listed in Table 6.5.

The function $F$ is given by Equation 6.1. All resistances are in k$\Omega$ and all capacitances are in attoFarads.
6.4.1.3 Results and Design Guidelines

The compact π model contains only 11 number of elements for both via-first and via-last TSVs where each element is represented by Equation 6.1 with five fitting coefficients. Alternatively, the number of circuit elements in the distributed model (based on 3D-TLM) can exceed a million when the unit cell dimension is 1 μm.

According to Table 6.5, maximum average error is slightly over 10% for certain resistances and capacitances. This error, however, does not significantly affect the electrical characteristics (and noise estimation at the victim node) since the maximum error occurs at the extreme cases when the resistance is sufficiently large and capacitance is sufficiently small. Also note that the average error over via-first and via-last TSVs is approximately 6%.

The compact model illustrated in Figure 6.13, Equation 6.1, and fitting parameters listed in Table 6.5 can be used to investigate the effect of various design and fabrication parameters such as placement of substrate contacts and TSV type. As an example, the effect of increasing \( d_1 \) (placing the victim farther from the TSV) on peak noise is investigated for both via-first and via-last TSVs. The results are shown in Figure 6.15. According to this figure, placing the victim transistor farther from the switching TSV is an effective method for via-first TSVs. Alternatively, for via-last TSVs, the noise exhibits low sensitivity to the distance between TSV and victim transistor. This phenomenon can be explained by longer height (therefore smaller substrate resistances) and larger diameter (therefore larger capacitances) of via-last TSVs.

6.4.2 Case Study: SI Analysis of a 3D-Integrated SoC

The primary objective of this study is to evaluate the signal integrity characteristics of a 3D-integrated mixed-signal circuit and compare the results with a 2D implementation. It is typically assumed that the noise performance of a 3D circuit is superior than a 2D system since the aggressor and victim blocks can be placed on separate planes, thereby enhancing signal isolation [5,7]. The validity of this assumption is evaluated by developing a comprehensive electrical model for both 2D and 3D versions of the same circuit. The circuit functionality, architecture, and signal integrity modeling approach are described in the following subsections.

![Figure 6.15](image-url)

**FIGURE 6.15** TSV-induced switching noise at the victim node as a function of \( d_1 \) at constant \( d_2 \) for via-first and via-last TSVs.
6.4.2.1 Potentiostat Architecture

A 16-channel VLSI potentiostat chip, designed and fabricated in 0.5 μm CMOS technology, simultaneously records neurotransmitter levels from multiple neurons [86,87]. The detection of the neurotransmitters is critical for neural pathways and the etiology of neurological diseases like epilepsy and stroke [88]. High sensitivity and wide dynamic range are critical design objectives since the measured currents are in the picoampere range. Thus, an accurate evaluation of signal integrity is critical.

To manage computational complexity, the proposed signal integrity analysis focuses on a single channel that consists of a first-order delta-sigma modulator, counter for decimation, and shift register, as depicted in Figure 6.16 [86,87]. Delta-sigma modulator consists of a current integrator, comparator, and switched-current 1-bit D/A converter in the feedback loop. The counter is the primary aggressor whereas the sense amplifier within the current integrator is identified as one of the primary victim blocks. The switching noise that couples from the counter to the sense amplifier is analyzed for different scenarios, as described in the following subsections.

6.4.2.2 3D Signal Integrity Modeling

Highly distributed 3D electrical models based on TLM method (as described in Section 6.4.1) are utilized to analyze signal integrity. Both the substrate and TSVs are discretized using unit cells consisting of RLC impedances, and an entire electrical model for a single channel of a neurotransmitter chip is generated in both 2D and 3D technologies.

In the 3D-integrated potentiostat, the aggressor (counter) and victim (delta-sigma modulator) are placed on separate planes. Specifically, the top plane (closer to the I/O pads) is dedicated to the victim block whereas the bottom plane (closer to the heat sink) is dedicated to the aggressor block. A conceptual representation of the electrical model is depicted in Figure 6.17. The bulk nodes within the schematic are connected to the corresponding nodes on the substrate. Two separate substrates exist: (1) substrate of the bottom plane where the bulks of the counter are connected, and (2) substrate of the upper plane where the bulks of the delta-sigma modulator are connected. As depicted in Figure 6.17, a face-to-face bonding technology is assumed with via-first fabrication technique. In this technique, the TSVs go through the upper (analog) substrate and reaches the metal layers of the analog plane. The topmost metal layer of the analog plane is connected to the topmost metal layer of the digital plane using bumps. Since only a single channel of the device is modeled, eight TSVs are required: five for the clock signals (each at 1 MHz), two for power supply voltage (3 V), and one for data signal. Signal integrity results are described in the following subsection.

6.4.2.3 Results

A transient analysis is performed and the noise at the bulk of the victim device is observed. Peak noise is illustrated in Figure 6.18 for two different cases: (1) nonideal TSVs with practical capacitance values, (2) ideal TSVs with zero capacitance value. Note that the result of the 2D analysis is also included for comparison. As depicted in this figure, the 3D system with practical TSVs, despite
having separate substrates for aggressor and victim, exhibit significantly higher noise (positive peak noise exceeds 6 mV) than the 2D system.

To determine the primary noise source, the TSV capacitance $C_{TSV}$ of the clock TSVs is removed, producing an ideal clock TSV with no coupling into the substrate. In this case, the peak noise is significantly reduced (to approximately 2 mV) and is smaller than the 2D system. Thus, in a 3D system, significant noise couples into the substrate through clock TSVs. The same conclusion is validated by observing the RMS noise over 10 μs, as listed in Table 6.6 for all of the cases. The RMS noise is reduced by more than 50% only if the TSVs are ideal, that is, TSV-to-substrate noise coupling is prevented.

For applications such as the neurotransmitter sensing as described in this section, the top plane of a 3D-IC should be dedicated to the highly sensitive frontend circuits due to physical proximity to the pads. In this case, however, clock TSVs with short rise times inject significant noise into the substrate of the analog plane since these signals need to reach the bottom plane where the digital circuit is placed. This coupling mechanism is due to the TSV-to-substrate capacitance $C_{TSV}$ of the TSVs. Thus, the distance between an aggressor TSV and a victim device should be carefully considered. Efficient and 3D-specific signal isolation strategies should also be developed.
6.5 SUMMARY AND CONCLUSIONS

TSV-based 3D technologies facilitate higher and heterogeneous integration, enable enhanced performance while reducing the overall power consumption. Despite various challenges at the fabrication level (such as developing low cost and high aspect ratio vertical vias and reliable bonding technologies at lower temperatures), no fundamental limitations exist. A similar argument applies to the design process where significant research has been conducted during the past decade. TSV-based 3D-ICs enable exciting opportunities not only for high-performance computing systems, but also for low-power SoCs with application to mobile computing, life sciences, and environment control.

This chapter has focused on two important issues encountered during the physical design process of 3D SoCs: power and signal integrity. An overview of existing TSV technologies was first provided to better understand the implications of each TSV technology on power delivery and signal integrity. A case study was described to illustrate power distribution in a nine-plane 3D processor-DRAM stack. According to the International Technology Roadmap for Semiconductors, processor-memory stacks are expected to be one of the early applications of TSV-based 3D-ICs where the issue of power integrity is exacerbated [89].

Next, the importance of power gating has been emphasized for 3D-ICs. It was shown that conventional decoupling capacitor topologies can degrade power integrity when one or more planes are power-gated. A reconfigurable decoupling capacitor topology was discussed to alleviate this
issue and significantly enhance power integrity with relatively small overhead in physical area and power consumption.

An important concern, particularly in heterogeneous 3D integration with sensitive analog/RF blocks, is TSV-to-transistor noise coupling. This signal integrity concern was described and two approaches (that exhibit distinct accuracy versus complexity tradeoffs) were presented to analyze noise coupling in 3D-ICs. Finally, another case study of a 3D-IC with application to bio-electronics (neurotransmitter sensing) was discussed with emphasis on 3D signal integrity. It was demonstrated that the expected signal isolation advantages of 3D-ICs are possible if TSV-to-substrate noise coupling is significantly reduced.

REFERENCES


