Physical Design of Monolithic 3D ICs with Applications to Hardware Security

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***Abstract*—Monolithic 3D ICs provide vertical interconnects with comparable size to on-chip metal vias and therefore achieve ultra-high density device integration. A custom cell library and design flow are proposed to develop fully placed and routed monolithic 3D ICs. A monolithic 3D implementation of a 128-point, highly parallelized FFT core with approximately 330K cells is demonstrated. The effects of monolithic 3D technology on power, footprint, and performance are quantified. Furthermore, the proposed design kit and cell libraries are utilized to evaluate the effects of circuit camouflaging on system power, delay, and area. A camouflaged lightweight block cipher, SIMON, is developed. GDS-level simulation results demonstrate that the monolithic 3D technology is highly effective to facilitate the utilization of camouflaging technique against image analysis based reverse engineering attacks. At the expense of a slight degradation in timing characteristics, monolithic 3D technology eliminates not only the area, but also the power overhead related to camouflaging.**

***Keywords*—Monolithic 3D integration; 3D cell library; 3D hardware security; circuit camouflaging; reverse engineering**

I. Introduction

Recently, interest on monolithic 3D integration has grown in both academia and industry due to encouraging developments on sequentially fabricating multiple transistor layers (particularly the thermal characteristics) [1]. In monolithic vertical integration, stacked transistors are sequentially fabricated after the bottom layers have been manufactured. Communication among the tiers is achieved by monolithic inter-tier vias (MIVs). A critical challenge in the fabrication of monolithic 3D ICs is to minimize the detrimental effect of the manufacturing process of the top tier on bottom tier [2]. Thus, significant research on the fabrication side has focused on developing low thermal budget processes [3].

In transistor-level monolithic 3D integration, nMOS and pMOS transistors within a circuit are separated into two different tiers. This approach not only achieves fine-grained 3D integration with intra-cell MIVs, but also enables the individual optimization of the bottom and top tier devices. A process design kit and a standard cell library are developed in this research to characterize large-scale monolithic 3D ICs. This design kit is used to demonstrate the applicability of monolithic 3D technology to circuit camouflaging, an emerging countermeasure to thwart reverse engineering attacks that try to recover the original netlist through scanning electron microscopy (SEM) images [4], [5]. The circuit obfuscation level achieved by the camouflaging technique, however, depends upon the number and location of the camouflaged gates [5]. Thus, these parameters play an important role in achieving the desired attack resilience. A larger number of camouflaged gates strengthens the countermeasure at the expense of significant overhead in area, power, and delay characteristics [5]. Thus, monolithic 3D ICs introduce a unique opportunity due to significant potential to reduce the overhead of traditional circuit camouflaging [6]–[9]. Note that existing split manufacturing techniques developed primarily for through silicon via (TSV) and interposed based vertical integration are not applicable to monolithic 3D ICs. Unlike TSV based 3D ICs, in monolithic 3D ICs, all of the tiers are manufactured sequentially by the same foundry, as depicted in Fig. 1. Thus, splitting the system functionality into multiple tiers is not effective to protect monolithic 3D ICs from reverse engineering and hardware intellectual property (IP) piracy attacks from untrusted foundries.

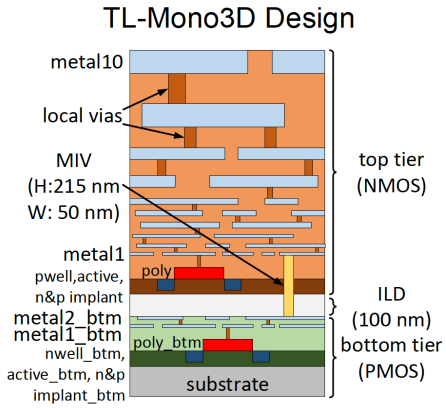

Fig. 1. Cross-section of the transistor-level monolithic (TL-Mono) 3D technology with two tiers. The top tier hosts the nMOS transistors whereas the pMOS transistors are placed within the bottom tier.

The rest of the paper is organized as follows. The details of the proposed open source cell library, characterization, and comparison with 2D technology are provided in Section II. Power, timing, and physical design characteristics of a 128-point FFT core developed with the proposed monolithic 3D standard cell library are also investigated in this section. The

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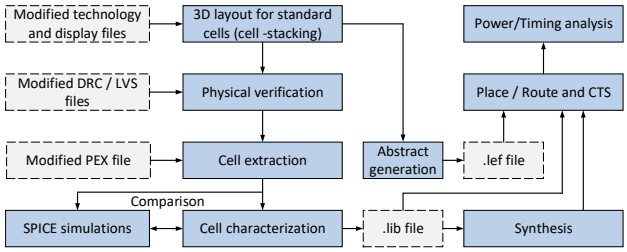

Fig. 2. Integration of the proposed open source cell library into design flow, illustrating the required modifications.

3D cell library is applied to circuit camouflaging in Section III and results of a camouflaged SIMON cipher are discussed. The paper is concluded in Section IV.

II. Open Source Cell Library and Design Flow for Monolithic 3D ICs

The primary characteristics of the proposed cell library are described in Section II-A. The design flow to integrate the proposed library into the design process is discussed in Section II-B.

A. Library Development

An open source standard cell library (*Mono3D*) for transistor-level monolithic 3D technology is developed in 45 nm technology with different cell heights to provide flexibility for routing congestion [10]–[13]. *Mono3D* consists of two tiers where each tier is based on the 2D 45 nm process design kit *FreePDK45* from North Carolina State University (NCSU) [14]. The pull-down network of a CMOS gate (nMOS transistors) is built within the top tier whereas the pull-up network (pMOS transistors) is fabricated within the bottom tier. Two metal layers are allocated to the bottom tier (metal1_btm and metal2_btm), as illustrated in Fig. 1. These metal layers are primarily for routing the intra-cell signals.

The top tier is separated from the bottom tier with an inter-layer dielectric (ILD) with a thickness of 100 nm. Inter-tier coupling is minimized at this thickness, as experimentally validated [15]. The 10 metal layers that exist in the top tier are used for inter-cell and global routing. The intra-cell connections that span the two tiers are achieved by MIVs. Each MIV has a width of 50 nm and height of 215 nm.

Each standard cell is developed with a full-custom design methodology using a cell stacking technique. The power rail is located at the top of the bottom tier and ground rail is located at the bottom of the top tier. These power and ground rails at each cell row are connected to the system-level power network through power and ground rings placed during the placement and routing process.

B. Design Flow

The design flow adopted in this work and the modifications required for 3D monolithic technology are depicted in Fig. 2. A new technology file (*.tf*) is generated for *Mono3D* to include all of the new layers (interconnects, via, ILD, and MIV). A new display resource file (*.drf*) is generated to develop full-custom layouts of the 3D cells. The design rule check (DRC), layout versus schematic (LVS) and parasitics extraction (PEX) are performed using *Calibre*. The DRC rule file is modified to include new features for the additional metal layers, vias, transistors, ILD and MIV. For example, minimum spacing between two MIVs is equal to 120 nm, producing an MIV pitch of 170 nm.

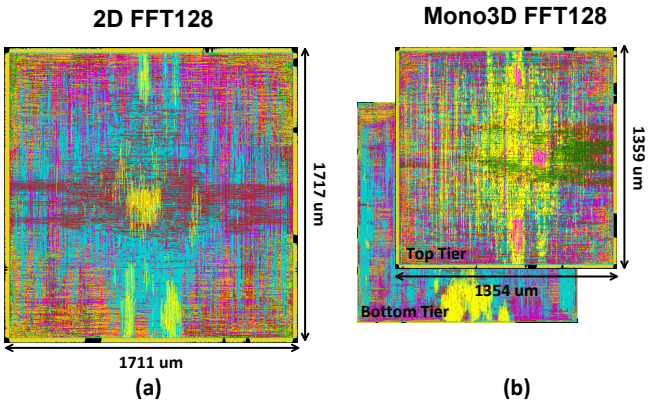

Fig. 3. The layout views of a highly parallelized 128-point FFT core in (a) conventional 2D technology, (b) transistor-level monolithic 3D technology.

The LVS rule file is also modified for the tool to be able to independently identify transistors located in separate tiers. The extracted netlist with MIVs is analyzed to accurately extract the interconnections between nMOS (within the top tier) and pMOS (within the bottom tier) transistors. The RC extraction rule file is modified to be able to recognize the new device tier, new metal layers, and MIVs. For metal interconnects, intrinsic plate capacitance, intrinsic fringe capacitance, and nearbody (coupling) capacitance are considered between silicon and metal, and metal and metal. A single MIV is characterized with a resistance of 5.5 Ωs and a capacitance of 0.04 fF.

After RC extraction, 3D cells are characterized with *Encounter Library Characterizer (ELC)* to obtain the timing and power characteristics (lookup tables) of each cell. The *.lib* file for the *Mono3D* generated by *ELC* is converted into the *.db* format, which is used for circuit synthesis, placement, clock tree synthesis, and routing.

C. System-Level Evaluation of Mono3D

The proposed open source *Mono3D* cell library and design flow are used to investigate the power, timing characteristics and routing congestion of a 3D 128-point FFT core with approximately 330K cells.

1) Footprint, Wirelength, and Routing Congestion: The layout views of the 2D and 3D versions of the 128-point FFT core are depicted in Fig. 3. The comparison of footprint, overall wirelength, and DRC violations in 2D and 3D designs is listed in Table I for both 500 MHz and 1.5 GHz clock frequencies.

According to this table, 3D FFT core consumes 37.5% less area as compared to conventional 2D version at 1.5 GHz. At 500 MHz, no DRC violations are reported. At high frequency

TABLE I
COMPARISON OF FOOTPRINT, WIRELENGTH, AND NUMBER OF DRC VIOLATIONS (VIOS) IN 2D AND MONOLITHIC 3D TECHNOLOGIES. THE PERCENT CHANGES WITH RESPECT TO 2D VERSIONS ARE LISTED.

Operating Frequency		500 MHz				1.5 GHz				
Circuit	Design Style	Footprint (mm^2)	Change (%)	Wirelength (μm)	Change (%)	Footprint (mm^2)	Change (%)	Wirelength (μm)	Change (%)	DRC Vios
FFT128	2D	2.54	-	12,205,011	-	2.94	-	15,201,864	-	0
	3D	1.59	**-37.2**	9,240,148	**-24.3**	1.84	**-37.5**	11,407,021	**-24.9**	7

TABLE II
COMPARISON OF POWER CONSUMPTION IN 2D AND MONOLITHIC 3D TECHNOLOGIES. *INT, SWI*, AND *LK* REFER, RESPECTIVELY, TO INTERNAL, SWITCHING (NET), AND LEAKAGE POWER.

Operating Frequency		500 MHz				1.5 GHz			
Circuit	Design Style	Power component (mW)				Power component (mW)			
		INT	SWI (Change)	LK	Total (Change)	INT	SWI (Change)	LK	Total (Change)
FFT128	2D	2,365	924.8 (-)	119.5	3,510 (-)	7,891	2,859 (-)	144.9	10,895 (-)
	3D	2,309	726.0 **(-21.50%)**	118.8	3,154 **(-10.14%)**	6,863	2,309 **(-19.24%)**	145.9	9,318 **(-14.47%)**

TABLE III
COMPARISON OF TIMING CHARACTERISTICS IN 2D AND MONOLITHIC 3D TECHNOLOGIES. *WS*, *WNS*, AND *TNS* REFER, RESPECTIVELY, TO WORST SLACK, WORST NEGATIVE SLACK, AND TOTAL NEGATIVE SLACK.

Operating Frequency		500 MHz	1.5 GHz		
Circuit	Design Style	WS (ns)	WNS (ns)	TNS (ns)	Number of Violations
FFT128	2D	0.21	-0.104	-516.100	8,097
	3D	0.23	-0.091	-302.582	6,221

constraint, however, 3D FFT core exhibits DRC violations (indication of routing congestion) due to denser layout as compared to 2D technology. The reduction in the overall wirelength is approximately 24%.

2) Power Characteristics: The power consumption of 2D and monolithic 3D FFT is compared in Table II. All of the three components of power consumption (internal, switching, and leakage) are provided. Internal power is consumed due to the intra-cell device and interconnect capacitances and short-circuit current during the switching activity of a cell. Switching power is consumed by the inter-cell interconnect (net) capacitances. Due to considerable reduction in overall wirelength in monolithic 3D designs, the switching power is reduced by 21.5% at 500 MHz and 19.2% at 1.5 GHz.

3) Timing Characteristics: The timing characteristics of the 2D and monolithic 3D FFT are compared in Table III where the worst slack (WS), worst negative slack (WNS), total negative slack (TNS), and number of timing violations are listed at both 500 MHz (with no timing violations) and 1.5 GHz (with timing violations). There is timing improvement in the 3D FFT design due to both area and wirelength decrease in the proposed 3D library. Specifically, the WNS decreases by 13 ps, and there are 1876 less timing violations which decreases TNS by 213 ns at 1.5 GHz.

III. APPLICATION TO HARDWARE SECURITY

A. Circuit Camouflaging

Circuit camouflaging is a method to obfuscate logic function by making subtle changes to the physical layout of standard cells [4], [5]. The primary goal of camouflaging is to disguise the circuit against a reverse engineer who utilizes SEM pictures to recover the original chip design. For example, from the SEM image analysis, a camouflaged logic cell appears to be a 2-input NAND gate. In practice, however, that cell can be a 2-input NOR gate. This wrong perception can be achieved by small changes on metal contacts and vias. Thus, an attacker cannot entirely rely on SEM image analysis to successfully extract the correct circuit netlist. Since reverse engineers cannot partially etch a layer [16], circuit camouflaging with dummy contacts/vias has become an effective method to obscure the original circuit. Camouflaging, however, incurs significant area, power, and delay overhead, particularly when the camouflaged number of cells increases [5].

B. Camouflaged Cells in 2D and Monolithic 3D Technologies

Two camouflaged standard cell libraries are developed. The first one is for conventional 2D technology whereas the second one is for monolithic 3D technology with inter-tier vias [6]. Both libraries contain 12 cells, as listed in Table IV. Of these cells, NAND, NOR, AND, OR, XOR, and XNOR are camouflaged. For example, NAND and NOR cells are designed to look identical where the actual function depends upon the real

TABLE IV
LIST OF STANDARD CELLS IN THE CAMOUFLAGED 2D AND MONOLITHIC 3D LIBRARIES.

Regular Standard Cells		Camouflaged Standard Cells
INVX1	INVX2	NAND2X1 & NOR2X1
CLKBUF1	CLKBUF2	AND2X1 & OR2X1
DFFPOSX1	FILL	XNOR2X1 & XOR2X1

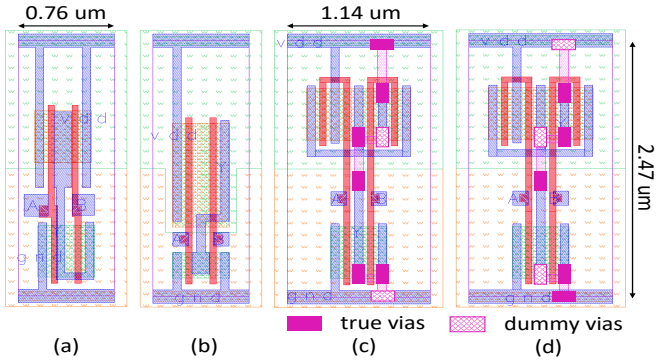

Fig. 4. Standard cell layouts in 2D technology: (a) conventional NAND, (b) conventional NOR, (c) camouflaged NAND, and (d) camouflaged NOR.

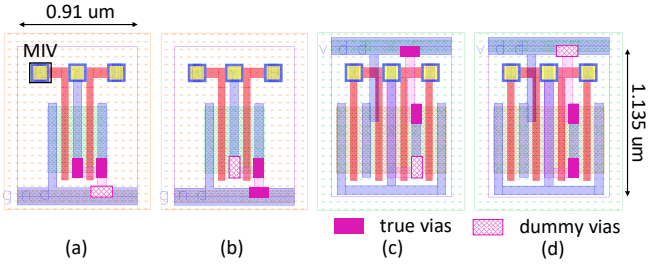

Fig. 5. Camouflaged cell layouts in monolithic 3D technology: (a) top tier of NAND gate, (b) top tier of NOR gate, (c) bottom tier of NAND gate, (d) bottom tier of NOR gate.

and dummy contacts. This behavior also holds for AND/OR and XOR/XNOR cell pairs. The camouflaged 2D NAND and NOR gates with both dummy and real contacts/vias are shown, respectively, in Figs. 4(c) and (d). As a reference, the non-camouflaged NAND and NOR gates are also illustrated in Figs. 4(a) and (b), respectively.

In camouflaged monolithic 3D cells, the power rail is located at the top of the bottom tier and the ground rail is located at the bottom of the top tier. MIVs are distributed within the cell to minimize the interconnect distance and reduce the cell height, as shown in Fig. 5, where the camouflaged 3D NAND and NOR gates are illustrated. Both the top [see Figs. 5(a) and b)] and bottom tiers [see Figs. 5(c) and d)] in each cell look identical from top view.

In camouflaged 3D cells, the cell height is 1.135 μm, which is 54% smaller than the standard cell height (2.47 μm as shown in Fig. 4) in *Nangate* 45 nm cell library [17]. The top tier metal layers and true/dummy contacts of these camouflaged cells are illustrated in Fig. 6 for both NAND and NOR cells. Note that contrary to non-camouflaged cells that utilize only metal 1 for intra-cell routing, camouflaged cells require both metal 1 and metal 2 for routing, which affects both the cell-level and chip-level area, power and timing characteristics.

C. Cell-Level Evaluation

The effect of camouflaging on cell-level area, delay, and power consumption is investigated for both 2D and 3D technologies. The results are listed in Table V.

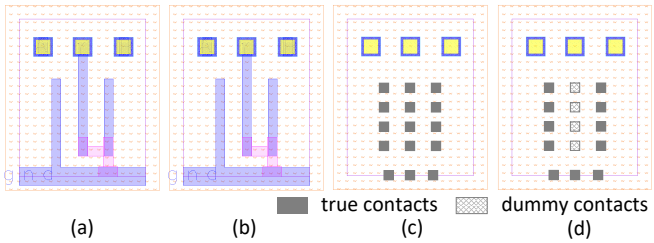

Fig. 6. Metal layers and true/dummy contacts within the top tier of camouflaged monolithic 3D cells: (a) NAND metal layers, (b) NOR metal layers, (c) NAND contacts, (d) NOR contacts.

TABLE V
AREA, AVERAGE DELAY AND POWER CHARACTERISTICS OF CONVENTIONAL 2D, CAMOUFLAGED 2D (2D_C), MONOLITHIC 3D, AND CAMOUFLAGED MONOLITHIC 3D (3D_C) STANDARD CELLS. ALL OF THE PERCENTAGES ARE WITH RESPECT TO CONVENTIONAL 2D RESULTS.

Std Cell	Design	Area (μm^2)	Delay (ps)	Power (μW)
NAND_2D	2D	1.88	7.61	1.28
	2D_C	2.82 (**50%**)	8.93 (**17%**)	1.82 (**42%**)
NAND_3D	3D	0.6 (**-68%**)	8.95 (**18%**)	1.45 (**13%**)
	3D_C	1.04 (**-45%**)	10.3 (**35%**)	1.97 (**54%**)
NOR_2D	2D	1.88	8.73	1.41
	2D_C	2.82 (**50%**)	8.05 (**-8%**)	1.80 (**28%**)
NOR_3D	3D	1.04 (**-45%**)	9.05 (**4%**)	1.42 (**1%**)
	3D_C	1.04 (**-45%**)	8.22 (**-6%**)	1.82 (**29%**)
AND_2D	2D	2.87	14.2	2.28
	2D_C	3.66 (**28%**)	17.0 (**20%**)	2.98 (**31%**)
AND_3D	3D	1.27 (**-58%**)	15.3 (**8%**)	2.32 (**2%**)
	3D_C	1.42 (**-51%**)	18.1 (**27%**)	2.99 (**31%**)
OR_2D	2D	2.87	15.4	2.26
	2D_C	3.66 (**28%**)	15.6 (**1%**)	2.75 (**22%**)
OR_3D	3D	1.42 (**-51%**)	16.9 (**10%**)	2.35 (**4%**)
	3D_C	1.42 (**-51%**)	17.0 (**10%**)	2.76 (**22%**)
XNOR_2D	2D	4.67	29.6	9.82
	2D_C	4.67 (**0%**)	31.2 (**5%**)	10.3 (**5%**)
XNOR_3D	3D	3.10 (**-34%**)	31.4 (**6%**)	10.2 (**4%**)
	3D_C	3.10 (**-34%**)	32.9 (**11%**)	10.5 (**7%**)
XOR_2D	2D	4.67	29.3	10.1
	2D_C	4.67 (**0%**)	30.6 (**4%**)	10.5 (**4%**)
XOR_3D	3D	3.10 (**-34%**)	31.7 (**8%**)	10.4 (**3%**)
	3D_C	3.10 (**-34%**)	32.5 (**11%**)	10.7 (**6%**)

1) Footprint: For the 2D camouflaged cells, the increase in cell area varies from 0 to 50%, depending upon the cell type. For example, for XNOR and XOR gates, there is no overhead in area since the transistors in both cells have the same sizes. Thus, it is not necessary to upsize the cells to make them look identical. Furthermore, the inherent cell area is sufficiently large, leaving sufficient space for intra-cell routing needed for camouflaging the cells. For camouflaged monolithic 3D standard cells, the cell area is reduced as compared to non-camouflaged 2D cells due to the inherent advantage of monolithic 3D technology. This reduction in cell area varies from 34% to 51%. Despite more than 50% reduction in cell height, the average area reduction is less than 50% due to camouflaging overhead and MIVs. The area of the non-camouflaged 3D cells is also listed in the table as a reference.

2) Delay and Power Consumption: *HSPICE* simulations are performed on the extracted non-camouflaged 2D, 3D, and camouflaged 2D and 3D netlists to compare the cell-

TABLE VI
THE OVERALL NUMBER OF GATES AND DISTRIBUTION OF CAMOUFLAGED AND NON-CAMOUFLAGED CELLS.

Circuit	Number of Gates	**Non-Camouflaged Cells**		**Camouflaged Cells**					
		DFF	INV	NAND	NOR	AND	OR	XOR	XNOR
SIMON	903	168 (18.6%)	23 (2.5%)	529 (58.6%)	20 (2.2%)	1 (0.1%)	0	1 (0.01%)	161 (17.8%)

level power and delay characteristics at nominal operating conditions. Non-camouflaged 2D results are considered as the baseline for all of the percentages reported here. In general, the 2D camouflaged cells of this work have significantly less delay and power overhead as compared to [5]. As listed in Table V, for the 2D camouflaged cells, the percent change in average propagation delay varies from -8% (for the NOR gate) to 20% (for the AND gate), while for the monolithic 3D technology, it varies from -6% (for the NOR gate) to 38% (for the NAND gate). Thus, except the NOR gate, camouflaging increases the delay in both 2D and 3D technologies due to additional interconnects and vias. For the camouflaged NOR gate, the size of the nMOS has been increased from 0.25 μm to 0.5 μm (since the size of each nMOS in the NAND gate is 0.5 μm due to series connection), thereby lowering the average propagation delay.

For the camouflaged 2D cells, the increase in power consumption varies from 4% (for the XOR gate) to 42% (for the NAND gate), while for the camouflaged monolithic 3D cells the power overhead is between 6% (for the XOR gate) and 54% (for the NAND gate).

According to Table V, camouflaged 3D cells have, on average, 7.82% higher propagation delay and 2.33% higher power consumption as compared to the camouflaged 2D cells. This slight increase in the delay and power is due to the MIV impedances and the denser cell layout that produces additional coupling capacitances. Thus, for monolithic 3D technology, significant reduction in cell area is achieved at the expense of slight increase in cell-level power and delay characteristics. The chip-level implications of these effects are investigated in the following section.

D. System-Level Evaluation of Circuit Camouflaging

The proposed camouflaged cells are characterized (after *RC* extraction) with *Encounter Library Characterizer (ELC)* to obtain timing and power characteristics. SIMON block cipher, a balanced Feistel cipher to fulfill the security concerns of sensitive and hardware constrained applications, is synthesized using *Synopsys Design Compiler*. The distribution of cells in camouflaged SIMON cipher is listed in Table VI. Synthesized netlists are placed (at 70% placement density) and routed using *Cadence Encounter*. The clock frequency is 0.5 GHz for all of the circuits.

1) Footprint and Wirelength: Physical layouts of the conventional 2D, camouflaged 2D, and camouflaged monolithic 3D implementations of the SIMON block cipher are depicted in Fig. 7. Approximately 80% of the gates is camouflaged. The area and overall wirelength characteristics in conventional 2D, camouflaged 2D, and camouflaged monolithic 3D are listed in Table VII. According to this table, in camouflaged 2D circuits,

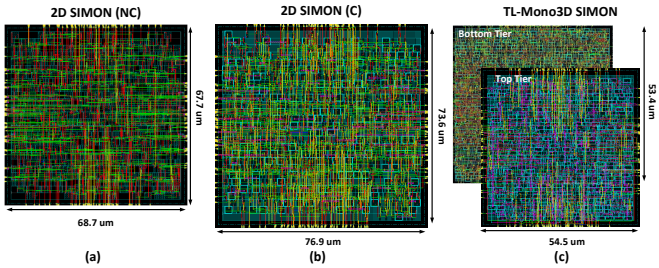

Fig. 7. The layout views of SIMON cipher in (a) conventional 2D technology without camouflaging, (b) conventional 2D technology with camouflaging, (c) transistor-level monolithic 3D technology with camouflaging.

TABLE VII
AREA AND WIRELENGTH CHARACTERISTICS IN CONVENTIONAL 2D, CAMOUFLAGED 2D (2D_C), MONOLITHIC 3D, AND CAMOUFLAGED MONOLITHIC 3D (3D_C) CIRCUITS. ALL OF THE PERCENTAGES ARE WITH RESPECT TO CONVENTIONAL 2D RESULTS.

Circuit	Design style	Area (mm^2)	Change (%)	Wirelength (μm)	Change (%)
SIMON_2D	2D	0.0047	-	10694	-
	2D_C	0.0057	**21**	11905	**11**
SIMON_3D	3D	0.0025	**-47**	8530	**-20**
	3D_C	0.0029	**-38**	9008	**-16**

the area and wirelength increase, respectively, by 21.1% and 11.3%. For the camouflaged monolithic 3D circuit, however, the area and overall wirelength are reduced, respectively, by 37.7% and 15.7% as compared to the conventional 2D implementation.

2) Power Characteristics: The power consumption of the conventional 2D, camouflaged 2D, and camouflaged monolithic 3D circuits is compared in Table VIII. All of the three components of power consumption (gate, interconnect, and leakage) are provided. The camouflaged 2D circuits consume 7.4% more power than the conventional 2D version. This increase is primarily due to the increase in camouflaged gate power and longer interconnects. In camouflaged 2D cells, an additional metal layer is needed for intra-cell routing to make

TABLE VIII
COMPARISON OF POWER CONSUMPTION IN CONVENTIONAL 2D, CAMOUFLAGED 2D (2D_C), MONOLITHIC 3D, AND CAMOUFLAGED MONOLITHIC 3D (3D_C) CIRCUITS. *INT* REFERS TO INTERCONNECT POWER. ALL OF THE PERCENTAGES ARE WITH RESPECT TO CONVENTIONAL 2D RESULTS.

Circuit	Design style	Power Component (mW)			
		Gate	Int.	Leakage	Total
SIMON_2D	2D	5.57	1.43	0.20	7.20
	2D_C	5.89	1.59	0.25	7.73 **(7.4%)**
SIMON_3D	3D	4	1.12	0.20	5.32 **(-26%)**
	3D_C	4.18	1.17	0.25	5.60 **(-22%)**

TABLE IX
TIMING CHARACTERISTICS IN CONVENTIONAL 2D, CAMOUFLAGED 2D (2D_C), MONOLITHIC 3D, AND CAMOUFLAGED MONOLITHIC 3D CIRCUITS. ALL OF THE PERCENTAGES ARE WITH RESPECT TO CONVENTIONAL 2D RESULTS.

Circuit	Design Style	Worst Slack (ns)
SIMON_2D	2D	0.921
	2D_C	0.770 **(-16%)**
SIMON_3D	3D	0.885 **(-4%)**
	3D_C	0.745 **(-19%)**

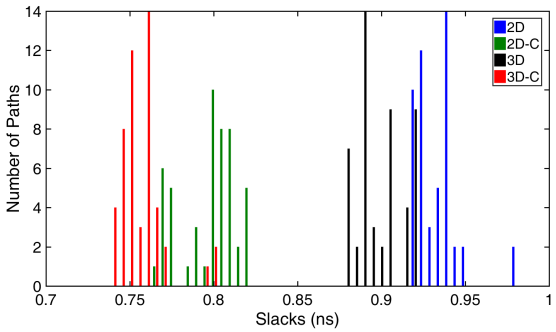

Fig. 8. Slack distribution of the 50 slowest paths in SIMON cipher for 2D technology without (2D) and with (2D-C) camouflaging, and monolithic 3D technology without (3D) and with camouflaging (3D-C).

the two cells with different logic functions look identical. Since this metal layer occupies a routing track for inter-cell routing, the overall interconnect length increases (see Table VII), thereby increasing the net power. Alternatively, camouflaged monolithic 3D circuits consume 4% less power than the conventional 2D version. This reduction is primarily due to reduced area and therefore shorter interconnects. Thus, an important observation for monolithic 3D technology is that the cell-level power increase due to camouflaging is compensated by the reduction in interconnect power. Also note that in SIMON cipher, gate power is slightly reduced in 3D technology despite the increase at the cell-level power consumption.

This behavior is due the reduced interconnect length in 3D technology which improves the average signal slew (due to lower interconnect resistance), which in turn reduces the short circuit power (one of the components of gate power).

3) Timing Characteristics: The worst slack (from the slowest timing path) of the conventional 2D, camouflaged 2D, and camouflaged monolithic 3D circuits is compared in Table IX. Note that the timing constraints are satisfied in all of the circuits at 0.5 GHz frequency. According to this table, camouflaging degrades the timing characteristics for both 2D and 3D technologies since the slack is reduced. The average reduction in slack is approximately 16% for camouflaged 2D and 19% for camouflaged 3D circuits.

To better observe the change in timing characteristics, the slack histogram of the 50 slowest paths is provided in Fig. 8, where the effect of 2D and 3D camouflaging on slack is illustrated. 2D camouflaging degrades the slack by approximately 120 ps (6% of the clock period). 3D camouflaging causes an additional degradation of approximately 50 ps (with respect to non-camouflaged 2D) due to larger cell-level delays.

IV. CONCLUSION

An open source transistor-level monolithic 3D cell library is developed and integrated into a digital flow. The proposed library is used to investigate several important characteristics of monolithic 3D ICs such as footprint, timing and power consumption. The results of a large-scale FFT core operating at 1.5 GHz demonstrate that the monolithic 3D technology can reduce the footprint and overall power consumption by, respectively, 38% and 14%. The proposed 3D cell library is used to achieve low overhead circuit camouflaging to thwart SEM image analysis based reverse engineering attacks. The results obtained from fully placed and routed SIMON cipher demonstrates that monolithic 3D technology is highly effective in eliminating not only the area, but also the power overhead of circuit camouflaging at the expense of a slight degradation in timing characteristics.

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