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Compact model to efficiently characterize TSV-to-transistor noise coupling in 3D ICs ☆

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ABSTRACT

A methodology is proposed to characterize through silicon via (TSV) induced noise coupling in three-dimensional (3D) integrated circuits. Different substrate biasing schemes (such as a single substrate contact versus regularly placed substrate contacts) and TSV fabrication methods (such as via-first and via-last) are considered. A compact π model is proposed to efficiently estimate the coupling noise at a victim transistor. Each admittance within the compact model is approximated with a closed-form expression consisting of logarithmic functions. The methodology is validated using the 3D transmission line matrix (TLM) method, demonstrating, on average, 4.8% error. The compact model and the closed-form expressions are utilized to better understand TSV induced noise as a function of multiple parameters such as TSV type, placement of substrate contacts, signal slew rate and voltage swing. The effect of differential TSV signaling is also investigated. Design guidelines are developed based on these results.

1. Introduction

Three-dimensional (3D) integrated circuits (ICs) have emerged as an effective solution to some of the critical issues encountered in 2D ICs such as the adverse effects of global interconnects [1,2]. In wafer-level 3D technologies, multiple wafers are thinned, aligned, and vertically stacked. For example, alignment accuracy of 1 μm has already been demonstrated [3]. Multiple bonding techniques have also been developed such as adhesive [4,5], oxide [6], and metal bonding [7]. The wafer thinning capability varies from hundreds of nanometers to several hundred micrometers, depending upon whether bulk silicon or silicon-on-insulator technology is utilized [8,9].

Through silicon vias (TSVs) provide communication among different tiers of a 3D stack, reducing the global interconnect length [2]. Several distinct TSV fabrication methods exist depending upon when the TSVs are formed. These methods are (1) via-first/middle [10,11] and (2) via-last TSVs [12]. Furthermore, since the tiers can be separately processed using different technologies, heterogeneous integration of diverse circuits and materials is facilitated, as depicted in Fig. 1.

International Technology Roadmap for Semiconductors identifies three phases for the application of 3D integration technology: (1) memory stacks, (2) processor-memory stacks, and (3) heterogeneous 3D integration with sensing and communication blocks [13]. An important challenge in each of these applications is to ensure system-wide signal integrity, which is exacerbated due to the multiple tiers interconnected with TSVs. In addition to traditional noise coupling and propagation mechanisms such as cross-talk, power supply noise, and substrate coupling, 3D ICs suffer from TSV induced noise coupling [14,15]. Specifically, during a signal transition within a TSV, noise couples from TSV into the substrate due to both dielectric and depletion capacitances. The coupling noise propagates throughout the substrate and affects the reliability of nearby transistors. This issue is exacerbated for TSVs that carry signals with high switching activity factors and fast transitions such as clock signals.

Analog/RF blocks and memory cells are among the most sensitive circuits to substrate noise coupling. For example, in [16], experimental data demonstrates that the signal-to-noise-plus-distortion ratio (SNDR) of a delta-sigma modulator is reduced by more than 20 dB due to substrate noise. Note that in heterogeneous 3D systems (see Fig. 1), the front-end circuitry consisting of analog/RF blocks is typically located at the top plane (closer to the I/O pads) to reduce the overall impedance between the pads and analog inputs. In this floorplan, TSVs are required to transmit the digital signals (including the clock signal) to the data processing plane. Thus, TSV induced noise becomes an important issue

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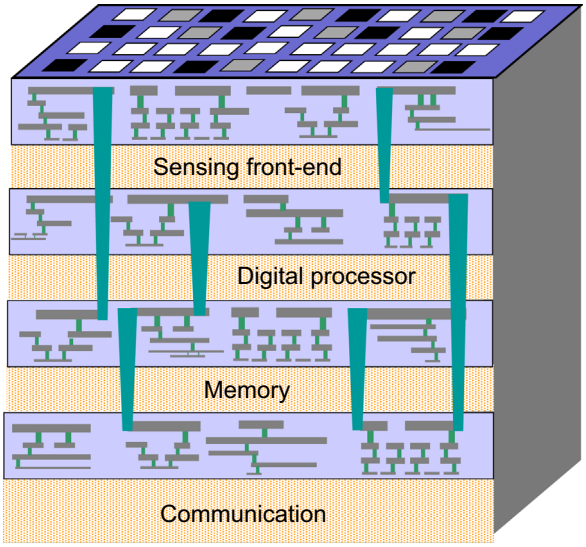

Fig. 1. Three-dimensional integration of diverse planes using through silicon via technology [2].

for the reliability of the analog/RF blocks. Digital transistors are also affected by TSV induced noise if the physical distance between the TSV and device is sufficiently short [17]. TSV induced noise changes the drain current characteristics of both an on and off transistor, as observed in [18].

Existing works have investigated TSV induced noise coupling using different approaches [19,20]. For example, in [19], the effect of several parameters such as substrate type, TSV height, TSV isolation layer thickness, transient signal slew rate has been investigated. An *RC* grid has been used to model the substrate. Alternatively, some works have focused on the mitigation of TSV induced noise. In [20], the efficacy of traditional techniques (such as guard rings) in reducing TSV induced noise has been investigated. A three-dimensional transmission line matrix (3D-TLM) method has been used to model the TSVs and substrate. These studies, however, do not consider different substrate biasing schemes and distinct TSV fabrication methods. Furthermore, computationally expensive approaches (such as 3D-TLM and field solvers) are utilized, prohibiting the use of these approaches for fast evaluation of different physical structures during the early stages of TSV floorplanning.

The primary contributions of this paper are as follows: (1) a compact model and a closed-form expression for each parameter within this model are developed to efficiently estimate TSV induced noise at a victim transistor, (2) the effect of different substrate biasing schemes and both via-first and via-last TSV characteristics are considered by the proposed model, which is validated using the 3D-TLM method, (3) design guidelines on substrate contact placement, TSV type, slew rate and voltage swing of the transient signals, and differential signaling are provided to reduce TSV induced noise based on the results obtained from the proposed compact model.

The rest of the paper is organized as follows. A highly distributed electrical model (used as a reference to validate the proposed compact model) to analyze noise injection and propagation is described in Section 2. A compact π model is proposed in Section 3 for efficient estimation of TSV induced noise at a victim transistor. Each admittance within the compact model is expressed in Section 4 as a function of multiple physical parameters. This approach is useful to consider different substrate biasing schemes and TSV types. Design guidelines are provided in Section 5 based on the analysis results obtained from the compact model. Finally, the paper is concluded in Section 6.

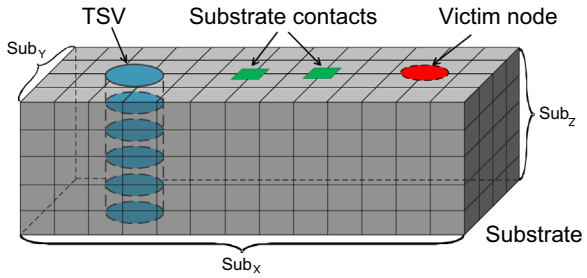

Fig. 2. Physical structure used to analyze TSV induced noise coupling.

2. Distributed model for TSV induced noise coupling

To characterize TSV induced noise coupling as a function of multiple design parameters, the physical structure depicted in Fig. 2 is used. This structure consists of a noise injector (TSV), a noise transmitter (substrate), and a noise receptor (victim transistor). Substrate contacts are also included to bias the substrate. Note that the number and placement of substrate contacts between the TSV and the victim transistor play an important role in the noise coupling analysis and safe zone characterization, as demonstrated in this paper.

To analyze this physical structure, several approaches have been adopted such as using an electromagnetic field solver, a device simulator, and a highly distributed model using a 3D TLM method [20–22]. In the distributed model, the physical structure is discretized into unit cells (for both TSV and substrate) and each unit cell is modeled with lumped parasitic impedances. A distributed model based on 3D-TLM is described in this section. This model is used as a reference to validate the proposed compact model (see Section 3) and closed-form expressions (see Section 4). The TSV and substrate models are described, respectively, in Sections 2.1 and 2.2. The advantages and limitations of a 3D-TLM based distributed model are discussed in Section 2.3.

2.1. TSV model

A typical TSV is represented as a cylinder with a diameter and depth, as illustrated in Fig. 3(a). Two primary components of a TSV are (1) conductive filling material such as polysilicon, tungsten or copper (varies depending upon the specific TSV fabrication technology as mentioned in Section 2.1.1) and (2) a dielectric layer that surrounds the conductive part to prevent the filling material from diffusing into silicon [12]. Different types of TSVs are summarized in the following section.

2.1.1. Via-first and via-last TSV technologies

TSVs are classified as via-first and via-last depending upon the fabrication method [23]. In the via-first method, TSVs are fabricated before the front-end-of-line (FEOL) process, *i.e.* before the transistors are etched within the silicon substrate. Alternatively, in a via-last technology, the TSVs are manufactured after the back-end-of-line (BEOL) process, *i.e.* after the metalization layers are fabricated.

Via-first TSVs utilize high resistivity polysilicon as the filling material. Polysilicon can withstand high temperatures required during the processing steps [23]. Alternatively, a low resistivity copper is used for via-last TSVs since via-last TSVs are fabricated after the formation of transistors and metal layers [23]. The physical dimensions of the TSVs are also affected by the fabrication

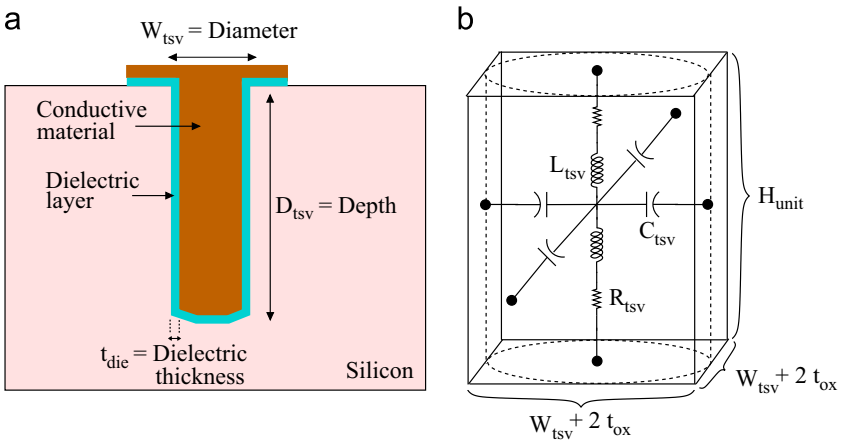

Fig. 3. TSV representations: (a) cross-section of a TSV consisting of a conductive material and dielectric layer and (b) electrical model of a unit TSV cell used for discretization.

Table 1
Via-first and via-last TSV characteristics [23].

Parameter	Via-first TSV	Via-last TSV
Filling material	Polysilicon	Copper
Material resistivity	7.2 μΩ.m	16.8 nΩ.m
Diameter	4 μm	10 μm
Height	10 μm	50 μm

process. Specifically, via-first TSV dimensions are typically smaller than via-last TSVs, as listed in Table 1. These physical characteristics and physical dimensions significantly affect the noise coupling analysis, as demonstrated in this paper.

2.1.2. TSV unit cell

A TSV unit cell consisting of parasitic resistance ${R_{tsv}}^{unit}$, parasitic inductance ${L_{tsv}}^{unit}$, and capacitance to substrate ${C_{tsv}}^{unit}$ is illustrated in Fig. 3(b) [24]. The x and y dimensions of the unit cell are both equal to $W+2t_{ox}$, as determined by the TSV diameter W and thickness of the oxide layer t_{ox}. The z dimension is equal to H_{unit}, as determined by the TSV height and the required resolution in the transmission line matrix method.

Considering the skin effect, the unit TSV resistance ${R_{tsv}}^{unit}$ is determined by [25]

$$R_{tsv}^{unit} = \frac{1}{2}\sqrt{(R_{AC}^{tsv,unit})^2 + (R_{DC}^{tsv,unit})^2}, \tag{1}$$

where the DC resistance $R_{DC}^{tsv,unit}$ and AC resistance $R_{AC}^{tsv,unit}$ are, respectively,

$$R_{DC}^{tsv,unit} = \frac{1}{2}\frac{\rho_f H_{unit}}{\pi(W/2)^2}, \tag{2}$$

$$R_{AC}^{tsv} = \frac{\rho_f H_{unit}}{4\pi(W/2)\delta_{tsv}}, \tag{3}$$

where ρ_f is the resistivity of the filling material and the skin depth δ_{tsv} is

$$\delta_{tsv} = \sqrt{\frac{\rho_f}{\pi f \mu_f}}, \tag{4}$$

where f is the frequency and μ_f is the permeability of the filling material. The unit TSV inductance ${L_{tsv}}^{unit}$ is

$$L_{tsv}^{unit} = \frac{1}{2}\frac{\mu_o}{4\pi}\left[2H_{unit}\ln\left(\frac{2H_{unit}+\sqrt{(W/2)^2+(2H_{unit})^2}}{W/2}\right) + \left(W/2-\sqrt{(W/2)^2+(2H_{unit})^2}\right)\right], \tag{5}$$

where μ_o is the vacuum permeability. The unit TSV capacitance ${C_{tsv}}^{unit}$ has two series components: oxide and depletion capacitance. The oxide capacitance is determined from the cylindrical capacitor formula as [26]

$$C_{ox}^{unit} = \frac{1}{4}\frac{2\pi\varepsilon_{ox}H_{unit}}{\ln\left(\frac{W/2+t_{ox}}{W/2}\right)}, \tag{6}$$

where ε_{ox} is the oxide permittivity. Assuming that the TSV voltage is at V_{DD}, TSV depletion capacitance is [27]

$$C_{dep}^{unit} = \frac{1}{4}\frac{2\pi\varepsilon_s H_{unit}}{\ln\left(\frac{W/2+t_{ox}+t_{dep}}{W/2+t_{ox}}\right)}, \tag{7}$$

where ε_s is the dielectric permittivity of silicon and t_{dep} is the depletion width within the substrate when the TSV voltage is at V_{DD}. The overall TSV capacitance is

$$C_{tsv}^{unit} = \frac{1}{4}\frac{C_{ox}^{unit}C_{dep}^{unit}}{C_{ox}^{unit}+C_{dep}^{unit}}. \tag{8}$$

2.2. Substrate model

A lightly doped bulk type substrate is assumed. Note that an epi type substrate with a heavily doped bulk beneath the lightly doped silicon layer typically produces greater noise coupling. Thus, an epi type substrate is less applicable to 3D heterogeneous integration where circuits with distinct electrical characteristics coexist. Also note that a lightly doped silicon substrate produces a lower TSV capacitance due to a larger depletion width [27].

A similar discretization technique is applied to model the lightly doped substrate. A unit substrate cell consisting of six parallel RC admittances is illustrated in Fig. 4. Referring to this figure, the three substrate resistances R_{s1}, R_{s2}, and R_{s3} are, respectively,

$$R_{s1} = \frac{1}{2}\frac{\rho_s d_3}{d_1 d_2}, \tag{9}$$

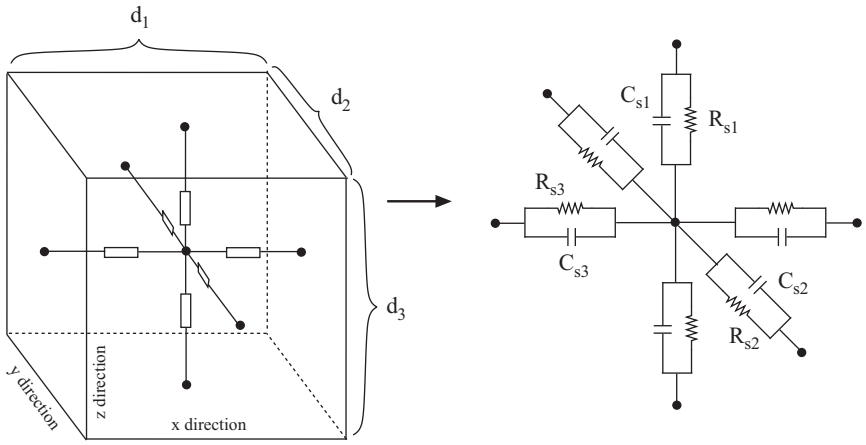

Fig. 4. Distributed model of a substrate network where each unit cell is represented by six resistances and capacitances.

$$R_{s2} = \frac{1}{2}\frac{\rho_s d_2}{d_1 d_3}, \tag{10}$$

$$R_{s3} = \frac{1}{2}\frac{\rho_s d_1}{d_2 d_3}, \tag{11}$$

where ρ_s is the substrate resistivity. Similarly, the three substrate capacitances C_{s1}, C_{s2}, and C_{s3} are, respectively,

$$C_{s1} = 2\frac{\varepsilon_s d_1 d_2}{d_3}, \tag{12}$$

$$C_{s2} = 2\frac{\varepsilon_s d_3 d_1}{d_2}, \tag{13}$$

$$C_{s3} = 2\frac{\varepsilon_s d_2 d_3}{d_1}. \tag{14}$$

2.3. Accuracy and limitations of the distributed model

The TSV and the substrate unit cells are combined to produce a highly distributed mesh based on 3D-TLM. Substrate contacts are also considered in the model to properly bias the substrate.

Previous studies have demonstrated the accuracy of the distributed model using 3D-TLM [28,20]. In [28], a fabricated test vehicle using an industrial via-last TSV technology is used to measure TSV induced noise coupling. The transfer function from TSV to victim transistor is measured and compared with the transfer function obtained from the distributed model. The comparison results demonstrate that below 100 MHz, the 3D-TLM matches reasonably well with the experimental results where the error is less than 1 dB. As the frequency increases (up to 10 GHz), the discrepancy increases, but remains within 3 dB. Similarly, in [20], a 3D field solver is used to analyze TSV-to-TSV noise coupling. The result is compared with the distributed 3D-TLM model. The error in the noise transfer function is within 2 dB until approximately 10 GHz. Both the measurement and 3D field solver results demonstrate that the 3D-TLM model can accurately model the 3D physical structure including a TSV, substrate contact, and victim transistor.

Despite the reasonable accuracy achieved by the distributed model, the computational complexity is significantly high, particularly when the dimensions of the unit cells are small. This issue is exacerbated as the distance between the TSV and the victim transistor increases. Furthermore, the number and location of the substrate contacts play an important role in characterizing the TSV safe zone. Re-analysis of the distributed structure when these characteristics change is computationally prohibitive. Therefore, a compact model is proposed to alleviate these limitations, as described in the following section. A highly distributed model based on a 3D-TLM method is used as a reference to evaluate the accuracy of the proposed compact model.

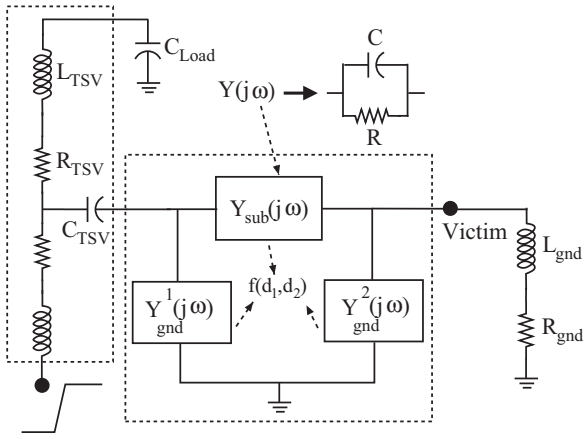

Fig. 5. Compact π model to efficiently estimate the noise at the victim node in the presence of a TSV and substrate contacts.

3. Compact Π model for efficient TSV noise coupling analysis

A two-port, linear time-invariant network can be generally characterized with four admittances: $Y_{11}(j\omega)$, $Y_{12}(j\omega)$, $Y_{21}(j\omega)$, and $Y_{22}(j\omega)$. Utilizing this characteristic, the proposed compact model consists of a single TSV cell and an equivalent two-port π network to model noise propagation, as depicted in Fig. 5.

Each electrical element within the π network consists of a parallel RC circuit, producing an admittance $(1/R)+j\omega C$. These admittances can be obtained from the distributed mesh (based on the 3D-TLM method), as described in the previous section. Specifically, the four $Y(j\omega)$ parameters of the distributed mesh are obtained through an AC analysis. The resistances and capacitances within the π network are determined such that the four $Y(j\omega)$ parameters of the compact π network are equal to the respective $Y(j\omega)$ parameters of the distributed mesh. According to this procedure, the admittances within the π network $Y_{sub}(j\omega)$, $Y^1_{gnd}(j\omega)$, and $Y^2_{gnd}(j\omega)$ are determined as follows:

- $Y_{sub}(j\omega) = (1/R_{sub}) + j\omega C_{sub} = Y_{21}(j\omega)$: represents the equivalent substrate admittance between the TSV and the victim transistor.

- $Y^1_{gnd}(j\omega)=(1/R^1_{gnd})+j\omega C^1_{gnd}=Y_{11}(j\omega)-Y_{21}(j\omega)$: represents the equivalent substrate admittance between the TSV and the ground node.
- $Y^2_{gnd}(j\omega)=(1/R^2_{gnd})+j\omega C^2_{gnd}=Y_{22}(j\omega)-Y_{21}(j\omega)$: represents the equivalent substrate admittance between the victim node and the ground node.

Note that in this study, Y_{11}, Y_{12}, Y_{21}, and Y_{22} are obtained by simulating the distributed mesh. Another approach is to obtain these Y parameters directly from a 3D field solver or measurement results. Also note that a single RC value is chosen for each admittance since the variation of the resistance and capacitance with frequency is negligible in the frequency range of interest. Specifically, the maximum change is less than 0.1% up to 100 GHz.

3.1. Accuracy analysis

The accuracy of the compact model is demonstrated by comparing the transfer function of the compact model with the transfer function of the distributed mesh with significantly higher complexity. Assuming a lightly doped substrate (with 10 Ω.cm resistivity and 103.4×10^{-12} F/m absolute permittivity), the two transfer functions are compared in Fig. 6 for both via-first and via-last TSVs.

In the distributed model, the dimensions L_{sub}, W_{sub}, and H_{sub} of the unit substrate cell are each 1 μm. The distance between the TSV and the victim node is 10 μm and a single substrate contact is placed in the middle of the two ports. The overall length of the substrate is 100 μm. The height of the substrate (determined by the TSV height) is 10 μm for a via-first TSV and 50 μm for a via-last TSV. Alternatively, the width of the substrate (partly determined by the TSV diameter) is 5 μm for a via-first TSV and 12 μm for a via-last TSV. Note that via-last TSVs have greater dimensions as compared to via-first TSVs, significantly affecting the noise at the victim node, as further discussed in Section 5.

As illustrated in Fig. 6, noise coupling due to TSVs is accurately estimated by the compact model with negligible error within the frequency range of interest. Note that the noise magnitude at the victim node is higher for via-last TSVs due to higher TSV capacitance and greater substrate dimensions. This difference is more than 20 dB at low frequencies and decreases to approximately 4 dB in the gigahertz range.

3.2. Complexity analysis

For a via-first TSV unit cell, the x and y dimensions are both equal to 4.4 μm ($W+2t_{ox}$ where $W=4$ and $t_{ox}=0.2$), whereas the z dimension is 1 μm. Alternatively, for a via-last TSV unit cell, the x and y dimensions are equal to 10.4 μm ($W+2t_{ox}$ where $W=10$ and $t_{ox}=0.2$) and the z dimension is 1 μm. In the distributed model with a via-first TSV, these dimensions produce 60,080 number of circuit elements (resistance, capacitance, and inductance). For a via-last TSV, this number increases to 720,400 due to greater y and z dimensions of the substrate. Alternatively, the compact π model contains only 11 number of elements for both via-first and via-last TSVs.

Sufficient accuracy and significantly lower complexity of the proposed compact model support the analysis of TSV induced noise. To consider the effect of various design parameters on coupling noise, each RC element within the compact model is expressed as a function of two physical design parameters, as described in the following section.

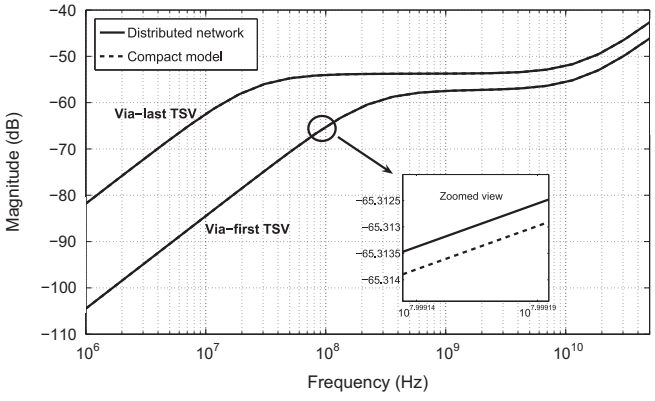

Fig. 6. Comparison of the proposed compact π model with high complexity distributed mesh for both via-first and via-last TSVs. The solid line represents noise at the victim node obtained from distributed mesh, whereas the dashed line represents noise at the victim node obtained from the compact π model.

4. TSV safe zone characterization

To determine TSV safe zone, the dependence of TSV induced noise on design parameters such as distance between TSV and victim node, and the number and location of substrate contacts should be characterized. Two substrate biasing schemes are considered. In the first scheme, as depicted in Fig. 7(a), a single substrate contact is placed between the TSV and the victim node. The physical distance between the TSV and the victim node is d_1 and the distance between the TSV and the substrate contact is d_2. In the second scheme, as depicted in Fig. 7(b), substrate contacts are regularly placed between the TSV and the victim node. In this case, d_2 refers to the distance between each substrate contact. The second scenario is considered since substrate contacts can be regularly placed in an automated manner based on latch-up constraints of the technology [29]. These two scenarios are separately investigated for both via-first and via-last TSVs, producing four different cases, as summarized below:

- Case 1: via-first TSV with a single substrate contact between TSV and victim node.
- Case 2: via-first TSV with regularly placed substrate contacts between TSV and victim node.
- Case 3: via-last TSV with a single substrate contact between TSV and victim node.
- Case 4: via-last TSV with regularly placed substrate contacts between TSV and victim node.

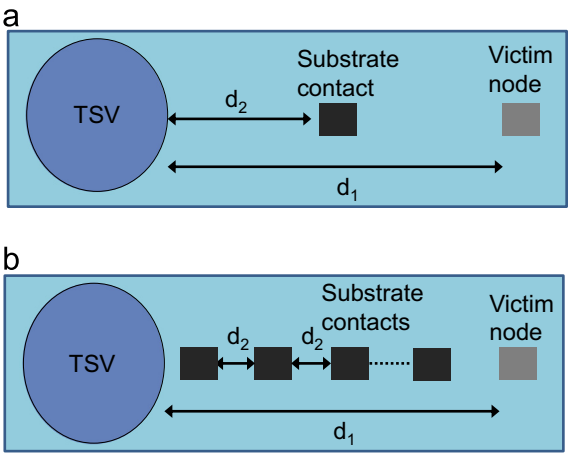

Fig. 7. Two substrate biasing schemes used to characterize noise coupling: (a) single substrate contact between TSV and victim node and (b) regular placement of the substrate contacts between TSV and victim node.

Table 2
Fitting coefficients for the function F that approximates the admittances within the compact model (see Fig. 5) for each case. The function F is given by (15).

Cases	Admittances	Fitting coefficients					Average error (%)
		A	B	C	D	E	
1	$R_{sub}=1000/F$ (kΩ)	27.09	0	0	−0.98	−5.11	6.6
	$C_{sub}=F$ (aF)	326.7	0.41	0.48	−17.26	−67.55	2.8
	$R^1_{gnd}=1000/F$ (kΩ)	28.31	0	0	−8.14	1.98	1.9
	$C^1_{gnd}=F$ (aF)	301.3	−0.28	0.66	−96.94	30.09	1.6
	$R^2_{gnd}=F$ (kΩ)	45.91	2.30	3.08	−218.3	154.9	9.6
	$C^2_{gnd}=1000/F$ (aF)	8.05	0.28	0.29	−20.39	12.49	10.4
2	$R_{sub}=1000/F$ (kΩ)	29.18	0.28	0.38	1.34	−11.78	8.3
	$C_{sub}=F$ (aF)	317.1	2.99	4.24	14.2	−127.6	10.8
	$R^1_{gnd}=1000/F$ (kΩ)	69.24	−0.046	1.97	−35.05	4.73	0.7
	$C^1_{gnd}=F$ (aF)	758.5	−0.49	21.13	−380.8	51.33	0.7
	$R^2_{gnd}=1000/F$ (kΩ)	9.50	−0.19	−0.99	−1.95	9.31	1.6
	$C^2_{gnd}=F$ (aF)	106.4	−2.05	−10.99	−20.83	100.7	1.6
3	$R_{sub}=1000/F$ (kΩ)	27.35	−0.082	0.036	−2.11	−1.12	2.4
	$C_{sub}=F$ (aF)	296.6	−0.89	0.83	−20.78	−13.12	1.9
	$R^1_{gnd}=1000/F$ (kΩ)	36.16	0.028	0.39	−10.16	1.18	2.4
	$C^1_{gnd}=F$ (aF)	235.6	−1.18	−2.16	−61.86	51.91	6.9
	$R^2_{gnd}=1000/F$ (kΩ)	11.57	0.11	−0.19	4.43	−5.86	11.6
	$C^2_{gnd}=F$ (aF)	129.1	1.18	−2.22	49.1	−65.23	10.9
4	$R_{sub}=1000/F$ (kΩ)	24.41	0.13	0.42	1.69	−8.36	8.5
	$C_{sub}=F$ (aF)	265.3	1.40	4.67	17.88	−91.2	7.2
	$R^1_{gnd}=1000/F$ (kΩ)	117.6	−0.03	0.40	−35.66	3.64	0.3
	$C^1_{gnd}=F$ (aF)	998	0.03	−68.78	37.31	32.11	2.9
	$R^2_{gnd}=1000/F$ (kΩ)	14.56	−0.01	−0.73	−3.49	5.93	2.4
	$C^2_{gnd}=F$ (aF)	162	−0.13	−8.17	−37.74	64.26	2.5

For each case, the $Y(j\omega)$ parameters of the π network are characterized as a function of d_1 and d_2. To evaluate these dependencies, AC analyses of the distributed mesh (based on 3D-TLM) described in Section 2 are performed with different values of d_1 and d_2. Note that a 3D field solver can also be used to perform these analyses. The data obtained in this step are used to generate a 3D surface for each resistance and capacitance within $Y_{sub}(j\omega)$, $Y^1_{gnd}(j\omega)$, and $Y^2_{gnd}(j\omega)$. This surface is approximated with a logarithmic function using a 3D least square regression analysis. The logarithmic function $F(d_1, d_2)$ used to approximate the admittances of the π network as a function of the physical distances d_1 and d_2 is

$$F(d_1, d_2) = A + Bd_1 + Cd_2 + D \ln d_2 + E \ln d_1, \quad (15)$$

where A, B, C, D, and E are fitting coefficients. These fitting coefficients are determined such that the resistor/capacitor value obtained from this expression reasonably approximates the actual resistor/capacitor value (in the compact π model) that is obtained from the highly distributed 3-D TLM model (or a field solver). Note that both the resistance (in kilo Ωs) and the capacitance (in atto Farads) of each $Y(j\omega)$ within the π network are represented by the function F. Also note that the distances d_1 and d_2 are in μm. Since the π network has three admittances each consisting of a parallel RC circuit, six logarithmic functions are developed for each case, producing a total of 24 functions. The fitting coefficients for each function are listed in Table 2.

As an example, the resistance R_{sub} and the capacitance C_{sub} of the $Y_{sub}(j\omega)$ are plotted, respectively, in Fig. 8(a) and (b) for a via-first TSV with a single substrate contact (case 1). The same parameters are plotted for a via-last TSV with regularly placed substrate contacts (case 4) in Fig. 8(c) and (d). The dotted points represent the data obtained from the analysis of the distributed mesh and the surface represents the function F that approximates these data. The procedure is similar for other cases and the RC elements of the remaining admittances [$Y^1_{gnd}(j\omega)$ and $Y^2_{gnd}(j\omega)$] within the compact model. Note that in all cases, d_1 is greater than d_2 since substrate contacts are placed between the TSV and the victim node.

The sufficient accuracy of the fitting method is demonstrated by quantifying the average percent error (as compared to the distributed mesh based on 3D-TLM) for each resistance and capacitance within the π network. Specifically, for each case, d_1 and d_2 are varied and the highly distributed model is simulated to obtain the RC values within the π model. The difference between these RC values and those obtained by (15) determines the error. The average error is listed in the last column of Table 2 for each case.

Note that the fitting coefficients listed in Table 2 are obtained for a certain range of d_1 and d_2. Specifically, for case 1 and case 3 (where a single substrate contact exists between the TSV and the victim node), d_1 (distance between TSV and victim node) varies from 4 μm to 55 μm and d_2 (distance between TSV and substrate contact) varies from 2 μm to 33 μm. Alternatively, for case 2 and case 4 (where multiple substrate contacts are regularly placed between the TSV and the victim node), d_1 varies from 4 μm to 44 μm and d_2 (distance between two substrate contacts) varies from 2 μm to 8 μm. Note that the maximum average error is slightly over 10% for certain resistances and capacitances. This error, however, does not significantly affect the electrical characteristics (and noise estimation at the victim node) since the maximum error occurs at the extreme cases when the resistance is sufficiently large and capacitance is sufficiently small. Also note that the average error over four cases is 4.8%. The proposed model and the function F can be used to efficiently characterize TSV-to-transistor noise coupling, as discussed in the following section.

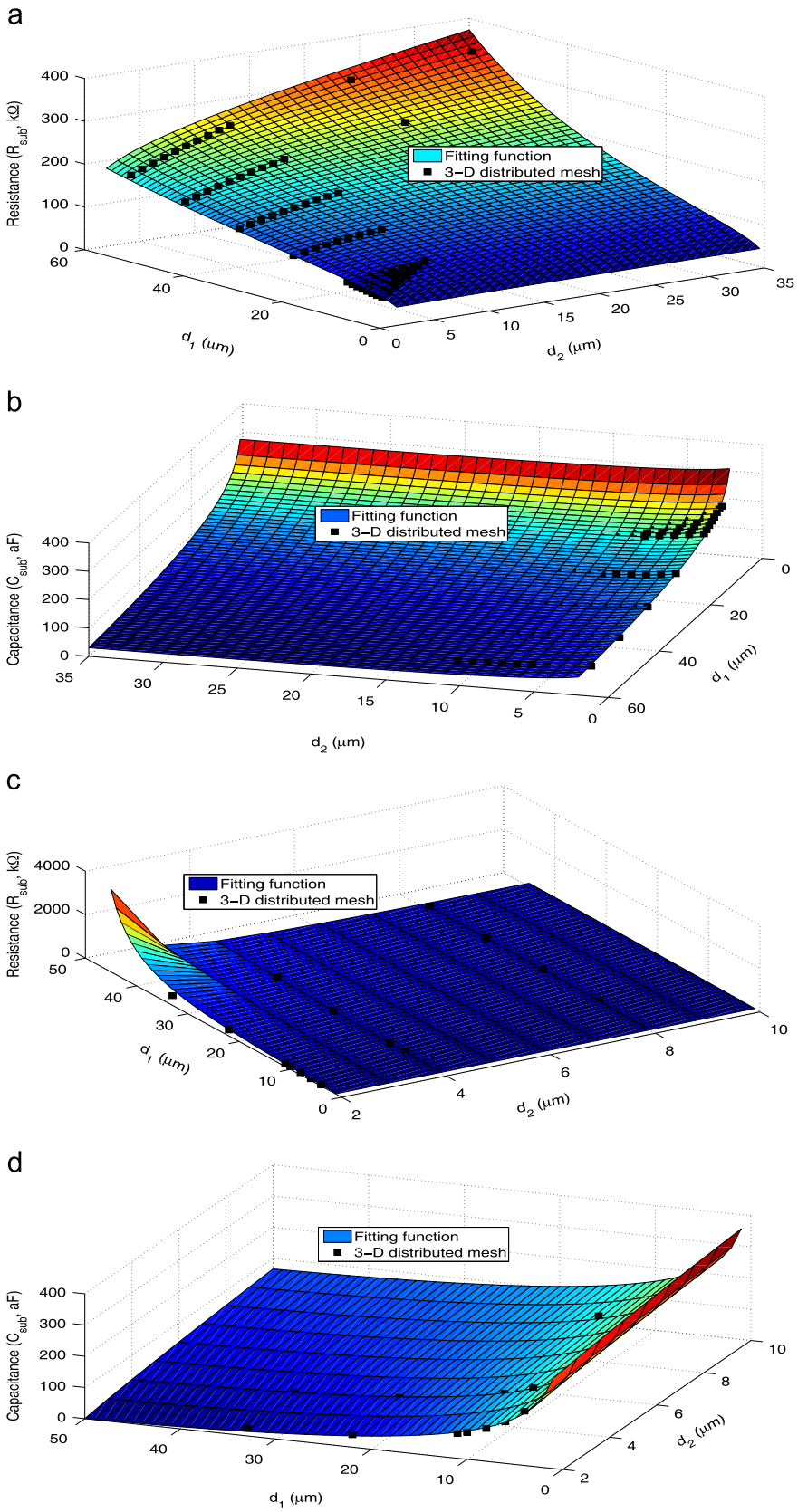

Fig. 8. Comparison of the data obtained from the analysis of the distributed mesh with the function F that approximates these data: (a) resistance R_{sub} of the $Y_{sub}(j\omega)$ with a via-first TSV and a single substrate contact (case 1), (b) capacitance C_{sub} of the $Y_{sub}(j\omega)$ with a via-first TSV and a single substrate contact (case 1), (c) resistance R_{sub} of the $Y_{sub}(j\omega)$ with a via-last TSV and regularly placed substrate contacts (case 4), and (d) capacitance C_{sub} of the $Y_{sub}(j\omega)$ with a via-last TSV and regularly placed substrate contacts (case 4).

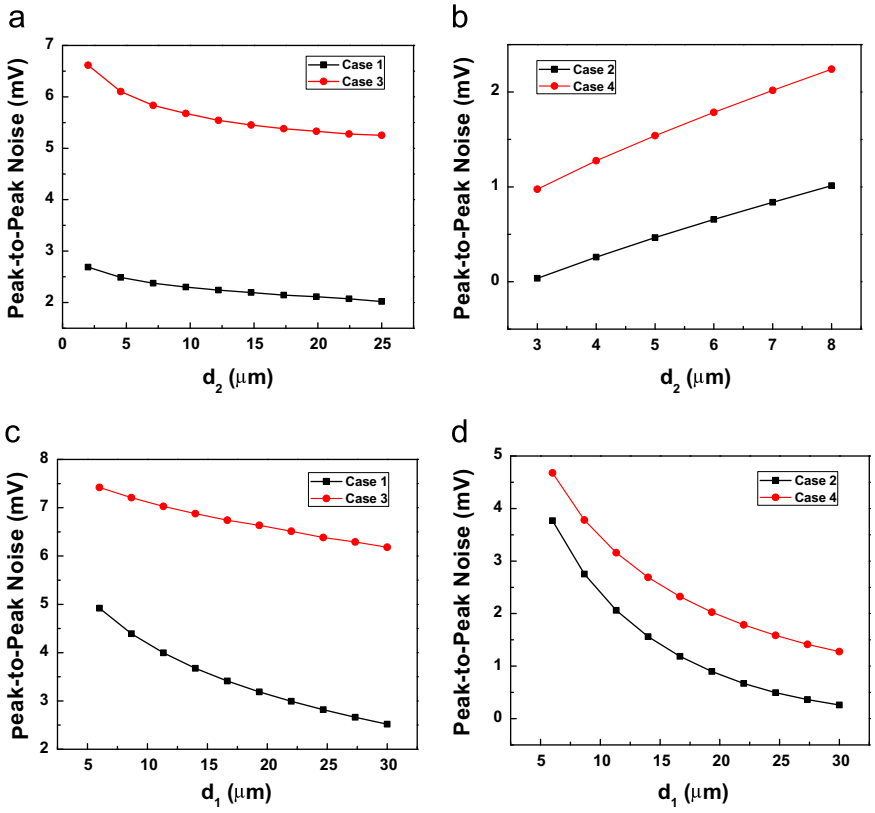

Fig. 9. TSV induced switching noise at the victim node: (a) as a function of d_2 at constant d_1 for case 1 and case 3, (b) as a function of d_2 at constant d_1 for case 2 and case 4, (c) as a function of d_1 at constant d_2 for case 1 and case 3, and (d) as a function of d_1 at constant d_2 for case 2 and case 4.

5. Design guidelines

The compact model illustrated in Fig. 5 and fitting parameters obtained in Section 4 are used to investigate the effect of various design and fabrication parameters such as placement of substrate contacts and TSV type (see Section 5.1), slew rate (see Section 5.2) and voltage swing (see Section 5.3) of the TSV signals, and differential signaling (see Section 5.4). Design guidelines are developed based on the analysis results to improve signal integrity in TSV based 3D ICs.

5.1. Placement of substrate contacts

Peak-to-peak noise at the victim transistor due to TSV activity is analyzed using (15) and the compact model. This noise is depicted in Fig. 9(a) and (b) as a function of d_2 when d_1 is constant at 30 μm.

According to Fig. 9(a), where a single substrate contact exists between the TSV and the victim node, switching noise is reduced as the substrate contact is placed closer to the victim node as opposed to the TSV. This characteristic is due to TSV height and distributed TSV capacitance to substrate. Thus, a single substrate contact closer to the TSV is not sufficiently effective since noise is injected into the substrate along the entire TSV depth. Note that based on Fig. 9(a), this characteristic is stronger in via-last TSVs since the height of a via-last TSV is five times greater than a via-first TSV. In traditional 2D circuits, it is typically a physical design decision to place the substrate contacts (or guard rings) around an aggressor noise source or around a sensitive victim block. In 3D circuits where TSVs are primary source of switching noise, placing the substrate contacts closer to the victim block is more advantageous, as demonstrated in Fig. 9(a).

According to Fig. 9(b), where multiple, regularly placed substrate contacts exist between the TSV and the victim node, switching noise is significantly less as compared to Fig. 9(a) and is further reduced as d_2 decreases, *i.e.*, the number of substrate contacts increases. Also note that in both figures, switching noise due to via-last TSVs is significantly greater than via-first TSVs since the diameter is larger and height is longer.

Peak-to-peak switching noise at the victim transistor is shown in Fig. 9(c) and (d) as a function of d_1 when d_2 is constant at 4 μm. As illustrated in Fig. 9(c), when only a single substrate contact exists, placing the victim transistor farther from the switching TSV is an effective method for via-first TSVs. Alternatively, for via-last TSVs, the noise exhibits low sensitivity to the distance between TSV and victim transistor. This phenomenon is due to longer height (therefore smaller substrate resistances) and larger diameter (therefore larger capacitances) of via-last TSVs.

According to Fig. 9(d), when multiple substrate contacts are regularly placed, increasing the physical distance between the switching TSV and the victim transistor is helpful for both via-first and via-last TSVs. In this case, the effective impedance between the TSV and the ground node becomes significantly lower since the number of substrate contacts increases as d_1 is increased.

5.2. Slew rate of the TSV signal

Slew rate of a signal within a TSV not only affects the circuit speed and power consumption, but also TSV induced noise coupling into the substrate. Specifically, the transient characteristics of a TSV signal determine the frequency range of interest and therefore the coupling strength between the TSV and a victim transistor. In this analysis, slew rate is varied by changing the rise/fall time of a transient signal applied to a TSV, as shown in Fig. 5. Each of the four cases described in the previous section is

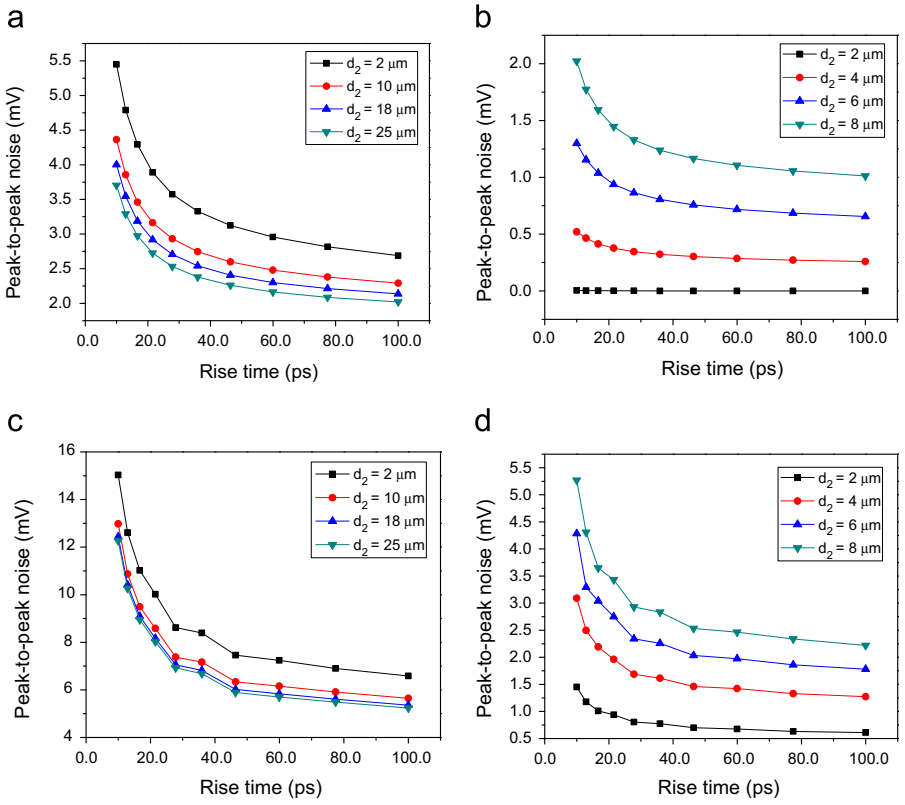

Fig. 10. TSV induced switching noise at the victim node as a function of rise time: (a) case 1: via-first TSV with a single substrate contact, (b) case 2: via-first TSV with regularly placed substrate contacts, (c) case 3: via-last TSV with a single substrate contact, and (d) case 4: via-last TSV with regularly placed substrate contacts.

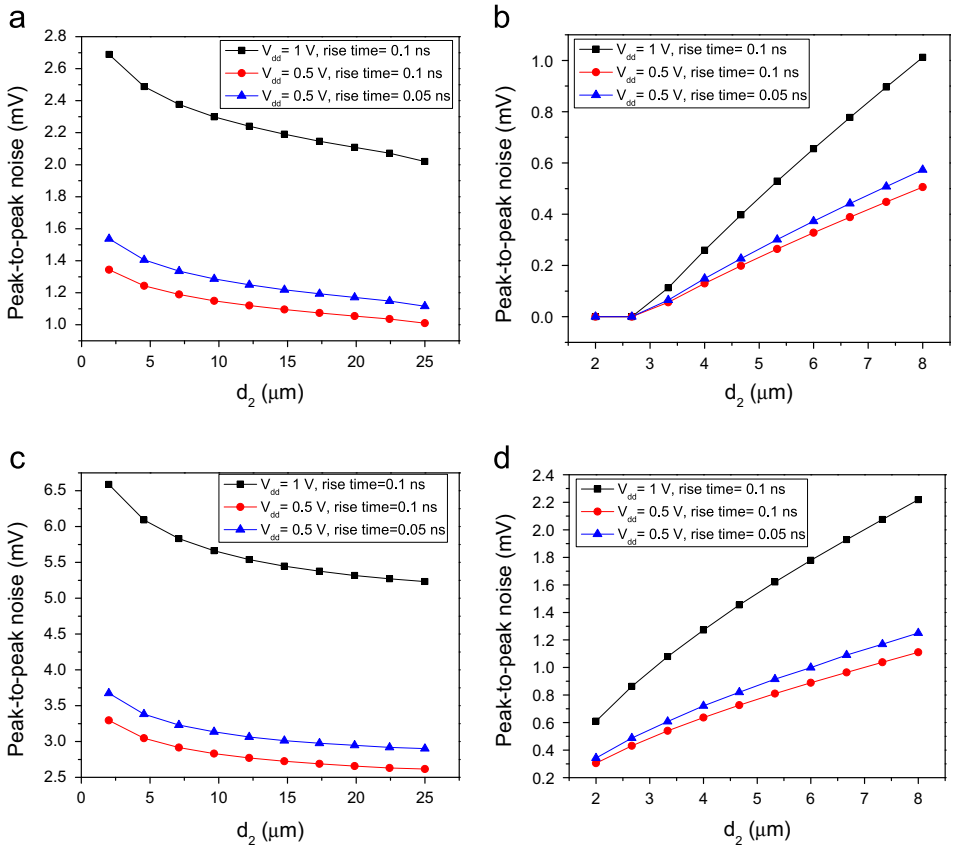

Fig. 11. TSV induced switching noise at the victim node at different voltage swings and rise times: (a) case 1: via-first TSV with a single substrate contact, (b) case 2: via-first TSV with regularly placed substrate contacts, (c) case 3: via-last TSV with a single substrate contact, and (d) case 4: via-last TSV with regularly placed substrate contacts.

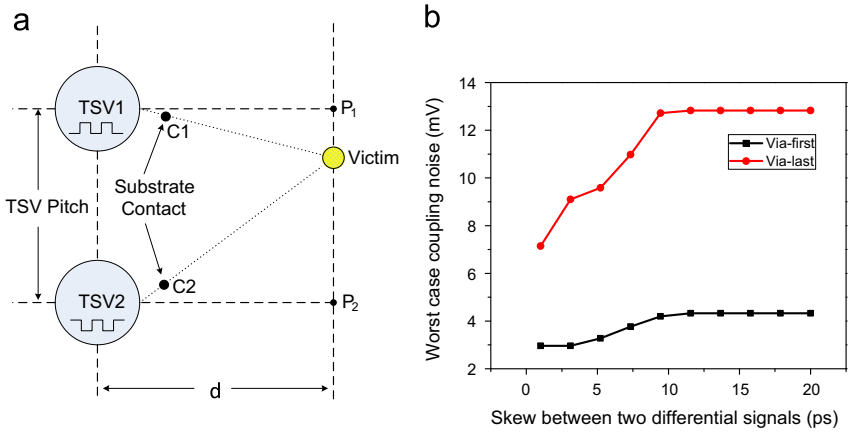

Fig. 12. Effect of differential signaling on TSV related noise coupling: (a) analysis setup and (b) noise at the victim node as a function skew between the two signals.

considered. In each case, four typical values of d_2 (distance between TSV and substrate contact in cases 1 and 3, distance between two substrate contacts in cases 2 and 4) are chosen based on the results obtained in the previous section. The voltage swing of the transient signal is constant at 1 V while d_1 (distance between TSV and victim node) is constant at 30 μm. The rise time varies from 10 ps to 100 ps.

As demonstrated in Fig. 10, a significant initial reduction in noise is achieved when the rise time increases from 10 ps to approximately 30 ps. For example, in case 1 where a via-first TSV and a single substrate contact exist, if the rise time of the transient signal increases from 10 ps to 30 ps, the peak noise is reduced by 34.4%, 32.7%, 32.2%, and 31.6% when d_2 (distance between TSV and substrate contact) is, respectively, 2 μm, 10 μm, 18 μm, and 25 μm. Similar reduction in noise is also observed for a via-last TSV. In regularly placed substrate contacts (cases 2 and 4), the effect of rise time is weaker as the number of substrate contacts increases.

5.3. Voltage swing of the TSV signal

Another parameter that affects the TSV power, delay, and noise characteristics is the voltage swing. Low swing TSVs reduce both power consumption and delay since the oxide and depletion capacitances require less charge. Noise coupling into the substrate is also reduced due to weaker dv/dt. Since the voltage swing and slew rate are interdependent, three configurations are investigated: (1) $V_{dd}=1$ V, rise time$=100$ ps, (2) $V_{dd}=0.5$ V, rise time$=100$ ps, and (3) $V_{dd}=0.5$ V, rise time$=50$ ps. d_1 (distance between TSV and victim node) remains constant at 30 μm. The simulation results for each case are shown in Fig. 11.

If the voltage swing is reduced from 1 V to 0.5 V, while the slew rate is the same (rise time is proportionally reduced), peak noise at the victim node is reduced by over 40% for case 1. If the voltage swing remains at 0.5 V and the rise time is increased from 50 ps to 100 ps, peak noise is reduced by an additional 10%. The other three cases exhibit a similar pattern. Thus, if the rise time of a TSV signal is above a certain threshold ($\approx$30 ps), reducing the voltage swing is a more effective method to reduce TSV induced noise than increasing the transition time.

5.4. Differential TSV signaling

An active substrate noise reduction method has been proposed in [30] where the phase of the noise is reversed and reinjected into the substrate, producing up to 83% reduction in noise. A similar result can be achieved in TSV related noise coupling through differential signaling, as investigated in this section. For example, differential clocking can significantly reduce the effective noise injected into the substrate by the TSVs. The proposed compact model is used to evaluate this behavior. As shown in Fig. 12(a), two TSVs carrying out-of-phase signals are placed on the substrate where the distance between the TSVs is equal to the minimum pitch (8 μm for via-first and 20 μm for via-last). Distance between each TSV and points P_1 and P_2 (d in the figure) is 30 μm. Worst case noise between points P_1 and P_2 is observed as a function of skew between the two out-of-phase TSV signals. This noise is plotted in Fig. 12(b). Note that the effect of substrate contact C1 on TSV2 and the effect of C2 on TSV1 are neglected since the model cannot consider contacts placed outside the trajectory between TSV and victim. This assumption is valid if pitch is sufficiently greater than the distance between TSV and substrate contact. In practice, noise at the victim node is expected to be slightly lower than the estimated value since C1 can filter a small amount of noise that originates from TSV2. The analysis therefore provides a pessimistic estimation.

According to Fig. 12(b), the efficiency of differential signaling in reducing TSV related noise is strongly dependent upon the skew between the two out-of-phase signals. If the two signals are almost exactly out-of-phase (1 ps skew), differential signaling achieves 32.1% and 44.9% reduction in peak noise, respectively, for via-first and via-last TSVs. However, when the skew reaches approximately 10 ps, the advantage of differential signaling diminishes. Thus, emphasis should be placed on ensuring small skew if differential signaling is utilized to cancel TSV related noise coupling in 3D ICs.

6. Conclusions

TSV-to-transistor noise coupling has been evaluated and quantified in 3D ICs. A compact π model has been proposed to estimate noise at a victim transistor as a function of different substrate biasing schemes (single substrate contact and multiple regularly placed substrate contacts) and TSV fabrication methods (via-first and via-last). A closed-form expression has been developed to approximate each admittance within the π model with a logarithmic function. Both the compact model and the closed-form expression have been validated using a 3D transmission line matrix method with an average error of 4.8%. These expressions and the model have been utilized to better understand the effect of different design parameters on noise for both via-first and

via-last TSVs, such as substrate contact placement, slew rate and voltage swing of the TSV signals, and differential TSV signaling.

Future work includes extending the proposed models to a chip-scale analysis where the effect of multiple TSVs is accurately considered. Since a substrate contact may filter noise originating from multiple TSVs, an effective range should be determined to identify those contacts that need to be considered for each TSV. Similarly, an effective range should be determined to identify those TSVs that help in shielding noise for an aggressor TSV. Under these geometric rules, the contribution of each TSV to a victim node should be characterized using analytic models, similar to those proposed in this paper.

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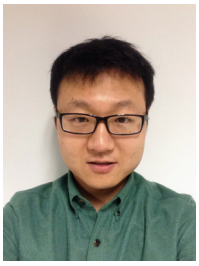

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