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Utilizing interdependent timing constraints to enhance robustness in synchronous circuits

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ABSTRACT

Interdependent setup-hold times are exploited during the design process to improve the robustness of a circuit. Considering this interdependence only during static timing analysis (STA), as demonstrated in the previous work, is insufficient to fully exploit the capabilities offered by interdependence. This result is due to the strong dependence of STA results on the specific circuit, cell library, and operating frequency. Interdependence is evaluated in this paper for several technologies to determine the overall reduction in delay uncertainty rather than improvements in STA. Reducing delay uncertainty produces a more robust synchronous circuit. The increasing efficacy of interdependence in deeply scaled technologies is also demonstrated by investigating the effect of technology scaling on interdependent timing constraints.

1. Introduction

Cell library characterization is a critical step in static timing analyses (STA) of large scale integrated circuits [1,2]. Since an STA tool relies on the data described in these libraries to analyze the timing characteristics of a circuit, the overall accuracy of STA is strongly dependent upon the accuracy of cell library characterization.

The setup and hold times, *i.e.*, timing constraints, of a sequential cell play a critical role in the timing analysis process since these timing constraints are used to determine whether a circuit can properly operate at the required clock frequency. Previous work has shown that the setup-hold times and clock-to-Q delay of a sequential cell are *interdependent* [3,4]. An *independent* characterization process may produce either optimistic or overly pessimistic STA results. Both cases should be avoided as the optimistic case can cause a circuit to fail whereas the pessimistic case unnecessarily degrades circuit speed.

One of the challenges in interdependent characterization of timing constraints is computational complexity since each sequential cell in a library should be extensively simulated to obtain the *clock-to-Q delay surface* [3]. The computational efficiency of interdependent setup-hold time characterization has been improved through state transition [5,6]. Interdependent setup-hold times have also been exploited in statistical static timing analysis (SSTA) processes [7].

While the need for interdependent characterization and using these interdependent timing constraints within the STA process have been well understood [3–7], the significance of interdependence in advanced technologies and the scaling characteristics of interdependent timing constraints have not been investigated. A disadvantage of relying only on STA is the inability to accurately evaluate the significance of interdependence. Specifically, the results presented in [3] strongly depend upon the specific circuit and clock frequency. For example, while interdependence can significantly reduce timing violations in one circuit, interdependence may not be as efficient in another circuit with the same technology, producing inconsistent results.

A different approach is proposed in this paper where the ability of the interdependence to tolerate variations [8,9] and reduce delay uncertainty (thereby enhance robustness) is investigated rather than improving timing analysis. This approach provides a more complete understanding of the efficacy of interdependence. Furthermore, the evolution of interdependence with process technology is also investigated to determine the effects of scaling on these interdependent timing constraints. The result has practical importance to understand whether the additional complexity required to characterize interdependent timing constraints is worth the effort in deep submicrometer technologies.

The rest of the paper is organized as follows. Background material reviewing the timing characteristics of a circuit and setup-hold interdependence is provided in Section 2. The problem

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is formulated in Section 3. A procedure to reduce delay uncertainty and compensate for variations is described in Section 4. A case study is presented in Section 5 to evaluate the significance of setup-hold interdependence to compensate for power supply and threshold voltage variations for four technology generations. Finally, the paper is concluded in Section 6.

2. Background

The timing characteristics of synchronous circuits are reviewed in Section 2.1. Interdependent setup-hold times are summarized in Section 2.2.

2.1. Timing characteristics of synchronous circuits

A simple synchronous digital circuit consisting of two sequentially-adjacent registers with a combinational circuit between these registers is shown in Fig. 1. Two inequalities should be satisfied for this circuit to function properly. Referring to Fig. 1, the first inequality is

$$T_{Cf}+T_{CP} \geq T_{Ci}+T_D+T_S, \tag{1}$$

where T_{Ci} and T_{Cf} are the delay for the clock signals to arrive, respectively, at the *initial* and *final* registers. Note that T_{Ci} and T_{Cf} are also referred to as, respectively, the delay of the clock launch path and clock capture path. T_{CP} is the clock period, T_D is the data path delay consisting of the clock-to-Q delay of the initial register, logic delay of the combinational circuit, and the interconnect delay. T_S is the setup time of the final register. Note that (1) determines the maximum speed of the circuit, making this inequality important for the critical paths within a circuit.

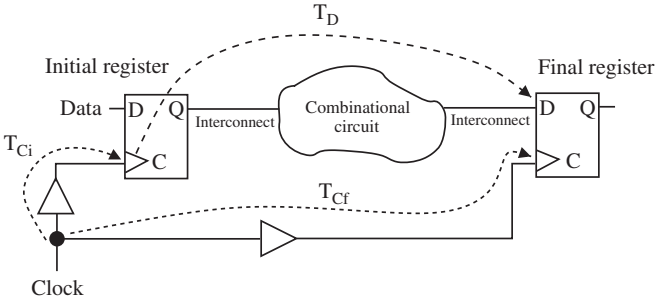

Fig. 1. Simple synchronous circuit consisting of a combinational logic and two registers.

The second inequality that needs to be satisfied is

$$T_{Ci}+T_D \geq T_{Cf}+T_H, \tag{2}$$

where T_H is the hold time of the final register. This inequality guarantees that no race condition exists, *i.e.*, the data are not latched within the final register during the same clock edge. Note that (2) is relatively more important for those timing paths where the data path delay is sufficiently small, such as a shift register or counter.

2.2. Interdependent setup-hold times

Inequalities (1) and (2) require a difference called a *skew* to be larger than or equal to a number called a *timing constraint*. These inequalities, therefore, can be rewritten as

$$\text{Setup skew} \geq T_S, \tag{3}$$

$$\text{Hold skew} \geq T_H, \tag{4}$$

where setup skew and hold skew are, respectively,

$$\text{Setup skew} = T_{Cf}+T_{CP}-(T_{Ci}+T_D), \tag{5}$$

$$\text{Hold skew} = T_{Ci}+T_D-T_{Cf}. \tag{6}$$

Note the important difference between setup-hold skews and setup-hold times: setup and hold skews refer to *any* time difference between the data and clock signals whereas the setup and hold times refer to the minimum required time difference to reliably capture and store the data. Also note that the difference between the left and right hand sides of (3), *i.e.*, (setup skew—T_S) is referred to as *setup slack*. Similarly, (hold skew—T_H) is referred to as *hold slack*. A negative slack therefore corresponds to a timing violation whereas a positive slack corresponds to available timing margin.

Existing approaches to characterize the timing constraints of a register, *i.e.*, setup and hold times in (1) and (2), assume these timing constraints are independent [10]. This independent characterization produces overly pessimistic results since the setup-hold times are, in reality, interdependent [3]. An example of an interdependent setup-hold contour curve obtained from a clock-to-Q delay surface at a constant delay is illustrated in Fig. 2 [4].

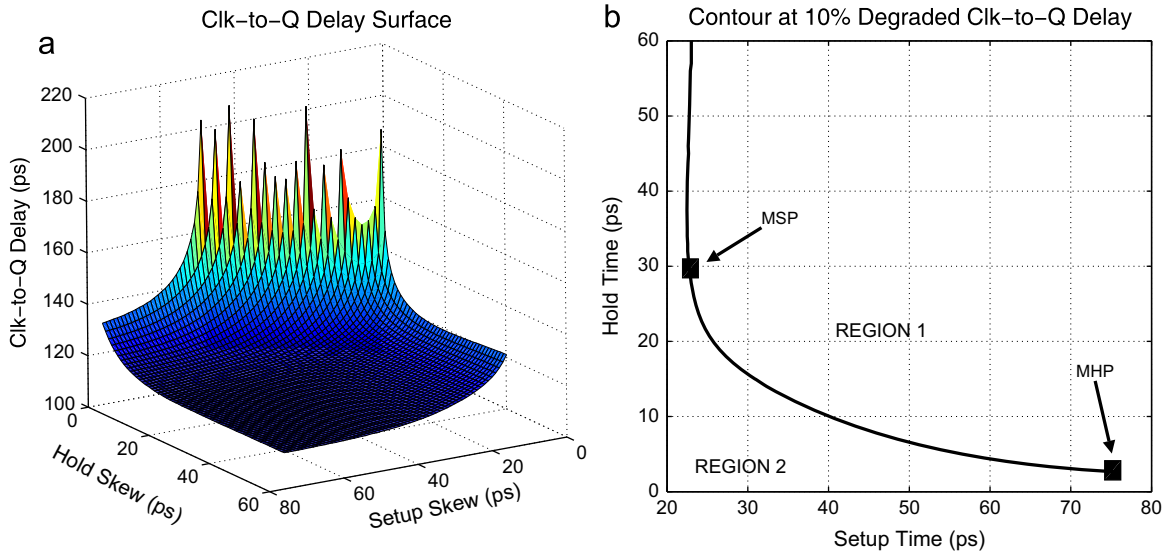

Fig. 2. Interdependent setup-hold time characterization: (a) clock-to-Q delay surface as a function of independently varying setup skew and hold skew and (b) the contour at 10% degraded clock-to-Q delay.

In Fig. 2(a), the clock-to-Q delay is obtained as a function of independently varying setup skew and hold skews. Those setup and hold skews corresponding to a specific per cent degradation in clock-to-Q delay are extracted from this surface, representing a contour curve. Each (setup, hold) pair on this contour curve shown in Fig. 2(b) is a valid pair for the register. Multiple timing constraints therefore exist rather than a single setup and hold time. As indicated in Fig. 2(b), a small setup time can be obtained at the expense of a large hold time. Similarly, a small hold time can be obtained at the expense of a large setup time. For example, *minimum setup pair* (*MSP*) and *minimum hold pair* (*MHP*) refer, respectively, to a pair on the contour with the minimum setup time and minimum hold time. Also note that any pair in region 1 is also valid with additional pessimism, whereas any pair in region 2 is invalid, as the pairs in this region are optimistic.

Previous work has primarily focused on the effect of interdependent setup-hold pairs on timing analysis [3,4,7] and characterization aspects of interdependence [5,6]. Considering only STA results, however, is insufficient to fully understand the capabilities of interdependence. Interdependent setup-hold times not only reduce pessimism in timing analysis, but also provide an opportunity to improve the tolerance of a circuit to process and environmental variations. Investigating interdependence from this perspective provides a more realistic understanding of interdependent timing constraints. Furthermore, the effect of technology scaling on interdependent setup-hold pairs is also investigated, demonstrating the increasing significance of interdependence in deeply scaled technologies.

3. Problem formulation

The contour curve illustrated in Fig. 2(b) can be approximated as a linear line using two critical pairs: *MSP* and *MHP*. This approximation is further described in Section 4.1. An approximation of the contour using two critical pairs is illustrated in Fig. 3 where the pairs *MSP* and *MHP* are represented, respectively, as $(T_{S,min}, T_{H,max})$ and $(T_{S,max}, T_{H,min})$.

According to (1) and (2) and referring to Fig. 1, the delay of the data path should satisfy

$$T_{Cf}+T_H-T_{Ci} \le T_D, \tag{7}$$

$$T_D \le T_{Cf}+T_{CP}-(T_{Ci}+T_S), \tag{8}$$

where (7) and (8) determine, respectively, the lower and upper bounds of the data path delay.

Characterization of the setup and hold times affects the design process by constraining the data path delay T_D. The allowable range of T_D is minimized if the pessimistic pair $(T_{S,max}, T_{H,max})$ is used, causing the circuit to be overdesigned. Which specific (setup, hold) pair should be chosen to design the circuit is unclear even if the interdependence is known since multiple valid pairs are available. For example, if the pair $(T_{S,min}, T_{H,max})$ is used, the lower bound constraint of the data path delay is difficult to satisfy since the hold time is large. Hence, the data path delay should be increased by inserting additional stages, dissipating unnecessary power. Alternatively, if the pair $(T_{S,max}, T_{H,min})$ is used, the upper bound constraint on the data path delay is difficult to satisfy since the setup time is large. Consequently, the data path delay should be lowered by inserting an additional register to satisfy the target frequency, also causing unnecessary power consumption. Furthermore, both pairs $(T_{S,min}, T_{H,max})$ and $(T_{S,max}, T_{H,min})$ exhibit low tolerance to process and environmental variations since the range of valid setup times $T_{S,max}-T_{S,min}$ and hold times $T_{H,max}-T_{H,min}$ is not exploited.

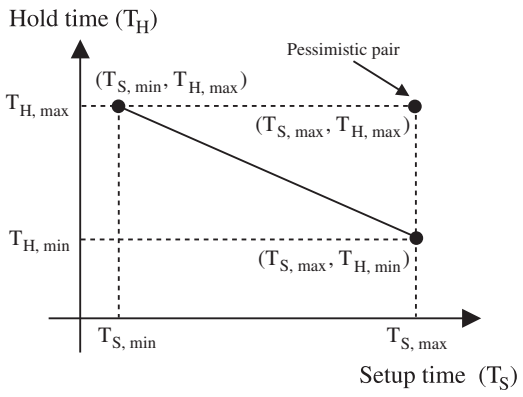

Fig. 3. Linear approximation of the contour curve using two pairs: $(T_{S,min}, T_{H,max})$ and $(T_{S,max}, T_{H,min})$.

It is therefore important to determine the appropriate (setup time, hold time) pair during the design process that lowers power consumption, satisfies the required delay, and increases the robustness of the circuit to achieve a higher tolerance to process and environmental variations. This procedure exploits interdependence to reduce delay uncertainty, as described in the following section.

4. Reducing delay uncertainty

A characterization technique to determine the critical pairs *MSP* and *MHP* is introduced in Section 4.1. A procedure to reduce delay uncertainty and compensate for variations is described in Section 4.2. The effect of variations on the interdependent characterization process is discussed in Section 4.3. The amount of compensation achieved by the proposed technique is determined in Section 4.4.

4.1. Obtaining linear setup-hold relationship

The first step to reduce delay uncertainty is to obtain a relationship between setup-hold times of a register. A piecewise linear approximation of the setup-hold contour exhibits a tradeoff between computational complexity and the amount of pessimism. A two-point approximation is achieved in this work to demonstrate the effectiveness of setup-hold interdependence in reducing delay uncertainty, even with this relatively simple approximation. Note that this approximation is valid due to two reasons: (1) any point above the curve, *i.e.*, in region 1, is a valid pair with some pessimism since the curve is convex, and (2) part of the curve between *MSP* and *MHP* represents a monotonically decreasing function. Additional points on the curve reduce pessimism at the expense of additional computational complexity. Note that both the convexity and monotonicity of the contour curve have been observed for each analysis, provided that an edge-triggered, master-slave type D flip–flop is used as a register. The sizing and process technology do not change this characteristic. Note however that the evaluation of setup-hold relationship for different flip–flop architectures and latches remains as future work.

An efficient, two-point approximation technique is described in this section. Note that additional points require the generation of the entire clock-to-Q delay surface, significantly increasing the computational time due to additional simulations. Furthermore, the number of linear equations characterizing the setup-hold relationship also increases. Referring to Fig. 3, the four points defining *MSP* and *MHP*, *i.e.*, $T_{S,min}$, $T_{H,max}$, $T_{H,min}$, and $T_{S,max}$, are

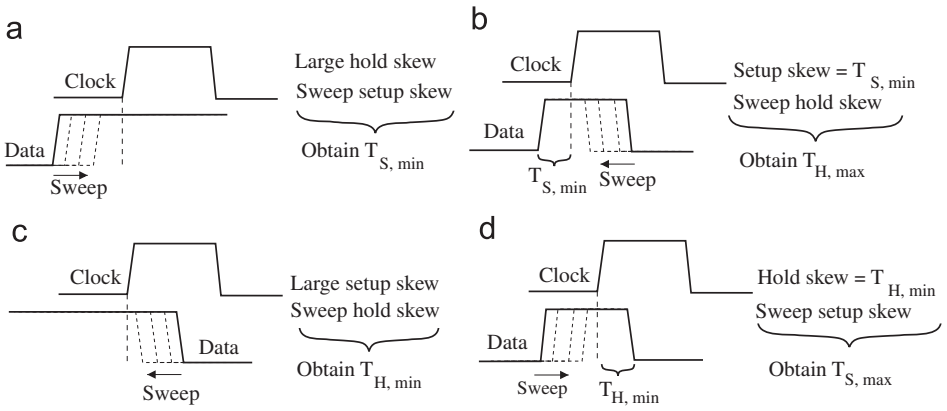

Fig. 4. Efficiently obtaining the critical setup-hold pairs of a register without generating a three-dimensional clock-to-Q delay surface: (a) $T_{S,min}$, (b) $T_{H,max}$, (c) $T_{H,min}$, (d) $T_{S,max}$.

obtained as follows where the corresponding waveforms of the clock and data signals are illustrated in Fig. 4.

- $T_{S,min}$: the clock-to-Q delay of a register is determined as a function of setup skew at a sufficiently high hold skew. The setup skew corresponding to a 10% degradation in delay is chosen as $T_{S,min}$.
- $T_{H,max}$: the clock-to-Q delay of a register is determined as a function of hold skew at *setup skew* $= T_{S,min}$. The hold skew corresponding to a 10% degradation in delay is chosen as $T_{H,max}$.
- $T_{H,min}$: the clock-to-Q delay of a register is determined as a function of hold skew at a sufficiently high setup skew. The hold skew corresponding to a 10% degradation in delay is chosen as $T_{H,min}$.
- $T_{S,max}$: the clock-to-Q delay of a register is determined as a function of setup skew at *holdskew* $= T_{H,min}$. The setup skew corresponding to a 10% degradation in delay is chosen as $T_{S,max}$.

The linear relationship between the setup and hold times can be represented by the critical pairs as $T_H = f(T_S)$ or, equivalently, $T_S = f^{-1}(T_H)$

$$T_H = f(T_S) = \frac{T_S T_{H,r} - T_{H,max} T_{S,max} + T_{H,min} T_{S,min}}{-T_{S,r}}$$

$$\text{for } T_{S,min} < T_S < T_{S,max}, \tag{9}$$

where the range of valid setup times $T_{S,r}$ and hold times $T_{H,r}$ are, respectively,

$$T_{S,r} = T_{S,max} - T_{S,min}, \tag{10}$$

$$T_{H,r} = T_{H,max} - T_{H,min}. \tag{11}$$

4.2. Procedure to reduce delay uncertainty

For a critical path, an increase in the delay of a data path ΔT_D due to variations causes the frequency to be decreased to satisfy (8). This increase in the data path delay produces additional hold slack in (7). This additional slack in the hold skew can be exploited to increase the hold time in (7) by ΔT_{Hold} where $\Delta T_{Hold} = \Delta T_D$. An increase in the hold time enables a decrease in the setup time by $\Delta T_S = f^{-1}(\Delta T_H)$ due to the interdependence, as illustrated in Fig. 3. The effect of the variation, *i.e.*, the decrease in frequency, can therefore be compensated by exploiting a lower setup time.

Similarly, for a timing path sensitive to a race condition, referred to as a *short path*, a decrease in the delay of the data path by ΔT_D can cause a hold time violation. Since the delay of the data path is reduced, any additional setup slack in (8) can be exploited by increasing the setup time by ΔT_S where $\Delta T_S = \Delta T_D$. An increase in the setup time supports a decrease in the hold time by $\Delta T_H = f(\Delta T_S)$, potentially resolving the violation. The delay uncertainty due to a variation is therefore reduced by exploiting interdependent setup-hold times. This procedure is summarized in the flowchart depicted in Fig. 5.

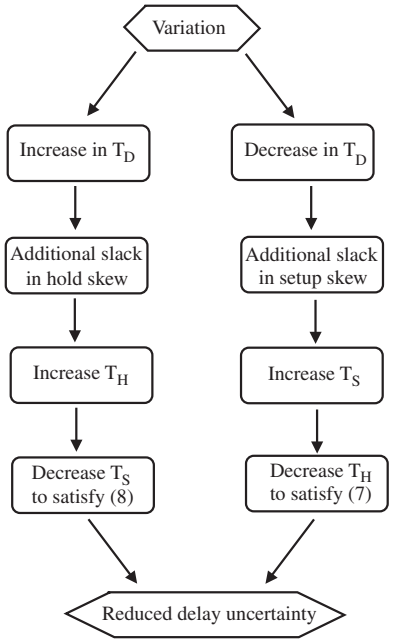

Fig. 5. Flow diagram to reduce delay uncertainty by exploiting interdependent setup-hold times.

Note that the variation in the delay of the clock launch path ΔT_{Ci} and clock capture path ΔT_{Cf} is assumed in this approach to be equal. For those cases where this assumption is not accurate, the variation in the delay of the clock path may either enhance or degrade the delay uncertainty depending upon the sign of $\Delta T_{Cf} - \Delta T_{Ci}$, as described in Section 4.4.

Another consideration for this procedure is the effect of variations on the interdependent setup-hold characteristics. This variation in the critical setup-hold pairs is sufficiently low as compared to the range of valid setup times and hold times, enabling the proposed procedure. This behavior is further described in the following subsection.

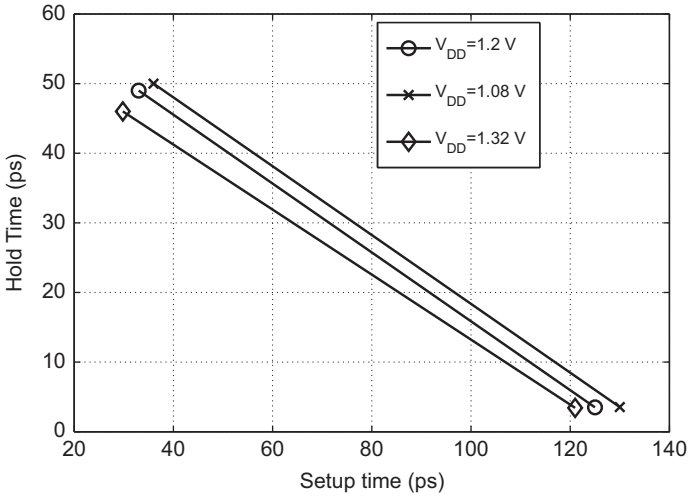

Fig. 6. Variation of interdependent setup-hold characteristics as a function of the power supply voltage for a 90 nm CMOS technology.

4.3. Setup-hold time characterization under variations

Process and environmental variations can also affect the critical pairs of a register, *i.e.*, $T_{S,min}$, $T_{H,max}$, $T_{S,max}$, and $T_{H,min}$. The effect of a variation on these critical pairs, however, is sufficiently small as compared to the range of valid setup times $T_{S,r}$ and hold times $T_{H,r}$. This behavior is primarily due to a stronger dependence of the clock-to-Q delay on the setup skew and hold skew when these skews are reduced [3]. For example, at a critical pair ($T_{S,min}$,$T_{H,max}$), the clock-to-Q delay is primarily determined by $T_{S,min}$, lowering the effect of process and environmental variations on this pair. Similarly, at a critical pair ($T_{S,max}$,$T_{H,min}$), $T_{H,min}$ has a relatively greater effect on the clock-to-Q delay.

To further illustrate this behavior, critical pairs are obtained for different power supply voltages in a 90 nm CMOS technology where the power noise is the source of the variation, as depicted in Fig. 6. The maximum variation in the power supply is assumed to be 10% of the nominal voltage. The variation in the critical pairs is compared with the range of valid setup and hold times. Specifically, the variation in the critical pairs caused by a 10% increase or decrease in the power supply voltage is listed, respectively, in Tables 1 and 2. As listed in these tables, $T_{S,r}$ and $T_{H,r}$ are sufficiently higher than the variation of the critical pairs, making interdependence an effective mechanism to reduce delay uncertainty.

4.4. Amount of compensation

The compensation in delay variation (or the reduction in delay uncertainty) is dependent upon three primary factors: (a) the range of the valid setup times $T_{S,r}$ and hold times $T_{H,r}$, (b) the specific (setup, hold) pair used in (7) and (8) to determine the data path delay, and (c) the effect of the variations on the clock launch and capture paths, *i.e.*, the clock distribution network.

If a register has a greater range of valid setup times and hold times, this register is more effective in reducing delay uncertainty. Note however that this type of register may exhibit other tradeoffs such as higher power consumption and clock-to-Q delay. Evaluation of different register architectures for setup-hold interdependence remains as a future work.

As described in Section 3, the specific (setup, hold) pair used to determine the data path delay can lower the power consumption while satisfying the target frequency and achieving a higher tolerance to variations. The middle point of the setup-hold line ($T_{S,mid}$, $T_{H,mid}$) results in a highest tolerance since the setup and hold times exhibit the maximum flexibility to variations, as illustrated in Fig. 7. Note that in this case, the data path should be designed to ensure that the delay of the data path satisfies

Table 1
Variation of the critical pairs due to a 10% decrease in the power supply voltage. Range of valid setup times is 139 ps.

Critical points (ps)	V_{DD}=1.2 V	V_{DD}=1.08 V	Variation (ps)
$T_{S,min}$	33	36	3
$T_{H,max}$	49	50	1
$T_{S,max}$	125	130	5
$T_{H,min}$	3.5	3.54	0.04
$T_{S,r}$	92	94	2
$T_{H,r}$	45.5	46.5	1

Table 2
Variation of critical pairs due to a 10% increase in the power supply voltage. Range of valid hold times is 54 ps.

Critical points (ps)	V_{DD}=1.2 V	V_{DD}=1.32 V	Variation (ps)
$T_{S,min}$	33	29.8	3.2
$T_{H,max}$	49	46	3
$T_{S,max}$	125	121	4
$T_{H,min}$	3.5	3.43	0.07
$T_{S,r}$	92	91.2	0.8
$T_{H,r}$	45.5	42.57	2.93

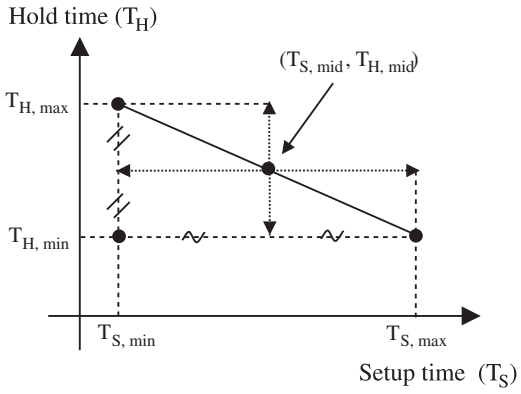

Fig. 7. A data path designed at the pair ($T_{S,mid}$,$T_{H,mid}$) achieves the highest tolerance to variations.

both (7) and (8), specifically when the setup time and hold time are, respectively, $T_{S,mid}$ and $T_{H,mid}$. This technique is analogous to clock skew optimization techniques proposed in the mid 1990s where the circuit is designed at the middle of the clock skew range among possible skew values (referred to as the permissible range) to maximize the tolerance of a circuit to variations [11,12].

The amount of variation tolerated by this methodology is also dependent upon the variation in the delay of the clock launch path ΔT_{Ci} and clock capture path ΔT_{Cf}. Specifically, if $\Delta T_{Ci} = \Delta T_{Cf}$, *i.e.*, constant clock skew, these variations compensate. In this case, the variation in the delay of the clock paths does not affect the amount of tolerance. If however $\Delta T_{Ci} > \Delta T_{Cf}$, less variation can be tolerated by a critical path since the delay of the clock launch path is increased, delaying the data signal from leaving the register. For a short path, however, additional variation can be tolerated. Alternatively, if $\Delta T_{Cf} > \Delta T_{Ci}$, additional variation can be tolerated for a critical path since the clock launch path is relatively faster than the clock capture path. For a short path, however, less variation can be tolerated.

The significance of interdependence in enhancing the robustness can also be understood by investigating the permissible range. The relationship between interdependent timing constraints and permissible range is described in the following section.

4.5. Permissible range and interdependence

A *permissible range* has been defined that describes the valid range of clock skew $T_{Ci}-T_{Cf}$ [13,12]. Rearranging (7) and (8), the clock skew should satisfy

$$T_H - T_D \le T_{Ci} - T_{Cf}, \tag{12}$$

$$T_{Ci} - T_{Cf} \le T_{CP} - T_D - T_S, \tag{13}$$

where the lower and upper bounds of the clock skew are determined, respectively, by (12) and (13). The permissible range T_{perr} of the clock skew is determined by the difference between the upper and lower bounds of the clock skew

$$T_{per} = T_{CP} - (T_S + T_H). \tag{14}$$

A methodology to tolerate skew variations by exploiting this permissible range has also been previously described [11]. According to (14), a smaller setup and hold time is desirable to increase the permissible range. Assuming that the circuit is designed at the middle of the permissible range, a higher range provides increased tolerance to variations.

Interdependent timing constraints provide additional flexibility to modify the permissible range. Specifically, the lower and upper bounds of the clock skew change depending upon the specific (setup, hold) pair, as illustrated in Fig. 8. For example, if the pair ($T_{S,min}$,$T_{H,max}$) is used, the permissible range shifts to the right since both bounds increase. In this case, the upper bound of the permissible range is greater. Alternatively, if the pair ($T_{S,max}$,$T_{H,min}$) is used, the permissible range shifts to the left since both bounds decrease, as shown in Fig. 8. In this case, the lower bound of the permissible range is smaller. The interdependence of the setup and hold times therefore provides additional flexibility in exploiting the permissible range to tolerate variations. Clock skew scheduling in the presence of interdependent setup-hold times remains as a future work.

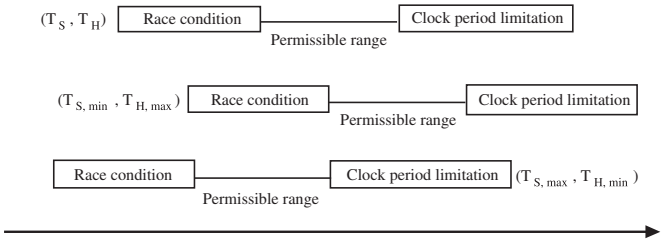

Fig. 8. Exploiting interdependent setup and hold times within a permissible range of the clock skew. A shift in the permissible range is achieved. This shift is dependent upon the specific (setup, hold) pair, providing additional flexibility to tolerate variations, thereby enhancing robustness.

5. Case study

The efficacy of setup-hold time interdependence to compensate power supply and threshold voltage variations is evaluated in this section. Note that power supply noise and threshold voltage variations are considered here as an example to demonstrate the significance and utility of the setup-hold interdependence [14]. Other factors that introduce delay uncertainty such as temperature variations can also be considered to evaluate the significance of setup-hold interdependence [15].

Four CMOS technology generations are considered: 180 nm, 90 nm, 65 nm, and 45 nm. An industrial model is used for the 180 nm, 90 nm, and 65 nm CMOS technologies. For the 45 nm CMOS technology, a predictive model is used [16,17]. Two clock frequencies are considered for each technology based on the data published in [18], as illustrated in Fig. 9. Higher frequencies represent the upper bound on the frequency while the lower frequencies represent the lower bound on the frequency.

The interdependent setup-hold time characteristics for each technology is described in Section 5.1. The dependence of these characteristics on process technology is also discussed. The variation in the delay caused by the power noise and threshold voltage variations is quantified as a function of technology in Section 5.2. Finally, the efficacy of setup-hold time interdependence in tolerating this delay variation is evaluated in Section 5.3.

5.1. Interdependent T_S vs T_H relationship

A master-slave type, rising edge triggered register is used to illustrate the T_S vs. T_H relationship for each technology node. The register has been simulated to obtain the critical setup-hold pairs, where the signal transition times are assumed to be 10% of the clock period. The T_S vs. T_H relationship for each technology is

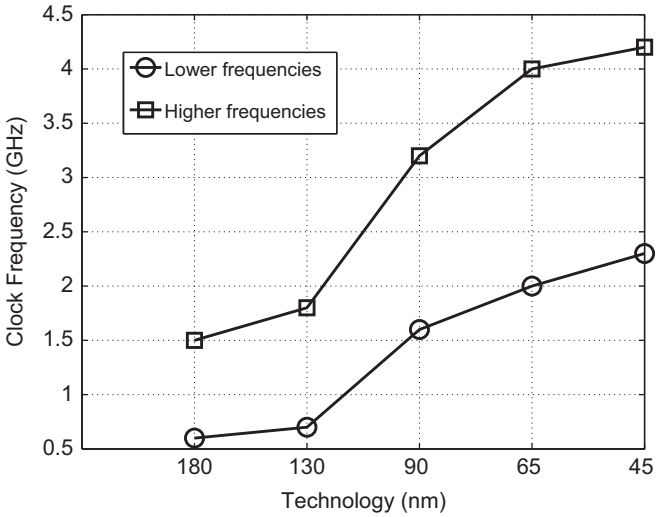

Fig. 9. Target clock frequency for each technology node. Higher frequencies represent the upper bound of the frequency while the lower frequencies represent the lower bound of the frequency.

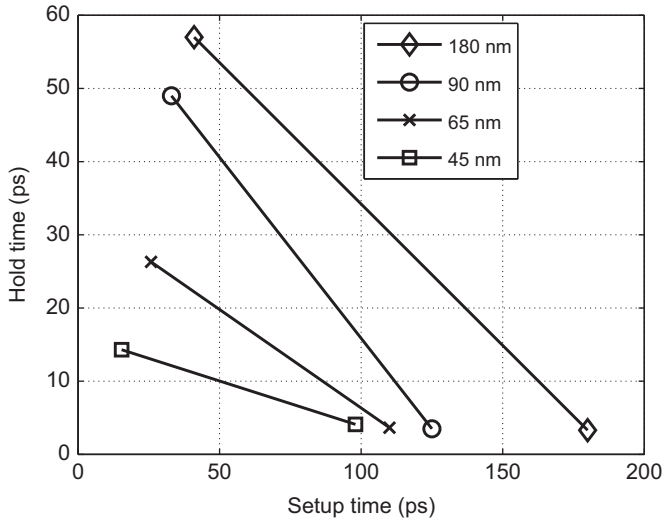

Fig. 10. Interdependent setup-hold time characteristics for four technologies.

illustrated in Fig. 10. Each line can be represented as

$$180\text{ nm}: T_H = -0.386T_S + 72.839 \text{ for } 41 \le T_S \le 180, \quad (15)$$

$$90\text{ nm}: T_H = -0.494T_S + 65.32 \text{ for } 33 \le T_S \le 125, \quad (16)$$

$$65\text{ nm}: T_H = -0.269T_S + 33.255 \text{ for } 25.8 \le T_S \le 110, \quad (17)$$

$$45\text{ nm}: T_H = -0.123T_S + 16.202 \text{ for } 15.4 \le T_S \le 98, \quad (18)$$

where each range is in picoseconds. The range of valid setup times $T_{S,r} = T_{S,max} - T_{S,min}$ and range of valid hold times $T_{H,r} = T_{H,max} - T_{H,min}$ scale with technology, as shown in Fig. 10. These critical points, clock-to-Q delay of the register, and power supply voltage are listed in Table 3 for each CMOS technology.

Note the behavior of $T_{S,r} = T_{S,max} - T_{S,min}$ (range of valid setup times) as a function of technology. The ratio of the range of valid setup times to the clock period ($T_{S,r}/T_{CP}$) increases as the technology advances, as illustrated in Fig. 11. Specifically, for the 45 nm CMOS technology, the range of valid setup times is approximately 20% of the clock period at lower frequencies. At higher frequencies, this ratio increases to 35%. The interdependence of the setup-hold times is therefore more able to tolerate variations in deep submicrometer technologies, where the difference between the maximum and minimum setup time is a significant fraction of the clock period.

5.2. Delay variation due to power noise and threshold voltage variations

The effect of power supply variations, *i.e.*, power noise, and threshold voltage variations on delay is evaluated in this section. These variations are compared with the range of valid setup times $T_{S,r}$ and hold times $T_{H,r}$, thereby determining the ability to exploit this interdependence to reduce delay uncertainty. The clock period corresponding to each technology is determined from Fig. 9. A critical path is designed for each technology to evaluate the efficacy of exploiting the interdependence relationship in compensating for a drop in the power supply voltage and an increase in the threshold voltage. A combinational circuit is inserted between the initial and final register until the delay of a data path satisfies (8).

A short path can also be generated by abutting the registers. This short path is designed to evaluate the efficacy of exploiting the interdependence relationship in compensating for an increase

Table 3
Power supply voltage, clock-to-Q delay, and critical points $T_{S,min}$, $T_{H,max}$, $T_{S,max}$, $T_{H,min}$, $T_{S,r}$, and $T_{H,r}$ for each technology.

CMOS technology (nm)	V_{DD} (V)	Clock-to-Q delay (ps)	$T_{S,min}$ (ps)	$T_{H,max}$ (ps)	$T_{S,max}$ (ps)	$T_{H,min}$ (ps)	$T_{S,r}$ (ps)	$T_{H,r}$ (ps)
180	1.8	172	41	57	180	3.3	139	53.7
90	1.2	86.4	33	49	125	3.5	92	45.5
65	1.1	57	25.8	26.3	110	3.6	84.2	22.7
45	1.0	29.8	15.4	14.3	98	4.1	82.6	10.2

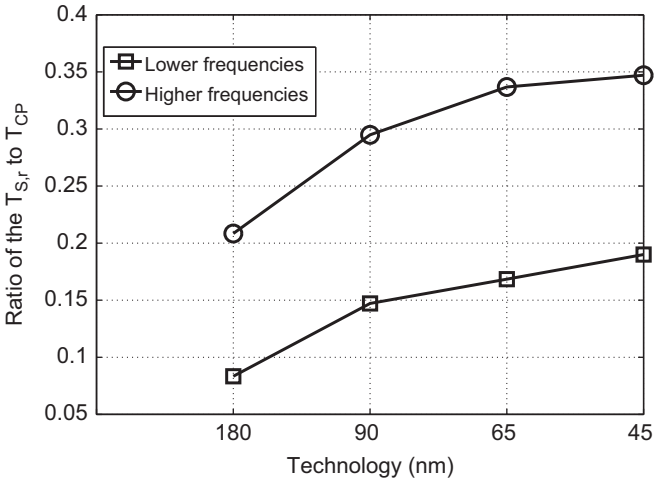

Fig. 11. Ratio of the range of valid setup times $T_{S,r}$ to the clock period T_{CP}.

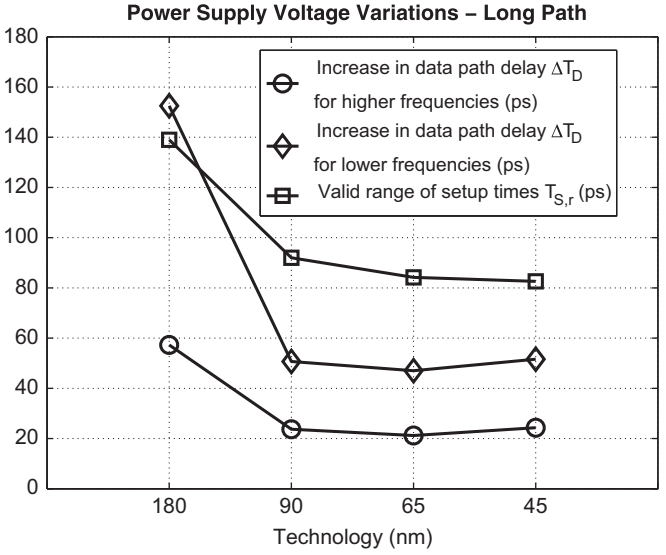

Fig. 12. Comparison of the increase in the delay of a critical data path with $T_{S,r}$ to evaluate the efficacy of exploiting the interdependence relationship. A 10% decrease in the power supply voltage is assumed.

in the power supply voltage and a decrease in the threshold voltage since both factors reduce the delay of the data path.

These long and short paths are simulated with SPICE, where the power supply voltage and threshold voltage are independently varied by 10%. Specifically, for a long path, the power supply is decreased by 10% and the threshold voltage is increased by 10%. Alternatively, for a short path, the power supply is increased by 10% whereas the threshold voltage is decreased by 10%. The corresponding variation in the delay of the data path,

including clock-to-Q delay, is determined by SPICE simulations for each technology.

For a long path, delay variations due to power supply noise and threshold voltage fluctuations are compared with the range of valid setup times $T_{S,r}$, respectively, in Figs. 12 and 13. Similarly, for a short path, delay variations are compared with the range of valid hold times $T_{H,r}$, as illustrated in Fig. 14. These figures help evaluating the efficacy of exploiting the interdependence relationship, as described in the following section.

5.3. Compensation of delay variations

As illustrated in Fig. 12, the interdependence relationship can be used to compensate for delay variations induced for power supply noise since the range of valid setup times is higher than the increase in the data path delay. The exception is the long path in 180 nm CMOS technology operating at 600 MHz. At this frequency, the delay of the data path is relatively large, causing a higher absolute variation in the delay.

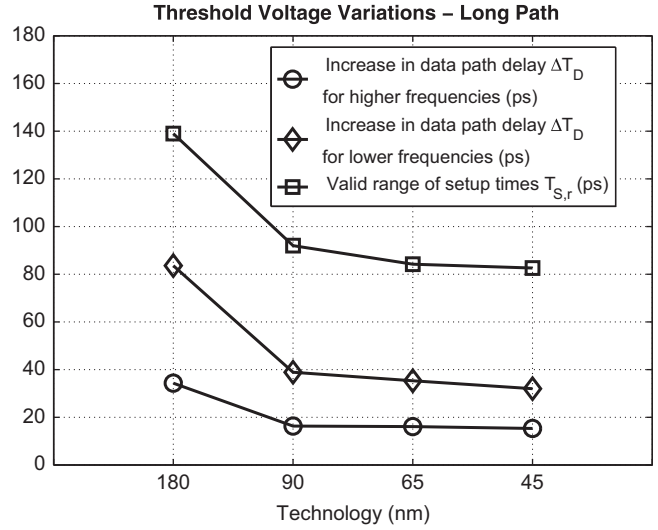

Fig. 13. Comparison of the increase in the delay of a critical data path with $T_{S,r}$ to evaluate the efficacy of exploiting the interdependence relationship. A 10% increase in the threshold voltage is assumed.

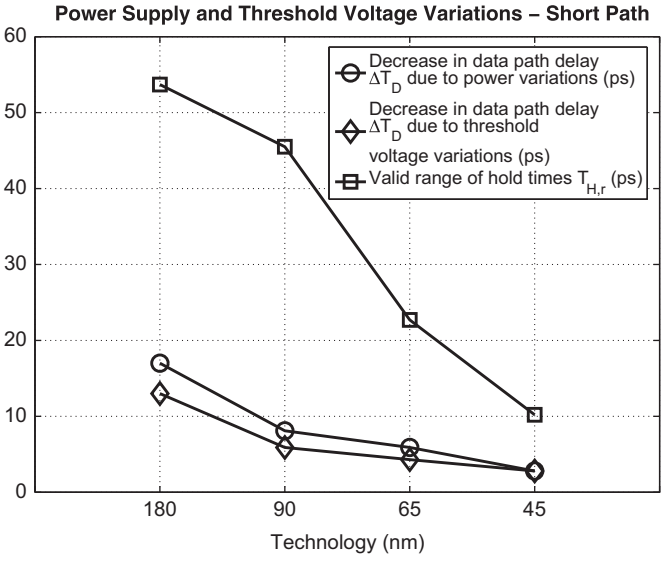

Fig. 14. Comparison of the decrease in the delay of a short path with $T_{H,r}$ to evaluate the efficacy of exploiting the interdependence relationship. Two cases are analyzed: (1) a 10% increase in the power supply voltage is assumed, (2) a 10% decrease in the threshold voltage is assumed.

If threshold voltage variations are considered, the range of valid setup times is higher than the delay variations for each technology and clock frequency, as depicted in Fig. 13. This characteristic is due to a stronger dependence of delay on power supply voltage as compared to threshold voltage.

According to both Figs. 12 and 13, the difference between the range of valid setup times and variation in delay is larger at higher frequencies since the delay of the data path is lower. Exploiting the interdependence relationship is therefore more effective in reducing the delay uncertainty of a critical path operating at higher frequencies. Also note that the absolute variation in delay due to both power supply noise and threshold voltage fluctuations somewhat saturates beyond the 130 nm technology node. This behavior is primarily due to the use of multicore processors where the increase in clock frequency is relatively low, as illustrated in Fig. 9.

For a short path, the range of valid hold times is larger than the decrease in data path delay for each technology, as illustrated in Fig. 14. This characteristic is valid for both power supply and threshold voltage variations. The difference between these two values, however, decreases for more deeply scaled technologies. For a short path, therefore, the interdependence relationship is more effective in reducing delay uncertainty in older technologies. This behavior is due to the significant decrease in the range of valid hold times with scaled technologies.

The procedure described in Section 4 has been performed on both long and short data paths. Note that these data paths are designed at the middle point ($T_{S,mid}$,$T_{H,mid}$) of the interdependent setup-hold line. For example, for the 90 nm CMOS circuit operating at 3.2 GHz, the delay of the worst case data path increases by 23.7 ps due to a drop in power supply voltage. The hold time of 26.3 ps is increased by 23.7 ps, producing a new hold time of 50 ps. Since 50 ps is larger than the maximum hold time at this technology, the hold time is increased to 49 ps. An increase in the hold time enables a decrease in the setup time from 79 ps to 33 ps, tolerating 46 ps of delay uncertainty. Note that this delay uncertainty is larger than the initial variation of 23.7 ps, achieving about 100% delay compensation in the critical path.

Similarly, for a short path, the decrease in the delay of the data path due to a 10% increase in the power supply voltage is 8.1 ps. The setup time can therefore be increased from 79 ps to 87.1 ps. The corresponding hold time is therefore reduced from 26.3 ps to 22.3 ps, as determined by (16), tolerating 4 ps of delay uncertainty. Since the variation in the delay of the data path is 8.1 ps, interdependence can compensate approximately 50% of the delay uncertainty of a short path. The results of this procedure for other technology nodes are listed in Tables 4 and 5 for, respectively, a worst case (long) data path and a short path.

Table 4
Compensation of delay uncertainty caused by power noise for a critical data path.

Technology (mm)	Critical data path				
	(T_{S1},T_{H1}) (ps)	Frequency (GHz)	ΔT_D (ps)	(T_{S2},T_{H2}) (ps)	Compensation (%)
180	(110.5, 30.2)	1.5	57.3	(41, 57)	100
		0.6	152.5	(41, 57)	45.6
90	(79, 26.3)	3.2	23.7	(33, 49)	100
		1.6	50.7	(33, 49)	90.7
65	(67.9, 14.9)	4	21.2	(25.8, 26.3)	100
		2	47	(25.8, 26.3)	89.5
45	(56.7, 9.2)	4.2	24.3	(15.4, 14.3)	100
		2.3	51.6	(15.4, 14.3)	80.1

Table 5
Compensation of delay uncertainty caused by power noise for a short path.

Technology (mm)	Short path			
	(T_{S1},T_{H1}) (ps)	ΔT_D (ps)	(T_{S2},T_{H2}) (ps)	Compensation (%)
180	(110.5, 30.2)	17	(127.5, 23.6)	38.8
90	(79, 26.3)	8.1	(87.1, 22.3)	50
65	(67.9, 14.9)	5.9	(73.8, 13.4)	26.2
45	(56.7, 9.2)	2.8	(59.5, 8.9)	10.7

Table 6
Compensation of delay uncertainty caused by threshold voltage variations for a critical data path.

Technology (mm)	Critical data path				
	(T_{S1},T_{H1}) (ps)	Frequency (GHz)	ΔT_D (ps)	(T_{S2},T_{H2}) (ps)	Compensation (%)
180	(110.5, 30.2)	1.5	34.3	(41, 57)	100
		0.6	83.6	(41, 57)	83.1
90	(79, 26.3)	3.2	16.3	(45.3, 42.6)	100
		1.6	38.9	(33, 49)	100
65	(67.9, 14.9)	4	16.1	(25.8, 26.3)	100
		2	35.3	(25.8, 26.3)	100
45	(56.7, 9.2)	4.2	15.3	(15.4, 14.3)	100
		2.3	32	(15.4, 14.3)	100

Table 7
Compensation of delay uncertainty caused by threshold voltage variations for a short path.

Technology (mm)	Short path			
	(T_{S1},T_{H1}) (ps)	ΔT_D (ps)	(T_{S2},T_{H2}) (ps)	Compensation (%)
180	(110.5, 30.2)	13	(123.5, 25.2)	38.7
90	(79, 26.3)	5.9	(84.9, 23.4)	49.5
65	(67.9, 14.9)	4.3	(72.2, 13.8)	25.6
45	(56.7, 9.2)	2.8	(59.5, 8.9)	10.7

As listed in Table 4, delay uncertainty caused by power supply noise in a critical data path can be compensated by up to 100% at higher frequencies. At lower frequencies, more than 80% compensation is achieved in the more deeply scaled technologies. Alternatively, as listed in Table 5, for a short path, the compensation is lower due to the relatively smaller slope of the function $T_H = f(T_S)$ as compared to $T_S = f^{-1}(T_H)$, as illustrated in Fig. 10.

The same procedure is also applied to threshold voltage variations. Delay variations due to uncertainty in the threshold voltage and the amount of compensation for long and short paths are listed, respectively, in Tables 6 and 7. For long paths, higher compensation is possible since the delay exhibits a relatively weaker dependence on threshold voltage as compared to power supply voltage. For short paths, compensation of the delay uncertainty caused by power supply and threshold voltage is comparable since the delay variations are sufficiently close in both cases.

6. Conclusions

The efficacy of interdependence in reducing delay uncertainty (therefore enhancing robustness) is investigated for four CMOS technologies. The proposed approach provides enhanced understanding of the capabilities provided by setup-hold interdependence, thereby overcoming the limitations of only considering static timing analysis results. The dependence of interdependence on technology scaling is also investigated. A case study is presented where the efficacy of setup-hold interdependence in reducing delay uncertainty due to power supply noise and threshold voltage variations is demonstrated. According to these results, interdependence is shown to be highly effective in enhancing the robustness of the critical paths in deep submicrometer technologies.

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