Perspective Paper—Can AC Computing Be an Alternative for Wirelessly Powered IoT Devices?

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***Abstract*—An alternative computing paradigm is explored in this letter with application to wirelessly powered Internet of Things (IoT) devices. Contrary to existing methods that rely on DC computing, the wirelessly harvested AC power is directly used for computation by leveraging charge-recycling theory. The proposed approach has the potential to significantly reduce the energy cost, one of the primary barriers that slows down the global scalability of IoT devices. This opportunity and related challenges are investigated in this letter to provide guidelines for future research in the field.**

***Index Terms*—AC computing, Internet of Things (IoT), wireless power.**

I. Introduction

INTERNET of Things (IoT) has emerged as an innovative platform to integrate diverse cyber-physical systems. The number of *connected* IoT devices is expected to reach 32 billion by 2020 and trillion-sensor networks are expected to be a reality within ten years [1].

Energy autonomy is one of the most critical challenges to realize this remarkable growth and ensure global scalability of IoT devices [2]. Relying on existing battery technologies is not only impractical (would require 275 million battery changes a day), but also insufficient due to stringent constraints on form factor and limited power densities of conventional electrochemical charge storage techniques [3].

Energy harvesting has long been studied to power traditional wireless sensor nodes. Light, motion, and radio frequency (RF) signals are promising energy sources for emerging IoT devices [4], [5]. Wireless/RF power harvesting has received considerable attention due to the ubiquity of RF energy around the world such as mobile phones, TV/radio broadcast, and mobile base stations [6], [7]. Dedicated wireless power sources have also been utilized as in RFIDs. A primary issue in wireless power harvesting methods is the strong dependence of the harvested power on the distance between the source and load due to signal attenuation throughout the space.

This letter embodies a novel vision on developing an efficient computing paradigm for wirelessly powered (WP) IoT devices. The proposed method investigates the direct use of AC power for computing while increasing the energy efficiency by more than an order of magnitude.

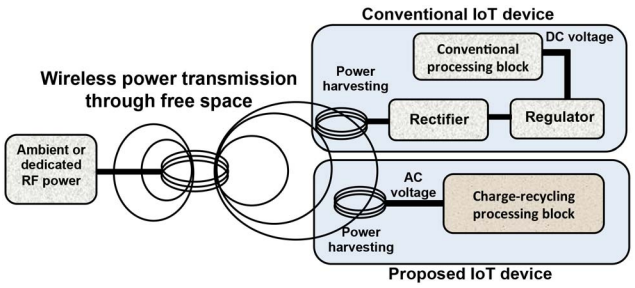

Fig. 1. Conceptual diagram illustrating the primary difference between the existing method and proposed approach.

II. Background and Previous Work

In traditional approaches, the harvested signal by the IoT device is *rectified* to obtain a relatively stable DC power supply voltage, as illustrated in Fig. 1. Rectification is required in existing practice since the conventional logical gates require a DC voltage for computation. Due to limited harvested power, the amplitude of the rectified voltage is typically low, thereby restricting the computational capability of the IoT device. Furthermore, the conversion efficiency of modern rectifiers is in the range of 50%–60%, meaning that approximately half of the harvested power is lost in this stage [8]. Traditional approaches also require a regulation stage to ensure that the power supply voltage does not vary when the processing block changes its activity [9].

Contrary to the existing practice, this letter focuses on leveraging the theory of charge-recycling operation that enables the direct use of the harvested signal *without* rectification and regulation, as also depicted in Fig. 1. More specifically, the proposed computing method using wireless energy relies on recycling electrical charge during operation to save energy. In conventional computing methods where power supply is a DC voltage, the charge used to represent a Boolean logic *high* is dissipated to ground when the state changes to logic *low*. Alternatively, in charge-recycling operation, a sinusoidal (AC) power supply is used and the charge is slowly transferred (i.e., recovered) back to the power supply.

Charge-recycling operation was invented in the early 1990s, following the ideas of famous physicists Feynman, Bennett, and Landauer on the thermodynamics of energy transfer [10], [11]. Specifically, if energy is transferred through a dissipative medium sufficiently slowly, power consumption can be extremely small. Charge-recycling operation aims at

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realizing this principle in circuit design to minimize power consumption.

Due to this highly desirable characteristic, significant research has been conducted on charge-recycling operation since 1990s [12]–[14]. Despite these research efforts, the practical application of charge-recycling has remained limited due to well understood limitations, particularly on the inefficient generation of the AC signal (with up to 10%–30% efficiency) used as the power source.

III. AC Computing for Wirelessly Powered IoT Devices

A. Proposed Approach

Interfacing wireless power harvesting with charge-recycling operation has the potential to overcome some of the fundamental limitations of the traditional charge-recycling circuits such as the generation of the AC signal from a DC source. In the proposed approach, the harvested signal is naturally in the form of an AC signal, which is directly used for computation without rectification and regulation. This approach brings the following advantages for IoT devices:

1) higher energy efficiency that will: a) expand the existing application domain by enabling powerful local processing capability; and b) enhance the digital implementation of the network protocols and algorithms;
2) elimination of the power losses due to rectification and regulation stages of conventional methods;
3) elimination of the strong dependence on battery, which is important for applications in environmental/structural monitoring where battery changes are not practical.

Existing charge-recycling mechanisms cannot be directly used to WP IoT devices due to the absence of a DC voltage and sinusoidal signals with negative voltages. Three methods are proposed in this letter, each leveraging a different charge-recycling mechanisms:

1) efficient charge-recovery logic (ECRL) [15];
2) pass transistor adiabatic logic (PAL) [16];
3) complementary energy path adiabatic logic (CEPAL) [17].

Each of these charge-recycling mechanisms works with an AC signal, but exhibits differences in operation.

For WP-ECRL [18], as depicted in Fig. 2, a peak detector and phase shifter are proposed. The peak detector (see Fig. 5) consists of a diode-connected pMOS transistor where the output signal is connected to the bulk terminals of all of the pMOS transistors to properly bias the substrate. Note that the current that flows through the peak detector is negligible and therefore the power loss is minimized. Two conventional *LC* phase shifters are used to obtain four AC signals with 90° phase difference, as required by ECRL.

For WP-CEPAL and PAL, as depicted, respectively, in Figs. 3 and 4, a signal shaper is proposed. As an advantage, CEPAL and PAL do not require 90° phase difference. As a limitation and unlike ECRL, these mechanisms cannot reliably operate with the wirelessly harvested AC signal that has both positive and negative voltage components. The proposed signal shaper (see Fig. 6) is similar to the peak detector, but when the transistor does not conduct, the output can still follow the shape of the input AC signal without falling below zero volt. Thus, the signal shaper enables charge recovery during the falling transition of the shaped signal through the relatively large gate-to-source and gate-to-bulk capacitances, even though the transistor is off. Also note that the power loss is minimized by ensuring small voltage difference across

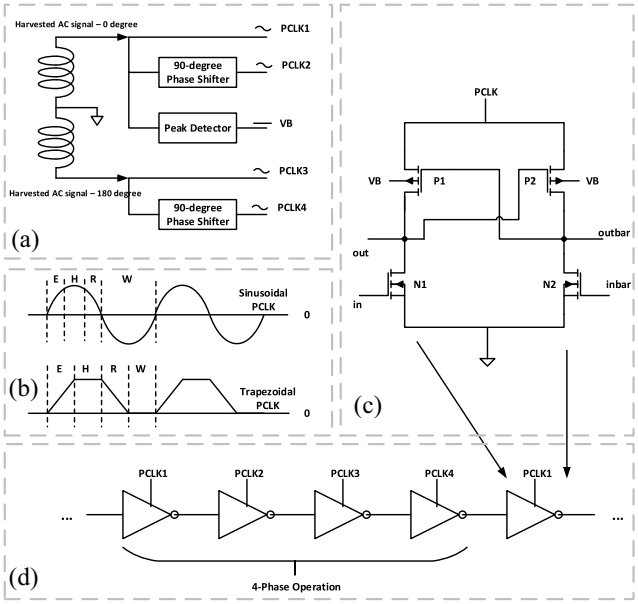


Fig. 2. WP-ECRL: (a) Requirement for two phase shifters and a peak detector. (b) AC power-clock (pclk) signal. (c) Example gate. (d) Cascaded gates.

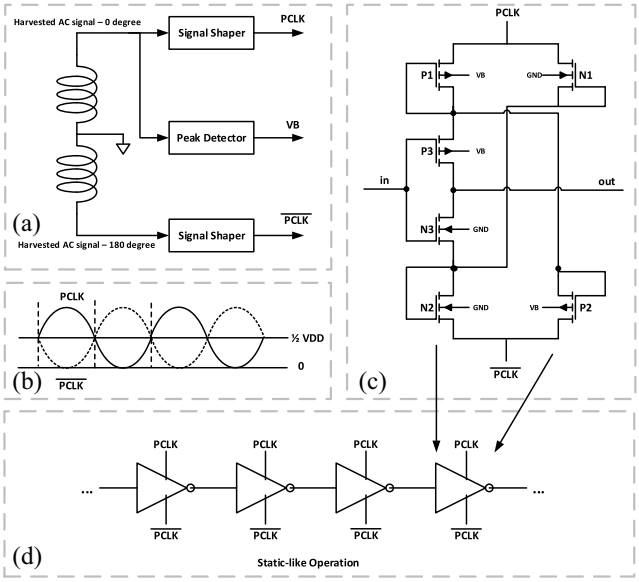


Fig. 3. WP-CEPAL: (a) Requirement for two signal shapers and a peak detector. (b) Two out-of-phase AC power-clock (pclk) signals. (c) Example gate. (d) Cascaded gates.

the shaper when the transistor is on. CEPAL and PAL do not require a phase shifter since the coil orientation within the secondary coil is exploited to wirelessly harvest two out-of-phase AC signals.

B. Simulation Results

To demonstrate the feasibility of the proposed approach and quantify the benefits in efficiency, a wireless link based on near-field inductive coupling has been designed. The link consists of two coils: a primary coil driven by an RF power amplifier to transmit a dedicated radio signal. The target IoT device harvests the electromagnetic energy by secondary coils. The amount of energy successfully harvested by the secondary coil depends upon the coupling coefficient (which is a strong

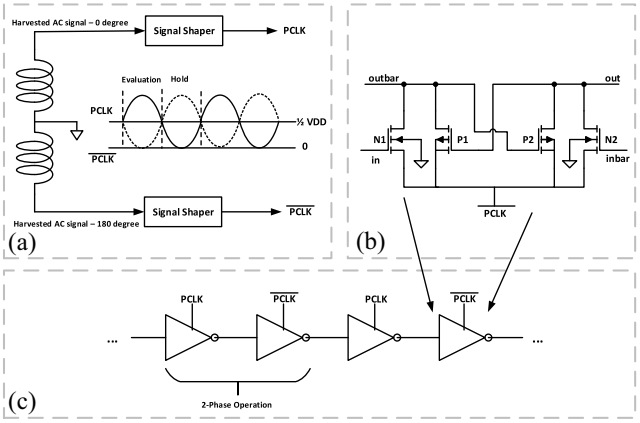


Fig. 4. WP-PAL: (a) Requirement for two signal shapers. (b) Example gate. (c) Cascaded gates.

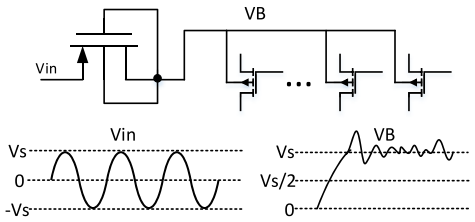


Fig. 5. Peak detector for WP-ECRL and CEPAL.

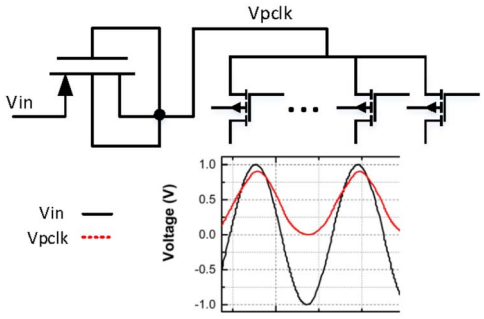


Fig. 6. Signal shaper for WP-CEPAL and PAL.

function of distance between the coils). The weakly coupled wireless link can be accurately modeled with an *RLC* circuit and an ideal transformer, while considering the resistive losses due to the coils.

The wireless link has been combined with a 16-bit carry select adder that has been designed using both conventional and proposed methods. A 45-nm CMOS technology has been used for each method. The wirelessly harvested signal varies from -1 to $+1$ V. In the conventional approach, the harvested AC signal has been converted into a regulated DC signal of 1 V through a rectifier and regulator, as shown in Fig. 7. The regulated DC signal has been used to power conventional static CMOS based 16-bit carry select adder with flip-flops at the primary inputs and outputs. Alternatively, in the proposed approach, the harvested AC signal has been directly used for computation using three different charge-recycling mechanisms, as described in the previous section. ECRL and PAL are inherently pipelined so no flip-flops are required. Additional buffers, however, are inserted to ensure that the number of gates from inputs to each output is the same, thereby correctly synchronizing the data flow. Similar to static CMOS, CEPAL requires flip-flops for synchronization.

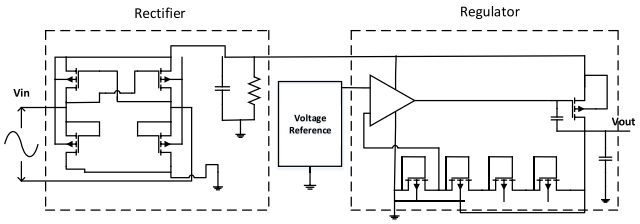


Fig. 7. Rectifier and regulator required for the conventional approach.

A representative waveform for one of the bits is depicted in Fig. 8(a) for each computing method. The average power consumed by each method has been analyzed at the same frequency (low RFID frequency band of 13.56 MHz) for 100 clock cycles with the same input data pattern. The results are shown in Fig. 8(b). According to this figure, the overall average power consumed by the conventional method is approximately 26.4 μW. Alternatively, the power consumed by the proposed method can be as low as 1.97 μW (for the WP-PAL), demonstrating 13.4$\times$ reduction. Note that the power consists of two components: 1) processing and 2) overhead power. The processing power represents the logical power consumed by the 16-bit adder whereas the overhead power represents the power consumed by the supporting blocks. In conventional method, these supporting blocks include the rectifier and regulator, consuming 17.6 μW, approximately 67% of the overall power. In WP-ECRL, the overhead power is due to two phase shifters (resistive loss) and a peak detector, consuming 3.7 μW. In WP-CEPAL, the overhead power due to two signal shapers and a peak detector is 1.5 μW. Finally, in WP-PAL, the overhead power due to two signal shapers is 1.7 μW. These results demonstrate that in the proposed approach, both the processing and overhead power are reduced, increasing the energy efficiency of a WP device by up to an order of magnitude. Several future research directions and limitations of the proposed method are discussed in the following section.

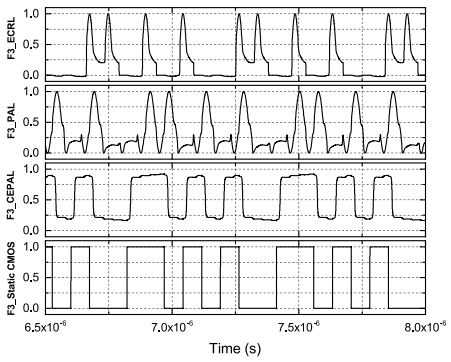
IV. Future Research Directions

An important future direction is to increase the frequency of the wireless signal to the UHF band, up to gigahertz range. This step is important to increase the wireless power transfer range and be able to consider high frequency wireless energy sources. Unlike static CMOS where energy to charge/discharge a capacitance does not depend upon transition time, in charge-recycling operation, energy is inversely proportional with the transition period of the wireless signal. Thus, charge-recycling circuits save more power at lower frequencies. Specifically, for charge-recycling operation to outperform static CMOS, the transition time T should satisfy

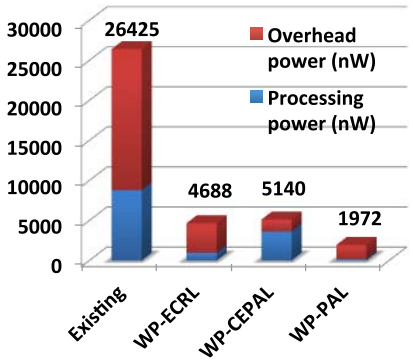
$$T > 4\frac{RC}{\alpha} \tag{1}$$

where α is the activity factor, R is the on-resistance of a transistor, and C is the load capacitance. Note that the RC parameter scales approximately quadratically with technology. Thus, in nanoscale technologies (where the RC is in the low picoseconds range), charge-recycling operation can provide considerable power savings, even at the gigahertz frequencies. Elimination of rectifier and regulator further increases the power savings.

Another future direction is analyzing the behavior of the WP charge-recycling logic under variations. One consideration is a possible deviation in the phase difference among multiple AC power supplies and variations in the peak-to-peak



(a)



(b)

Fig. 8. (a) Representative waveform for one of the bits for each computing method. (b) Comparison of the average power consumed by the 16-bit carry select adder operating at 13.56 MHz and designed in both existing and the proposed methods.

voltage of the harvested AC supply. Design guidelines should be developed to obtain a robust computational unit despite these nonidealities.

Future work can also focus on design techniques to operate with AC power supplies having reduced peak-to-peak voltages. Capability to operate at low voltages is essential for harvesting *ambient wireless energy* since voltage significantly attenuates throughout the space. AC computing with near-threshold charge-recycling operation presents new and largely unexplored opportunities.

In conventional energy harvesting systems with DC computing, the harvested energy can be stored within a storage device when not needed. These conventional storage components, however, cannot be used for the proposed scheme that is based on AC computing. Thus, another future direction is to mitigate this limitation by investigating high-Q LC tank based energy storage mechanisms and developing methods to copy data to nonvolatile memory when harvested energy is reduced to critical levels [19]. Another approach is to investigate the feasibility of electromechanical energy storage methods that do not require DC conversion.

Finally, most of the IoT devices require not only digital, but also analog blocks for sensing and communication. An interesting future direction is to investigate charge-recycling analog building blocks such as amplifiers. An intermediary solution would be to the split the overall energy and obtain a DC voltage, only for the analog blocks and leverage more efficient AC computing unit for local processing. The efficient on-site processing can extract meaningful information and potentially reduce the amount of data (and therefore power) that should be transmitted.

V. Conclusion

AC computing is introduced as a promising alternative for WP IoT devices. The fundamental characteristics of the proposed approach, related challenges and possible solutions have been outlined. Significant increase in energy efficiency has been demonstrated. The proposed approach can play an important role in the development of smarter IoT devices with powerful local processing capability, thereby bringing new opportunities in emerging applications such as computational RFIDs and structural/environmental monitoring.

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