A New Circuit Design Framework for IoT Devices: Charge-Recycling with Wireless Power Harvesting

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***Abstract*—Limited energy is a significant challenge for IoT devices since frequent battery replacement is not feasible. Various energy harvesting techniques have been previously proposed to alleviate this challenge. A new circuit design technique is developed in this paper to significantly enhance the power efficiency of existing wireless energy harvesting methods. Contrary to the traditional approach, the rectification and regulation blocks are eliminated and the harvested signal is directly used to power the IoT device by leveraging charge-recycling circuit theory. In addition to higher energy-efficiency, the proposed approach also reduces the form factor and therefore lowers the cost of an IoT device. The methodology is evaluated using a 45 nm CMOS technology, demonstrating approximately five times reduction in power consumption compared to the traditional approach.**

I. Introduction

Internet of things (IoT) is emerging as a novel computing paradigm connecting global cyber network with the everyday physical realm. This paradigm is applicable to many areas such as transportation, healthcare, smart environment, and social relationships [1]. The enabling factor of IoT is the development and integration of advanced identification, sensing, logic computation, and wireless communication devices.

Existing IoT devices suffer from limited battery life since it is not practical to regularly replace the battery of billions of devices. Even the passive RFID tags suffer from higher energy dissipation and larger area caused by the full wave rectifier and voltage regulator circuitries [2]. Thus, form factor and energy-efficiency are primary issues for future IoT devices.

Motivated by these fundamental issues, a novel wirelessly powered circuit is proposed in this paper, as depicted in Fig. 1. In this framework, existing charge-recycling theory is leveraged to directly power the computational block within the device with an AC signal harvested from a wireless energy source. Thus, the rectification and regulation steps of traditional approach are eliminated, enhancing energy-efficiency and lowering the form factor.

The rest of the paper is organized as follows. Existing approach for IoT devices with wireless energy harvesting is summarized in Section II. The proposed approach is described in Section III. Simulations results demonstrating the functionality and energy-efficiency of the proposed approach are presented in Section IV. Finally, the paper is concluded in Section V.

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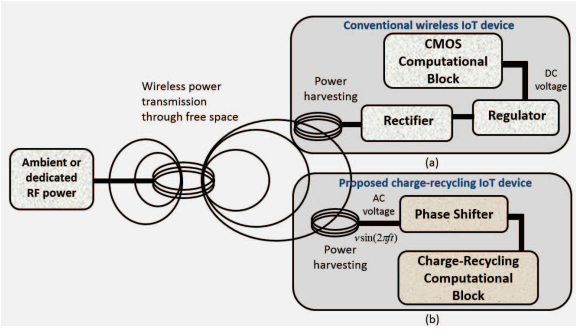

Fig. 1. Conceptual diagram of IoT devices with wireless power harvesting: (a) conventional topology, (b) proposed topology.

II. Background

Various energy harvesting methods (such as photovoltaic, electrostatic or piezoelectric, thermoelectric, and RF or inductive transducers) have been proposed to alleviate the strong dependence of IoT devices on battery [3]. The first three transducers are heavily dependent upon the presence of a corresponding energy source. Alternatively, RF wireless power harvesting can typically provide a more steady energy source, considering the abundance of various radio signals. A traditional RF energy harvester receives the propagated electromagnetic wave with an antenna (or coupling coil) and converts the alternating power into a stable DC voltage for driving the IoT devices [4]. This step typically consists of a full wave rectifier, a voltage multiplier, and a regulator. When the harvested RF signal is converted to a DC supply voltage, significant energy is lost due to low power efficiencies of the rectification process. Additional power is lost during the regulation step [5]. Even with the state-of-the-art RF-DC converters, at least 30% of the power is lost during this stage [4].

III. Proposed Methodology

In the proposed approach, the harvested AC signal (in the form of a sine wave) is directly used for computation by leveraging existing charge-recycling circuit theory. In charge-recycling circuits, power dissipation is significantly reduced by 1) steering the currents across the transistors with small voltage differences, and 2) by gradually recovering part of the energy stored in the parasitic capacitances [6]. This approach has been proposed in mid 1990s as an alternative computing method to static CMOS operation [7]. Its applicability,

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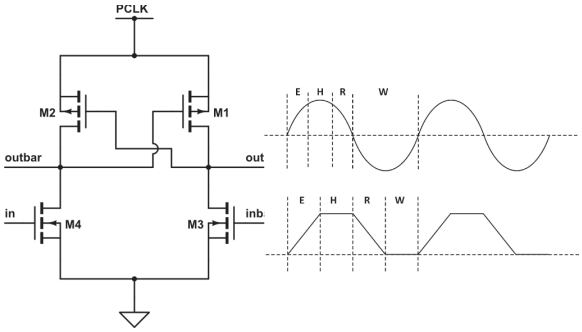

Fig. 2. Inverter designed with the efficient charge recovery logic (ECRL) and the related power-clock (PCLK) signal with four phases.

however, has remained highly limited due to the inefficient generation of the required AC (or trapezoidal) signal from a DC supply voltage, sacrificing most of the power savings [8].

Alternatively, in the proposed application, power is harvested in the form an AC signal, eliminating this well-known limitation. Thus, wirelessly powered IoT devices represent a unique application domain for charge-recycling circuits, as demonstrated in this paper.

The efficient charge recovery logic (ECRL), powered by a four-phase AC signal (known as the power-clock signal) is chosen as the logic family, as shown in Fig. 2 [7]. Power-clock signal is typically a trapezoidal waveform and has four phases: evaluation (E), hold (H), recovery (R), and wait (W). As shown in Fig. 2, an ECRL inverter has two cross-coupled PMOS transistors for precharge/evaluation and recovery phases, and two NMOS transistors for the functionality. Once the PCLK signal reaches the threshold voltage of M1, *outbar* starts to follow PCLK signal, assuming signal *in* is at logic high (so that *outbar* is at logic low). During the hold phase, the output voltage is stable so that the next stage can properly evaluate. During the recovery phase, PCLK gradually falls, recycling the charge stored on the load capacitance. For symmetry, a wait phase is inserted to complete the four-phase PCLK operation. There is 90° phase difference between the PCLK signal of adjacent gates, requiring four PCLK signals. Thus, ECRL logic is inherently pipelined.

In the proposed scheme, since the AC signal is wirelessly harvested, a sinusoidal PCLK signal is obtained rather than the traditional trapezoidal waveform. The three components of the proposed approach (wireless link, phase shifter, and charge-recycling computational block) are described in the following subsections.

A. Wireless Link

Based on the wireless energy harvesting technique used in RFID tags and certain biomedical implantable devices, the target IoT device is designed to obtain the power supply voltage through inductive coupling [9]. As illustrated in Fig. 1, a primary coil is driven by an RF power amplifier to transmit a dedicated radio wave. The target wireless device harvests the electromagnetic energy by secondary coils (that are inductively coupled).

The percentage of energy extracted by the secondary coil

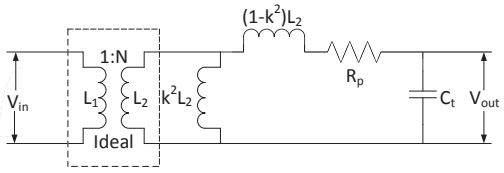

Fig. 3. Equivalent model of a weakly coupled inductive energy harvesting system.

TABLE I
WIRELESS LINK SPECIFICATIONS

Parameter	L_1	L_2	R_p	C_t	N
Value	228.4nH	3.656μH	1Ω	330pF	3

can be evaluated from the coupling factor *k*, which, in the air, can be empirically expressed by [10],

$$k = \frac{r_1^2 r_2^2}{\sqrt{r_1 r_2}(\sqrt{x^2 + r_2^2})^3}, \tag{1}$$

where r_1 and r_2 are the radii of, respectively, the primary and secondary coils. x represents the distance between the two coils. This weakly coupled topology can be accurately modeled with an RLC circuit and an ideal transformer, as depicted in Fig. 3. In this electrical model, L_1 and L_2 of the ideal transformer represent the two separate coils. R_p represents the parasitic resistive loss in the front-end harvesting circuitry and C_t is the tuning capacitance for boosting the coil voltage level. The ratio N inside the transformer is given as [10],

$$N = k\sqrt{\frac{L_2}{L_1}}. \tag{2}$$

The parameters of the wireless link for the proposed approach are listed in Table I. The two inductors are implemented on the board. Note that the two inductors within the secondary coupling circuit are configured such that the two harvested RF signals have 180° phase difference, thereby providing the first and third PCLK signals required for the ECRL logic. The remaining two phases are obtained by the proposed phase shift circuitry, described in the following section.

B. Phase Shift Circuitry

Phase shifters generate a fixed phase angle along a transmission line driven by an electromagnetic wave of a certain frequency. Switched low pass and high pass topologies are commonly used in monolithic microwave ICs for achieving a flat band of 180° phase shift [11]. Inspired from this topology, the low pass arm is extracted from the switched line phase shifter to generate the four-phase PCLK signal. The proposed phase shift circuitry can be modeled as a π-LC low pass network, as shown in Fig. 4. For a θ phase shift, the values of inductor (L) and capacitor (C) in the model are determined from

$$L = \frac{Z_0 \sin\theta}{\omega} \qquad \text{and} \qquad C = \frac{1 - \cos\theta}{\omega Z_0 \sin\theta}, \tag{3}$$

where Z_0 is the parallel impedance to alleviate the effect of varying load impedance. The design parameters of the proposed phase shifter are listed in Table II. The resistor and inductor are implemented on the board. As mentioned in the

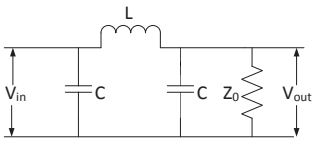

Fig. 4. Phase shift circuitry modeled as a π-LC low pass network.

TABLE II
PHASE SHIFTER SPECIFICATIONS.

Parameter	L	C	Z_0
Value	796μH	$100fF$	$100k\Omega$

previous subsection, 0° and 180° PCLK signals are obtained from the secondary coupling circuit. Thus, when these two signals propagate through the proposed 90° phase shifter, the third and fourth PCLK signals are generated to complete the full operation of ECRL computational block, as described in the following section.

C. Charge-Recycling 4-Bit Carry Ripply Adder

A 4-bit adder is chosen to demonstrate the functionality of the computational block that operates with the wirelessly harvested AC signal. Considering the inherently pipelined characteristic of ECRL logic, output signals should be carefully synchronized. Specifically, the overall number of ECRL gates from input to output should be the same for each output. This behavior requires the insertion of ECRL buffers along certain output paths.

A 4-bit carry ripple adder consisting of four cascaded 1-bit full adders requires 4 cycles (since 1-bit full adder requires 1 cycle) to complete an addition operation, assuming a standard cell based adder design. Instead, the *propagate* and *generate* signals are utilized for the carry ripple adder, as depicted in Fig. 5. Furthermore, the AND gate and OR gate are merged into one complex ECRL gate, referred to as the ECRL group PG cell [7]. Finally, due to inherent pipelining, buffers are inserted to synchronize each output. A logic depth of 1.25 cycles is achieved. This 4-bit ECRL carry ripple adder can be used as a building block to develop high bit ECRL adders.

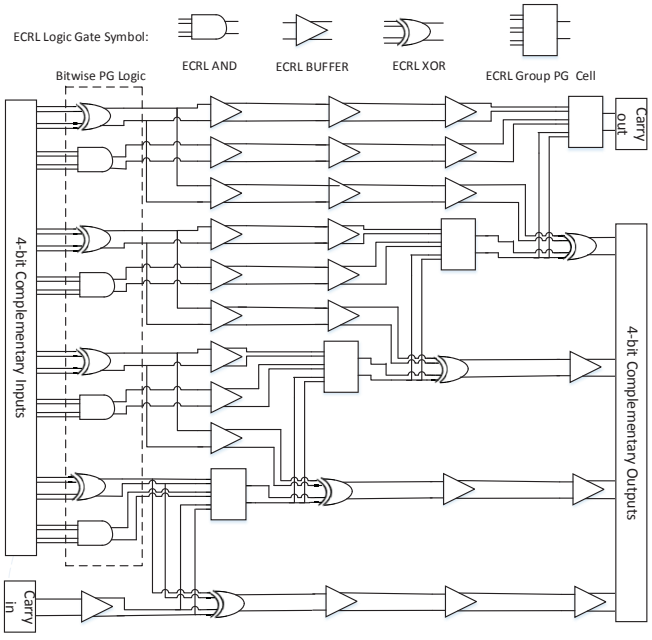

Fig. 5. Block diagram of a 4-bit ECRL carry ripple adder utilizing the *generate* and *propagate* signals.

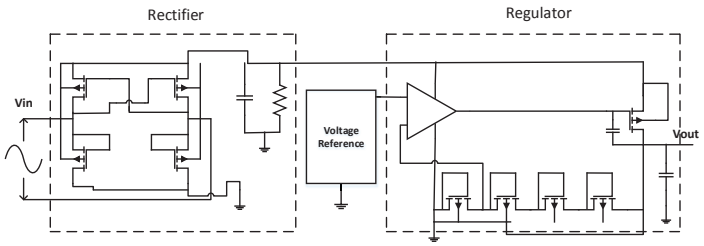

Fig. 6. Circuit diagram of a low complexity RF-DC converter and regulator for traditional IoT devices.

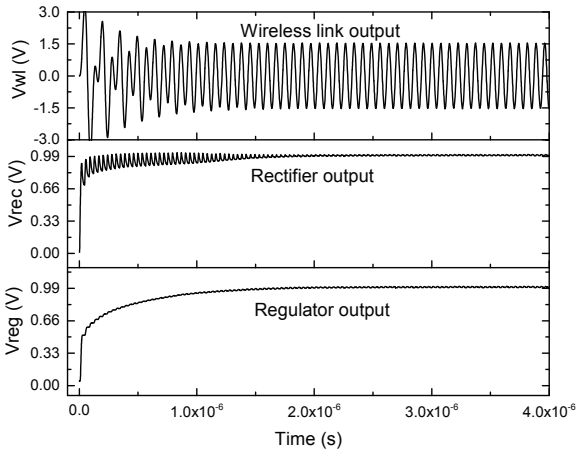

Fig. 7. Simulated output waveforms of the wireless link, rectifier, and regulator. The final regulated output voltage is approximately 1 V, which is used to drive the conventional 4-bit adder running at 13.56 MHz clock frequency.

IV. SIMULATION RESULTS

To investigate and quantify the benefits of the proposed approach, both the traditional method that rectifies and regulates the harvested AC signal and the proposed method are designed using 45 nm technology. Both approaches have the same wireless link, as described in Section III-A where the transmission frequency is 13.56 MHz. Note that this is the standard frequency for silicon based item-level RF identification [12].

For the conventional approach, an efficient and low complexity rectifier and regulator are designed, as shown in Fig. 6. The functionality of the rectification and regulation are illustrated in Fig. 7 where the output signals of the wireless link, rectifier, and regulator are shown. The output voltage is regulated at approximately 1 V. This voltage powers a conventional 4-bit carry ripple adder operating at 13.56 MHz. All of the primary inputs and primary outputs are latched into flip-flops.

Alternatively, for the proposed approach, the phase shifter described in Section III-B is designed to generate four PCLK signals with 90° phase difference, as depicted in Fig. 8. These sinusoidal PCLK signals are used to drive the ECRL adder,

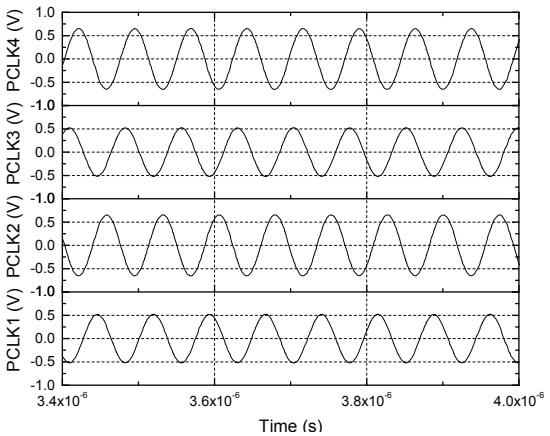

Fig. 8. Four PCLK signals at 13.56 MHz frequency and with 90° phase difference, as generated by the phase shifter. These sinusoidal PCLK signals drive the ECRL adder in the proposed approach.

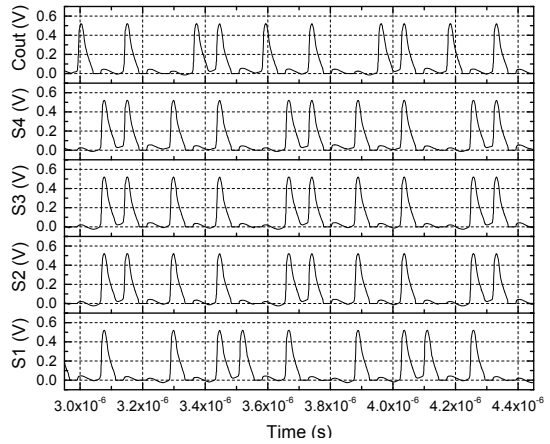

Fig. 9. Output signals of the 4-bit charge-recycling adder driven by four AC signals. The AC signals are obtained from the phase shifter, which takes the wirelessly harvested AC signal as the input.

described in Section III-C. Note that the peak amplitude of the PCLK waveforms shown in Fig. 8 is not identical with approximately 100 mV variation. This variation is due to the slightly different load impedance seen by each PCLK signal. This difference, however, does not affect the proper operation of the ECRL adder since the peak voltage is greater than the threshold voltage. The output signals of the ECRL adder driven by the wirelessly harvested AC signal are shown in Fig. 9 when a cyclic input data pattern is provided as $C_{in} = 11110000$, $A_i = 01010101$, $B_i = 11001100$, where $i = 1, 2, 3, 4$. As demonstrated by the output signals, the ECRL adder accurately and reliably works with the harvested AC signal where the logic high voltage levels are sufficiently distinguishable.

To compare energy consumption, both the traditional design (wireless link, rectifier, regulator, and static CMOS based 4-bit adder running at 13.56 MHz) and proposed approach (wireless link, phase shifter, and ECRL based 4-bit adder running with four harvested AC signal, each at 13.56 MHz) are simulated for 4 μs and the consumed energy is analyzed, as listed in Table III. According to this table, the overall energy consumed by the proposed approach is five times

TABLE III
ENERGY DISSIPATION COMPARISON OF THE PROPOSED AND TRADITIONAL APPROACH.

Conventional Design		Proposed Design	
Block	Energy Loss (fJ)	Block	Energy Loss (fJ)
4-bit Adder	5958	4-bit Adder	500
Rectifier and Regulator	70502	Phase Shifter	11490
Total	**76460**	**Total**	**16490**

less than the energy consumed by the traditional approach, even though both systems operate at the same 13.56 MHz frequency. Furthermore, the reduction in energy consumption is expected to further increase with a larger computational block since charge-recycling adder consumes approximately eleven times less energy than the static CMOS adder. Thus, the overhead incurred due to the phase shifter is further reduced as the logic grows.

V. CONCLUSION

A new circuit design framework has been proposed for IoT devices. The proposed method revitalizes the existing charge-recycling theory through application to wireless power harvesting. Despite the well-known limitations of the charge-recycling circuits in conventional systems, in the proposed application, charge-recycling can achieve significant power savings since the wirelessly harvested signal is already in the form of an AC signal. Electrical models and circuits have been developed for the wireless link, phase shifter, rectifier, and regulator. A comprehensive analysis method has been generated to achieve a fair comparison. Simulations in 45 nm technology demonstrate that the proposed approach can reduce the overall energy by approximately five times.

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