On-Chip Hybrid Regulator Topology for Portable SoCs with Near-Threshold Operation

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***Abstract*—A novel hybrid regulator topology is proposed to alleviate the weaknesses of existing hybrid topologies. Contrary to the dominant existing practice, a switched-capacitor converter and a resistorless LDO operate in a parallel fashion to supply current and regulate the output voltage. The proposed design targets a fully integrated regulator without using any inductors and resistors. The primary emphasis is on maximizing power efficiency while maintaining sufficient regulation capability (with ripple voltage less than 5% of the output voltage) and power density. Simulation results in 45 nm technology demonstrate a power efficiency of approximately 85% at 100 mA load current with an input and output voltage of, respectively, 1.15 V and 0.5 V. The worst case transient response time is under 20 ns when the load current varies from 65 mA to 130 mA. The worst case ripple is 22 mV while achieving a power density of 0.5 W/mm^2. These results outperform existing studies and demonstrate the applicability of the proposed regulator to portable SoCs.**

I. Introduction

The significance of on-chip voltage conversion and regulation has increased in the past decade due to various reasons such as power management within multi-core ICs, multi-voltage designs, dynamic voltage frequency scaling, power integrity, and near-threshold operation [1]–[4]. For example, Intel has developed a fully integrated voltage regulator (FIVR) for the Haswell microarchitecture, allowing dynamically managed multiple power domains [5].

Near-threshold computing has also received significant attention due to enhanced energy efficiency, particularly for mobile SoCs [6]. Highly parallelized architectures based on near-threshold operation have been proposed as a possible solution to dark silicon [7]. Developing an integrated voltage regulator module with application to near-threshold operation is challenging due to low output voltages in the range of 0.5 V. The regulator should simultaneously satisfy high power efficiency and power density (to minimize area overhead). Furthermore, the output ripple should be minimized since near-threshold circuits are highly sensitive to power supply variations (due to near-exponential dependence).

Linear low-dropout (LDO) regulators have been commonly used due to low cost and area efficiency. Unfortunately, LDO regulators suffer from low power efficiency (less than 60% in the majority of the cases) [8]. This issue is exacerbated for higher conversion ratios as needed in near-threshold computing since the output voltage is in the range of 0.5 V. Alternatively, switched-capacitor DC-DC converters enhance power efficiency, but typically have poor regulation capability, causing higher ripple voltage and long transient response time [1]. This limitation is critical for near-threshold operation due to high sensitivity to supply voltage. Finally, switching buck converters can achieve sufficiently high power efficiency and sufficient regulation capability, but require high-quality inductors (typically more than one due to multi-phase operation), significantly increasing the overall cost.

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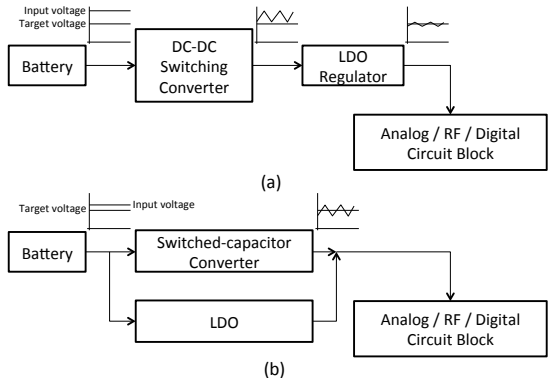

Fig. 1. **Conceptual block diagram of (a) a conventional hybrid regulator, (b) proposed hybrid regulator.**

Hybrid regulators have also been developed to exploit the advantages of both LDOs and switching converters [9], [10], as conceptually depicted in Fig. 1(a). Existing hybrid topologies, however, suffer in near-threshold operation, as further discussed in the following section. A novel hybrid topology, as shown in Fig. 1(b), is proposed in this paper applicable to producing low output voltages at high power efficiency. The proposed approach achieves approximately 85% power efficiency while supplying 100 mA output current at 0.5 V with a maximum ripple voltage of 22 mV.

The rest of the paper is organized as follows. The limitations of existing hybrid topology are discussed in Section II. The proposed hybrid voltage regulator is described in Section III. Simulation results are presented in Section IV. Finally, paper is concluded in Section V.

II. Limitations of the Existing Hybrid Topology

In existing approaches, a DC-DC switching converter is combined in series with an LDO, as shown in Fig. 1(a) [9], [10]. The switched-capacitor circuit functions as a converter

without any regulation capability whereas the LDO regulates the output voltage without any conversion. Thus, the circuit enhances power efficiency since LDO has a near-unity voltage conversion ratio. Regulation is also enhanced due to an LDO with fast transient response at the output. Feed-forward ripple cancellation has also been proposed to further improve the regulation process [9]. This topology, however, suffers in near-threshold operation with large output current and low output voltage due to three reasons:

- Power transistor of the LDO suffers from low $|V_{GS}|$ since the voltage conversion is achieved by the previous stage (switched-capacitor converter). This low input voltage makes it challenging to supply high current at the output.
- At high output current, the voltage drop across the power transistor (within an LDO) becomes nonnegligible, requiring a higher input voltage at the LDO. Higher input voltage, however, degrades the power efficiency.
- The maximum output load current cannot be larger than the current supplied by the switched-capacitor converter due to the series connection. Thus, the DC-DC switching converter needs to be optimized for the maximum load current rather than the nominal load current.

These limitations are exacerbated and the power efficiency is further degraded with reduced output voltages, as in near-threshold computing. Thus, a new hybrid topology is proposed in this paper where the switched-capacitor converter and LDO operate in a parallel fashion, as conceptually illustrated in Fig. 1. Specific design techniques are developed to ensure proper operation and outperform existing regulators, as described in the following section.

III. Proposed Regulator

A simplified circuit schematic of the proposed hybrid regulator is shown in Fig. 2. The switched-capacitor circuit and LDO operate in a parallel fashion where the source node of the power transistor within the LDO is connected to the primary DC input voltage V_{in}. Thus, this topology does not suffer from the aforementioned limitations since LDO has a relatively larger input voltage. The switched-capacitor circuit provides the nominal output current while converting the input voltage from 1.15 V to 0.5 V. At the nominal load current, LDO is turned off. Any variation at the output voltage is directly sensed by the error amplifier of the LDO and output voltage is regulated with a fast transient response time.

Some of the important characteristics of the proposed topology are: 1) no resistors are used within the LDO to minimize power loss, 2) a static current minimization technique is developed to maximize power efficiency, 3) since the output voltage is directly sensed by the error amplifier, a small gain-bandwidth product is adopted, thereby preventing the output ripple from being amplified. These characteristics are described in the following subsections.

A. Switched-Capacitor DC-DC Converter

A switched-capacitor converter consists of several switches and capacitors to achieve voltage conversion. The topology shown in Fig. 2 achieves a conversion ratio of two, as required in this study. According to [11], the overall power loss can be expressed by

$$P_{loss} = P_{C_{fly}} + P_{R_{sw}} + P_{bott-cap} + P_{gate-cap}, \quad (1)$$

where $P_{C_{fly}}$, $P_{R_{sw}}$, $P_{bott-cap}$, and $P_{gate-cap}$ refer, respectively, to power loss due to flying capacitor, switch resistance, parasitic capacitance of flying capacitor, and that of the switches. $P_{C_{fly}}$ and $P_{R_{sw}}$ are

$$P_{R_{sw}} \propto I_L^2 \frac{R_{on}}{W_{sw}}, \quad P_{C_{fly}} \propto I_L^2 \frac{1}{C_{fly} f_{sw}}, \quad (2)$$

where I_L is the load current, R_{on} is the on-resistance of a single switch, W_{sw} is the width of a single switch, C_{fly} is the flying capacitance, and f_{sw} is the switching frequency. The shunt power loss due to fully-integrated flying capacitor $P_{bott-cap}$ and gate capacitance of the switches $P_{gate-cap}$ are

$$P_{bott-cap} \propto V_o^2 C_{bott} f_{sw}, \; P_{gate-cap} \propto V_{sw}^2 C_{gate} f_{sw}, \quad (3)$$

where C_{bott} is the sum of the parasitic capacitance from the top and bottom plates of the flying capacitor, V_{sw} is the clock voltage swing, and C_{gate} is the gate capacitance of the switches. Following these expressions, the switch size and flying capacitor are determined to maximize power efficiency [11], [12]. These parameters are listed in Table I.

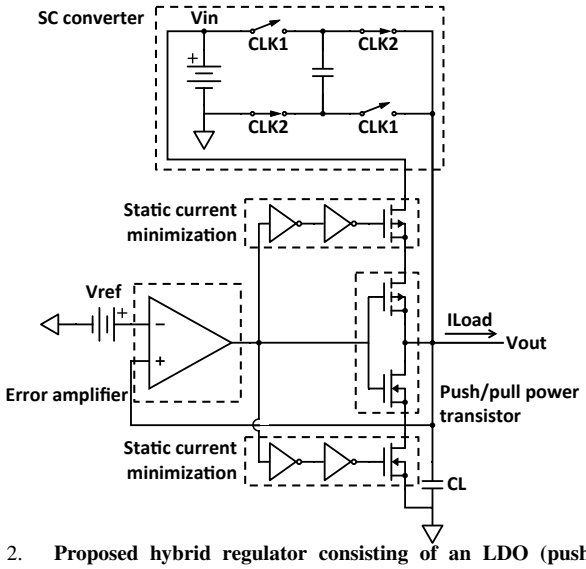

Fig. 2. **Proposed hybrid regulator consisting of an LDO (push/pull power transistors, error amplifier, and static current minimization) and switched-capacitor converter.**

TABLE I
PRIMARY PARAMETERS OF THE SWITCHED-CAPACITOR CONVERTER.

W_{sw}/L_{sw}	43×25 μm/50 nm
C_{fly}	1.5 nF
C_L	1.5 nF
Switching frequency	482 MHz

B. Proposed Resistorless LDO

Contrary to conventional LDOs, the proposed LDO does not contain any resistors to maximize power efficiency, as illustrated in Fig. 2. Instead, a PMOS push power transistor provides the additional current to the load whereas an NMOS

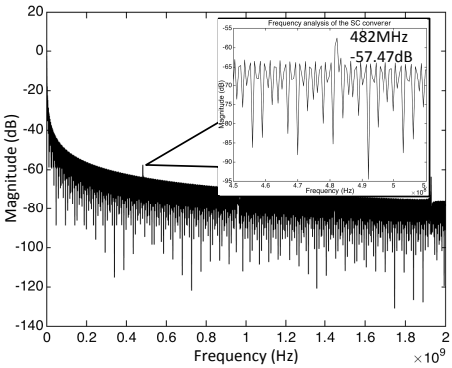

Fig. 3. **Frequency spectrum of the output voltage with 100 mA current.**

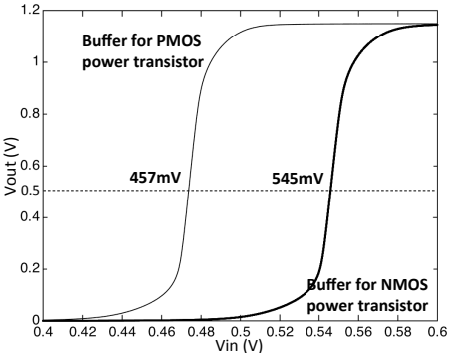

Fig. 4. **DC analysis of the buffers added to prevent static current.**

pull transistor reduces the output voltage. These power transistors are controlled by the output of the error amplifier. The error amplifier directly senses the output voltage and adjusts its output based on the difference between the reference voltage and output voltage. Two important design characteristics are the error amplifier and the static current minimization technique, as described in the following subsections.

1) Optimization of the Error Amplifier: In conventional LDOs, the output frequency spectrum is determined solely by the error amplifier within the LDO. Alternatively, in the proposed regulator, the high frequency components of the output frequency spectrum, as depicted in Fig. 3, are dominantly determined by the switched-capacitor converter since it operates in parallel with the LDO. As listed in Table I, the switching frequency is 482 MHz. According to Fig. 3, the output voltage has a strong frequency component at this switching frequency, demonstrating the effect of switched-capacitor on the frequency spectrum. Thus, the ripple at the output voltage is primarily determined by the switched-capacitor. This behavior is important since the error amplifier directly senses the output voltage in the proposed approach. To prevent the error amplifier from amplifying output ripple, the gain-bandwidth product should be smaller than the switching frequency of the switched-capacitor circuit. Note, however, that a sufficiently small gain-bandwidth product slows down the circuit, increasing the response time. Considering this tradeoff, the gain-bandwidth product is determined as approximately 350 MHz.

2) Static Current Minimization: As opposed to conventional LDOs with single PMOS power transistor, the proposed LDO consists of both PMOS and NMOS power transistors to be able to increase and decrease the output voltage during regulation. Thus, according to the error amplifier output, both power transistors can be on, dissipating significant static current. This behavior should be prevented to maximize power efficiency. For this reason, a buffer with a different switching voltage is added before each power transistor, as illustrated in Fig. 2. The DC voltage characteristics of these buffers are shown in Fig. 4. As illustrated in this figure, the buffer preceding the PMOS power transistor has a much smaller switching voltage than the buffer preceding the NMOS power transistor. This difference in the switching voltage ensures that 1) either only PMOS power transistor is on, or 2) only NMOS power transistor is on, or 3) both power transistors are off. The difference in the switching voltages is determined to ensure that the situation when both transistors are on is avoided, thereby preventing the static current.

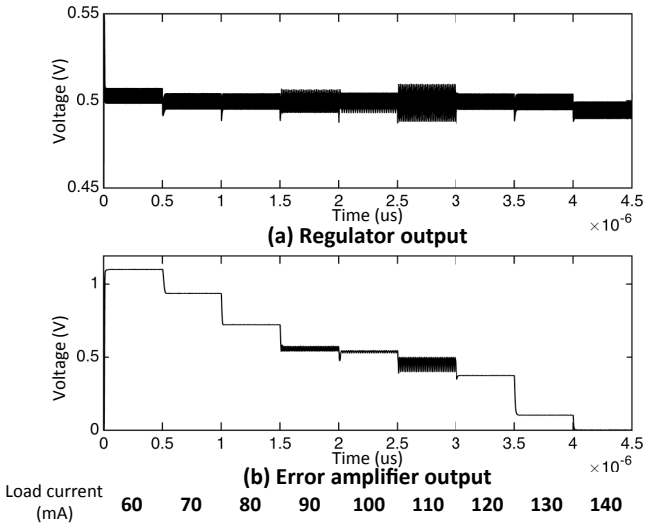

Fig. 5. **Simulation results as the load current abruptly changes from 60 to 140 mA with a step size of 10 mA: (a) output voltage of the regulator, (b) output voltage of the error amplifier.**

IV. Simulation Results

The proposed novel hybrid regulator is designed using a 45 nm CMOS technology with a capacitance density of 30 nF/mm^2. The input voltage is 1.15 V and the output voltage is 0.5 V which is slightly larger than the threshold voltage. The nominal load current is 100 mA, as supplied by the switched-capacitor converter. The total capacitance is 3 nF which approximately occupies 0.1 mm^2, thereby achieving approximately 0.5 W/mm^2. As recently demonstrated by [13], regulators for portable SoCs require this power density to ensure proper operation at reasonable cost.

The output voltage and error amplifier output are plotted in Fig. 5 when the load current varies from 65 mA to 130 mA. As illustrated in this figure, the output of the error amplifier is reduced as the load current increases. Thus, additional current is supplied by the PMOS power transistor. Output voltage remains approximately at 0.5 V with a maximum ripple of 22 mV.

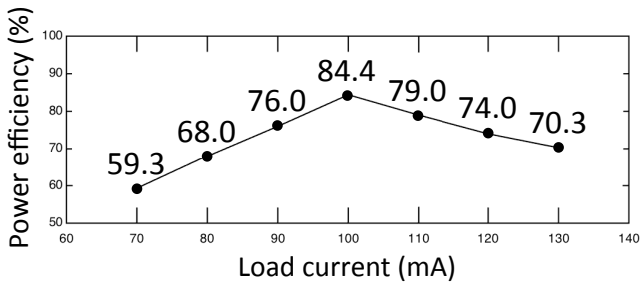

Fig. 6. **Power efficiency of the proposed regulator.**

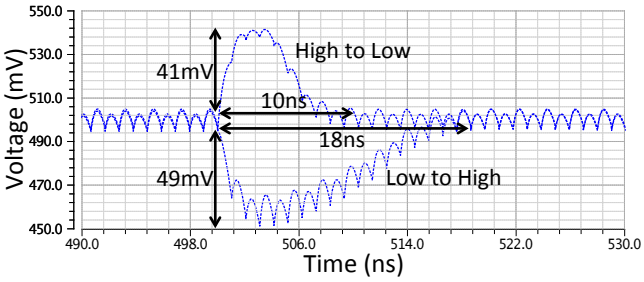

Fig. 7. **Transient response of the proposed regulator when the load current abruptly changes.**

The power efficiency is plotted in Fig. 6 as a function of load current. At the nominal load of 100 mA, the regulator achieves approximately 85% power efficiency. Note that the power efficiency is maintained above 70% across a relatively broad range of load current, from approximately 82 mA to 130 mA.

Finally, the transient response of the proposed regulator is depicted in Fig. 7. When the load current changes from 65 mA to 130 mA, the regulator requires approximately 18 ns to regulate the output voltage back to 0.5 V. Alternatively, when the load current changes from 130 mA to 65 mA, the regulator responds quicker with a response time of 10 ns. The maximum overshoot and undershoot are less than 50 mV in both cases.

The proposed regulator is compared with several recent existing works, developed for similar applications. The comparison results are listed in Table II. According to this table, at comparable current density, this work outperforms other works in both power efficiency and output ripple. Specifically, the output ripple is reduced by more than 60%, enabling a more robust near-threshold operation. A reasonable transient response time is also achieved.

V. CONCLUSIONS

A novel hybrid regulator topology has been proposed for near-threshold computing in portable SoCs. Contrary to existing approaches, a switched-capacitor converter and an LDO operate in a parallel fashion to convert and regulate the output voltage. The proposed LDO does not contain any resistors to minimize power loss. A static current minimization technique has also been introduced to maximize power efficiency. The error amplifier within the LDO is optimized by appropriately choosing the gain-bandwidth product, thereby minimizing the output ripple. Simulation results in 45 nm technology demonstrate that the proposed regulator outperforms existing approaches in primary design objectives.

TABLE II
COMPARISON OF THE PROPOSED REGULATOR WITH EXISTING WORK.

Reference	H.-P Le 2013 [14]	R. Jain 2014 [15]	M. Abdelfattah 2015 [16]	This work
Technology	65 nm	22 nm trigate	45 nm SOI	45 nm
Input voltage	3-4V	1.23V	1.15V	1.15V
Output voltage	1V	0.45-1V @88mA	0.5V @5-125mA	0.5V @65-130mA
Power efficiency	73%	70%@0.55V 84%@1.1V	74-80% @5-125mA	84.4% @100mA
Response time	N/A	3-5ns	3-95ns	<20ns
Current density	0.19 A/mm^2	0.88 A/mm^2	1.25 A/mm^2	1 A/mm^2
Ripple voltage	N/A	60mV	62mV	Max:22 mV Min:9 mV

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