Closed-Form Expressions for I/O Simultaneous Switching Noise Revisited

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***Abstract*— Closed-form expressions to estimate power supply noise due to the simultaneous switching of I/O drivers are revisited in this brief. It is shown that existing closed-form expressions share a common limitation and underestimate noise with up to 83% error in advanced nanoscale technologies with fast signal rise/fall times. This characteristic is investigated, both quantitatively and qualitatively. New closed-form expressions are developed for the signals with fast transition times. Results demonstrate that the proposed closed-form expressions exhibit an average error of 3.3% as compared with SPICE simulations, and enhance the accuracy of the existing expressions by up to 79.4%.**

***Index Terms*— Integrated circuit interconnections, integrated circuit modeling, RLC circuits, very large scale integration.**

I. Introduction

Power integrity has long been a primary concern in the design of high-performance integrated circuits. As shown in Fig. 1, large and fast transient current drawn by the simultaneous switching of the output I/O drivers and internal logic gates flows through a nonideal power distribution network, causing considerable voltage fluctuations [1]. Excessive noise not only degrades the circuit performance (due to the impact on the timing characteristics of the critical paths) but also causes functional failure [2]–[4].

Closed-form expressions have attracted considerable attention to analytically determine simultaneous switching noise (SSN) [5]–[13]. Unlike simulation-based methods, analytical models provide intuition on the effect of various circuit characteristics and are more applicable to different optimization frameworks.

However, as described in this brief, all the previous closed-form expressions [5]–[13] share a common limitation/assumption that makes these expressions significantly inaccurate when the signal transitions are fast. A new modeling methodology is developed to fix this limitation and enhance the accuracy of previous methods for nanoscale technology nodes with signal transition times in the range of several tens of picoseconds.

The rest of this brief is organized as follows. A summary of the previous work is provided in Section II. The relationship between the damping characteristics and the peak power supply noise is investigated in Section III with an emphasis on input transition time. The proposed modeling methodology and the closed-form expressions are provided in Section IV. Simulation results are presented in Section V to evaluate the proposed model. This brief is concluded in Section VI.

II. Summary of Previous Works

In the existing closed-form expressions, the SSN is typically modeled using the schematic shown in Fig. 2 [5]–[11]. Inductance L, resistance R, and capacitance C represent the parasitic impedances of the power network. The switching circuit is represented by CMOS gates. The input is a saturated ramp signal with transition time t_r. The time interval between t_0 and t_r is referred to as the transition period, whereas the time interval after t_r is referred to as the posttransition period.

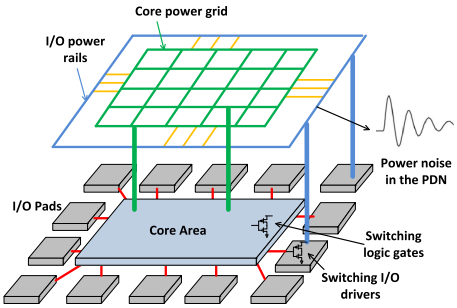

Fig. 1. Power distribution network for the core area and I/O pads.

Senthinathan *et al.* [5], [6] investigated the negative feedback effect between the ground noise and the switching current. In this model, switching current during the transition period is represented by a triangular wave, which is not sufficiently accurate. Furthermore, only the parasitic inductance L has been considered. Vaidyanath *et al.* [7] used a similar modeling approach as in [5] and [6]. It has been assumed that the power supply noise linearly increases during the transition period, which can cause considerable inaccuracy, as shown in this brief. Vemuru [8] adopted Sakurai's α-power law model [14] and assumed that the first-order derivative of the transistor current is constant in submicrometer technologies. Tang and Friedman [9] used a polynomial expansion approximation to obtain a closed-form expression for the SSN, also utilizing the α-power law model.

A primary limitation in all these works, i.e., [5]–[9], is the assumption that the peak noise occurs at the end of input signal transition, i.e., at $t = t_r$ in Fig. 2. As demonstrated in this brief, this assumption does not hold if the input signal transition time is sufficiently fast, as typically encountered in modern technologies.

In a relatively more recent work, Ding and Mazumder [10] discussed the effect of parasitic capacitance on the damping characteristics of an inductive power network. It has been indicated that under a certain range of parasitic capacitance, the system is underdamped during the transition period. The peak noise, therefore, does not occur at the end of transition, but at the first local maximum within the transition period. Hekmat *et al.* [11] improved the model in [10] by also considering the parasitic resistance.

More recently, closed-form expressions have been developed to estimate the power supply noise at the package and board levels [12], [13]. These works, however, have not considered the nonlinear on-chip switching circuit characteristics.

A. Contributions of This Brief

None of the previous works mentioned earlier have investigated the damping characteristics after the transition is over, i.e., within the posttransition period in Fig. 2. When the transition time of input signal is short, the SSN can continue increasing after the transition is complete. Thus, analysis of the power supply noise only within the transition period can significantly underestimate the peak noise under specific damping conditions, as described in this brief.

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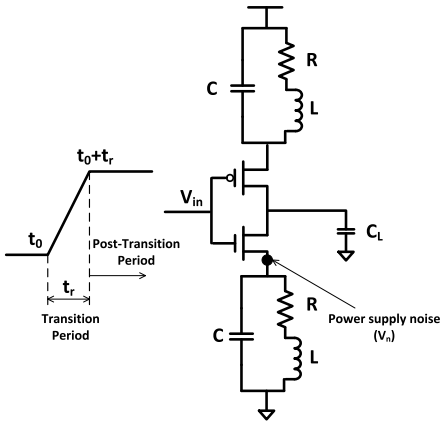


Fig. 2. Equivalent circuit typically used in existing work to develop closed-form expressions for power supply noise.

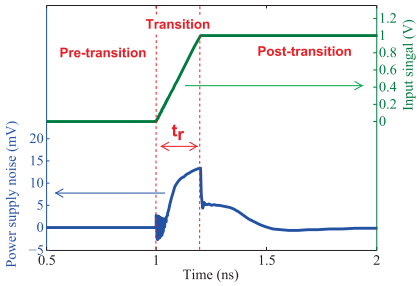


Fig. 3. Transient power supply noise waveform when parasitic capacitance is ignored: $R = 5\ \Omega$, $L = 1$ nH, $W_n = 1\ \mu$m and $W_p = 2\ \mu$m, transition time t_r is 200 ps, and output load capacitance is 1 pF.

According to the best of our knowledge, this brief is the first study that demonstrates this phenomenon and provides accurate closed-form expressions for SSN when the input transition times are sufficiently short.

Note that the proposed closed-form expressions are not intended for core area power supply noise analysis due to highly distributed characteristics (see Fig. 1). Instead, these expressions can be utilized to estimate the SSN caused by on-chip I/O drivers (which typically have a separate, routed power rail) or power supply noise at the package/board levels where lumped modeling is a typical practice [12], [13].

III. Motivational Example

A motivational example is provided to illustrate the effect of damping and input transition time on the peak noise characteristics. The power supply noise (voltage at the source node of the nMOS transistor) generated by a CMOS inverter in a 45-nm technology is analyzed. A saturated ramp signal is used as the input signal to the inverter.

In case 1, the schematic is simulated when the input transition time is 200 ps while ignoring the parasitic capacitance C, similar to [5] and [6]. The transient noise waveform is shown in Fig. 3. Since C is not considered, the circuit represents a first-order system (ignoring the transistor parasitic capacitances), and the power noise decreases after the transition. Thus, if parasitic capacitance is ignored, peak supply noise occurs at the end of transition, as assumed in the existing work.

In case 2, the same circuit is simulated using a parasitic capacitance C of 1 pF, also with 200 ps input transition time. Since the circuit is now a second-order system, the damping behavior depends upon the R, L, and C impedances and transistor characteristics. In this specific case, as shown in Fig. 4(a), the system is underdamped. Peak noise does not occur at the end of transition. Instead, the peak noise occurs at the first local maximum of the decaying sine wave, as also observed in [10].

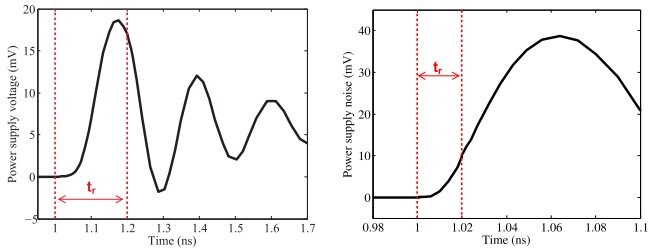


Fig. 4. Transient power supply noise waveform when $R = 5\ \Omega$, $L = 1$ nH, $C = 1$ pF, $W_n = 1\ \mu$m, $W_p = 2\ \mu$m, and output load capacitance is 1 pF. The transition times are (a) $t_r = 200$ ps and (b) $t_r = 20$ ps.

In case 3, the same circuit is simulated, but the transition time t_r is reduced from 200 to 20 ps. The transient noise waveform is shown in Fig. 4(b). As shown in Fig. 4(b), when the transition time is shorter, the power supply noise does not reach the first local maximum within the transition. Alternatively, the noise continues to increase and reaches the peak value within the posttransition period. Therefore, modeling the system only until $t = t_0 + t_r$ significantly underestimates the peak noise (by 73.8% in this example). It is therefore highly important to consider the circuit damping and noise characteristics after the input transition is complete.

This characteristic can be intuitively described by considering the extreme case when the gate input is a step signal with zero transition time. In this extreme case, the peak noise would always occur after the (zero) transition period. Since the system reacts to the step function with natural response, when the input transition time is sufficiently short, it is again expected that the peak noise would occur after the transition period. Since the input signal function is different within the transition and posttransition periods, the system damping behavior needs to be modeled separately, as described in Section IV.

IV. Proposed Model

A. Proposed Closed-Form Expressions

The transition period ($t_0 < t < t_r$) can be modeled by using an existing method (such as [11]), while considering all the R, L, and C parasitic impedances. Two important transient circuit characteristics need to be determined from the transition period that serve as the initial conditions for the analysis of the posttransition period: 1) the power supply noise (see Fig. 2) at the end of transition $V_{n(t=t_r+t_0)}$ and 2) the current flowing through the capacitance $I_{c(t=t_r+t_0)} = CdV_n/dt$.

Referring to Fig. 2, since pMOS current is negligible when the input signal is stable at high voltage during the posttransition period, current through the pMOS transistor is ignored. Similar to [10] and [11], an application specific device modeling methodology for MOS transistors is used. At relatively large load capacitances, the drain-to-source voltage V_{ds} of the nMOS transistor is larger than $V_{gs} - V_{th}$ when the peak noise occurs during the posttransition period (i.e., nMOS transistor is in saturation region when the peak noise is reached). Thus, the accuracy is not affected if the nMOS transistor goes into linear region after the peak noise is reached. Note that this assumption holds particularly for I/O drivers where the load capacitances are typically high. Thus, the drain current I_{ds} increases

approximately linearly with V_{gs}. A linear equation is therefore used to predict the nMOS current in saturation region

$$I = K_1(V_{\text{in}} - V_n - V_0) \tag{1}$$

where K_1 and V_0 are the constant parameters determined from experimental or simulation data. V_n is the voltage of the source node of the nMOS transistor, representing the power supply noise. When a large number of I/O drivers is in parallel, a parameter N is used as the effective number of I/O gates that switches simultaneously. Therefore, the overall drain current and the inductor current of those N gates during the posttransition period are

$$I_N = NK_1(K_2 - V_n) \text{ and } I_L = I_N - C\frac{dV_n}{dt} \tag{2}$$

where K_2 is $V_{\text{DD}} - V_0$, since the gate input voltage is stable at V_{DD} during the posttransition period. The damping characteristics of the system can be investigated by

$$V_n = RI_L + L\frac{dI_L}{dt} \tag{3}$$

where I_L and I_C are, respectively, the transient current flowing through inductance L and capacitance C. Solving (2) and (3) together, the following expression is obtained:

$$LC\frac{dV_n^2}{dt^2} + (RC + LNK_1)\frac{dV_n}{dt} + (RNK_1 + 1)V_n = RNK_1K_2. \tag{4}$$

The particular solution of (4) is in the form of $V_p = B_0$, where B_0 is

$$B_0 = \frac{RNK_1K_2}{RNK_1 + 1}. \tag{5}$$

The characteristic equation of (4) is

$$LCr^2 + (RC + LNK_1)r + (RNK_1 + 1) = 0. \tag{6}$$

The discriminant of the characteristic equation is

$$\Delta = (RC - LNK_1)^2 - 4LC. \tag{7}$$

Depending on the magnitude of (7), the system is either underdamped, overdamped, or critically damped.

1) Underdamped Case: If $\Delta < 0$, the system is underdamped, and the power supply noise during the posttransition period can be expressed as

$$V_n = e^{-\alpha t}(B_1 \cdot \cos\omega_d t + B_2 \cdot \sin\omega_d t) + B_0 \tag{8}$$

where

$$\alpha = \frac{RC + LNK_1}{2LC} \text{ and } \omega_d = \sqrt{\frac{RNK_1 + 1}{LC} - \alpha^2}. \tag{9}$$

B_1 and B_2 are two coefficients determined from the initial conditions

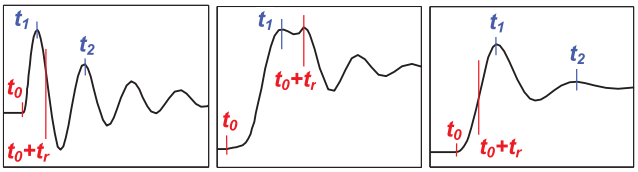
$$B_1 = V_{n(t=t_r)} - B0 \text{ and } B_2 = \frac{I_{c(t=t_r)}/C + \alpha B_1}{\omega_d}. \tag{10}$$

2) Overdamped Case: If $\Delta > 0$, the system is overdamped. The power supply noise can be expressed as the sum of general and particular solutions of (4)

$$V_n = A_1e^{\lambda_1 t} + A_2e^{\lambda_2 t} + B_0 \tag{11}$$

where

$$\lambda_{1,2} = -\frac{RC + LNK_1}{2LC} \pm \sqrt{\left(\frac{RC + LNK_1}{2LC}\right)^2 - \frac{RNK_1 + 1}{LC}}. \tag{12}$$



(a) (b) (c)

Fig. 5. Illustrative examples on the occurrence time of peak power supply noise in underdamped case. (a) Peak noise occurs within the transition period. (b) Peak noise occurs at end of the transition period. (c) Peak noise occurs within the posttransition period.

B_0 is the particular solution as provided by (5). A_1 and A_2 are the two coefficients determined from the initial conditions

$$A_1 = \frac{I_{c(t=t_r)}/C - (V_{n(t=t_r)} - B_0)\cdot\lambda_2}{\lambda_1 - \lambda_2} \tag{13}$$

$$A_2 = V_{n(t=t_r)} - B_0 - A_1. \tag{14}$$

Using (8) and (11), the voltage noise waveform and the peak power supply noise for the posttransition period can be determined. Note that when $\Delta = 0$, the system is critically damped. In this case, power supply noise can be estimated by either (8) or (11).

B. Effect of Input Transition Time on Peak Power Supply Noise

The effect of signal transition time on the peak noise characteristics can be analyzed using the proposed model. This analysis is important to determine the boundary transition time for which the proposed expressions are required.

1) Underdamped Case: According to [11], if the system is underdamped, the power supply noise waveform during the transition period ($t_0 < t < t_r$) is predicted by

$$\begin{aligned} V_n &= e^{-\alpha t'}(B_1' \cdot \cos\omega_d t' + B_2' \cdot \sin\omega_d t') + at' + b \\ &= e^{-\alpha t'}\sqrt{B_1'^2 + B_2'^2}\sin\left(\omega_d t' + \arctan\frac{B_2'}{B_1'}\right) + at' + b \end{aligned} \tag{15}$$

where $t' = t - t_0$ and $t_0 = tV_0/V_{DD}$. B_1', B_2', a, and b are determined by the initial conditions. Therefore, the noise waveform during the transition period is a decaying sine wave superposed with a linearly increasing term $at' + b$. The local maxima of the waveform occur at $t = t_n$ ($n = 1, 2, \ldots$) that satisfy

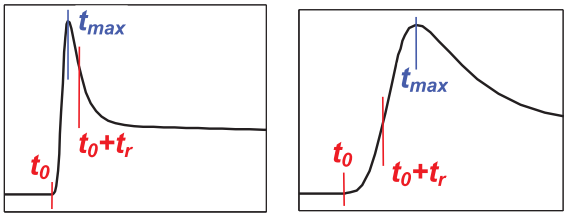
$$\omega_d(t - t_0) + \arctan\frac{B_2'}{B_1'} = 2n\pi - 3/2\pi \quad (n = 1, 2, \ldots). \tag{16}$$

According to [10], if the parasitic resistance R is not considered, the linearly increasing term $at' + b$ in (15) is reduced to a constant term. Therefore, the power supply noise at a local maximum is always smaller than its preceding local maximum [$V_n(t_1) > V_n(t_2) > V_n(t_3) > \cdots > V_n(t_n)$]. However, if the parasitic resistance R is included in the model, it is possible that a local maximum is larger than or equal to its preceding local maximum [e.g., $V_n(t_3) > V_n(t_2)$], due to the linearly increasing term in (15).

Alternatively, during the posttransition period, as investigated in this brief, the particular solution of (8) is constant, since the gate input signal is in steady state. The power supply noise waveform during the posttransition period is represented by a decaying sine wave superposed with a constant term. Therefore, if $t_r > t_1$, the peak noise can occur either at one of the local maxima t_n [see Fig. 5(a)] or at the end of transition period t_r [see Fig. 5(b)]. Alternatively, if $t_r < t_1$, the noise continues to increase after $t = t_r$. The peak power supply noise occurs at the first local maximum within the posttransition period, as predicted by the proposed closed-form expression (8) [see Fig. 5(c)].

TABLE I
COMPARISON OF THE SIMULATED AND ESTIMATED PEAK POWER SUPPLY NOISE FOR A VARIETY OF *RLC* IMPEDANCES WHEN $N = 100$ AND $t_r = 50$ ps

Parasitic impedances			SPICE	Ding [10]		Hekmat [11]		This paper	
R (Ω)	L (pH)	C (pF)		Peak (mV)	Error (%)	Peak (mV)	Error (%)	Peak (mV)	Error (%)
0.5	100	5	45.13	29.79	-33.99	30.02	-33.49	42.97	-4.79
		10	34.82	16.83	-51.67	16.89	-51.50	32.83	-5.73
	500	5	100.60	35.18	-65.03	35.19	-65.02	94.92	-5.64
		10	75.37	18.27	-75.76	18.28	-75.75	70.56	-6.38
	1000	5	136.60	35.90	-73.72	35.90	-73.72	128.31	-6.07
		10	102.80	18.46	-82.04	18.16	-82.04	96.03	-6.59
1	100	5	46.70	29.79	-36.21	30.23	-35.26	44.63	-4.43
		10	36.25	16.83	-53.58	16.95	-53.25	34.48	-4.87
	500	5	101.50	35.18	-65.34	35.20	-65.32	96.12	-5.30
		10	76.52	18.27	-76.12	18.28	-76.11	71.88	-6.06
	1000	5	137.70	35.90	-73.93	35.91	-73.92	129.38	-6.05
		10	103.70	18.46	-82.20	18.46	-82.20	97.24	-6.23
5	100	5	63.49	29.79	-53.08	31.58	-50.25	62.21	-2.01
		10	55.39	16.83	-69.62	17.31	-68.75	55.15	-0.44
	500	5	111.50	35.18	-68.45	35.27	-68.36	106.83	-4.19
		10	86.92	18.27	-78.98	18.30	-78.95	84.25	-3.07
	1000	5	145.40	35.90	-75.31	35.93	-75.29	138.46	-4.77
		10	112.60	18.46	-83.61	18.47	-83.60	107.89	-4.18
Average error (%)				-66.59		-66.26		-4.82	
Maximum error (%)				-83.61		-83.60		-6.59	



(a) (b)

Fig. 6. Illustrative examples on the occurrence time of peak power supply noise in overdamped case. (a) Peak noise occurs within the transition period. (b) Peak noise occurs within the posttransition period.

2) Overdamped Case: If the system is overdamped, the power noise during the transition period is predicted by

$$V_n = A_1' e^{\lambda_1 t'} + A_2' e^{\lambda_2 t'} + at' + b \tag{17}$$

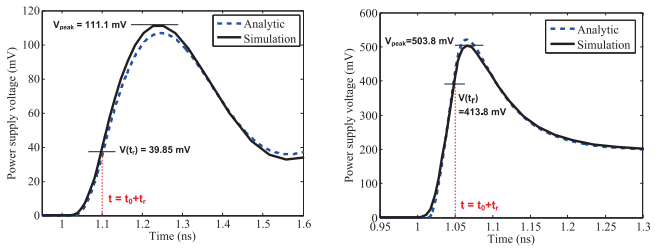
where $t' = t - t_0$. A_1' and A_2' are determined by the initial conditions of the transition period. a and b are the same as in (15). Thus, a single $t = t_{\max}$ exists that satisfies

$$\frac{dV_n}{dt'} = 0 \Longrightarrow A_1'\lambda_1 e^{\lambda_1 t'} + A_2'\lambda_2 e^{\lambda_2 t'} + a = 0. \tag{18}$$

The noise first increases monotonically until $t = t_{\max}$ and then decreases monotonically. Therefore, if t_r is larger than $t_{\max}$, the peak noise occurs before $t = t_0 + t_r$, as shown in Fig. 6(a). Alternatively, if t_r is smaller than $t_{\max}$, the noise monotonously increases during the transition period, and continues to increase within the posttransition period, as shown in Fig. 6(b). The validation of the proposed closed-form expressions with SPICE and comparison with existing models are provided in Section V.

V. SIMULATION RESULTS

To evaluate the proposed model, the schematic shown in Fig. 2 is simulated with a 45-nm CMOS technology using SPICE [15]. For a single inverter, W_n=100 nm, W_p=200 nm, and L=50 nm. To investigate the effect of number of simultaneously switching gates on power noise, N inverters are considered where N varies from 100 to 5000.



(a) (b)

Fig. 7. Comparison of the power supply noise predicted by the proposed expressions and SPICE simulations in a) underdamped and b) overdamped.

A. Estimation of the Power Supply Noise Waveform

1) Underdamped Case: The simulation results are compared with (8) for an underdamped case where $R = 5\ \Omega$, $L = 1$ nH, $C = 10$ pF, $N = 100$, and $t_r = 100$ ps. The comparison is shown in Fig. 7(a), demonstrating an average error of less than 5%. Note that since $t_r < t_1$ (see Section IV-B1), the noise does not reach the first local maximum at $t = t_0 + t_r$. Instead, the noise continues to increase during the posttransition period, reaching up to 111.1 mV. Thus, if the noise at $t = t_0 + t_r$ (39.85 mV) is used as the peak noise, as in previous works, the peak noise is underestimated by 64.1%.

2) Overdamped Case: The simulation results are compared with (11) for an overdamped case where $R = 5\ \Omega$, $L = 1$ nH, $C = 1$ pF, $N = 500$, and $t_r = 50$ ps. According to Fig. 7(b), the proposed closed-form expression accurately predicts the power supply noise with an error less than 4%. Similar to the underdamped case, estimating the peak noise at $t = t_0 + t_r$ underestimates the actual peak noise by 17.8%.

B. Estimation of the Peak Noise

The peak power supply noise predicted by the proposed closed-form expressions (8) and (11) is compared with the simulation results (SPICE), and the models proposed in [10] and [11] for a variety of *RLC* impedances. Error is calculated with respect to SPICE simulations. The results are listed in Table I.

As listed in Table I, the proposed expressions significantly enhance the accuracy in estimating the peak noise as compared with existing

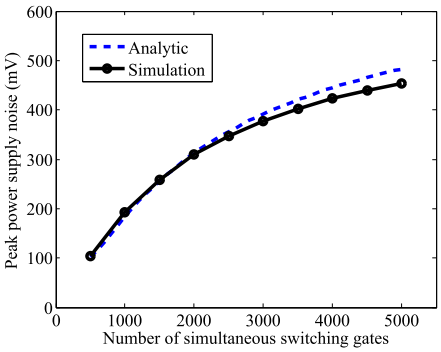


Fig. 8. Comparison of the peak power supply noise predicted by the proposed expressions and obtained by the SPICE simulations as the number of simultaneously switching gates increases.

models. Specifically, in Table I, the maximum error of the proposed model is 6.59% whereas the maximum error for [10] and [11] are, respectively, 83.61% and 83.60%. Similarly, the average error of the proposed model over all the cases is 4.82% whereas the average error for [10] and [11] are, respectively, 66.59% and 66.26%. Note that the slight underestimation is due to the linear approximation of the nMOS current [see (1)] in saturation region, which neglects the channel length modulation.

Finally, the accuracy of the model is evaluated when the number of simultaneously switching gates is increased (up to 5000). As shown in Fig. 8, peak noise is accurately estimated with an error less than 6%, and the proposed model can capture the negative feedback between supply current and power supply noise.

VI. Conclusion

Existing closed-form expressions to estimate SSN suffer from a common limitation if the signal transition times are fast, as commonly encountered in nanoscale technology nodes. This limitation has been described both quantitatively and qualitatively. New closed-form expressions have been developed, exhibiting a maximum error of 6.59% as compared with SPICE. The accuracy of existing models has been enhanced by up to 79%.

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