Low Swing TSV Signaling using Novel Level Shifters with Single Supply Voltage

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***Abstract*—Low swing TSV signaling is proposed for three-dimensional (3D) integrated circuits (ICs) to reduce dynamic power consumption. Novel level shifters are designed to lower the voltage swing before the TSV and to pull the voltage swing back to full rail at the far end of the TSV. Proposed level shifters operate with a single supply voltage, thereby reducing the overall cost. Critical TSV capacitance beyond which the proposed scheme saves dynamic power is determined. Up to 42% reduction in overall power is demonstrated with a voltage swing of 0.5 V, where the supply voltage is 1 V.**

I. Introduction

Three-dimensional (3D) integration is a promising technology to achieve higher integration density and reduce the global interconnect length (therefore reducing delay and power dissipation) [1], [2]. The essential component of 3D ICs is the through silicon vias (TSV) that connect different planes and provide data, clock, and power transfer among the planes.

In modern 3D IC processes, TSV dimensions (such as diameter and height) are still relatively large as compared to on-chip wires and transistors [3]. Thus, TSVs significantly contribute to overall capacitance which results in high delay and dynamic power consumption [4]. The primary objective of this study is to reduce the dynamic power consumed by TSVs through low swing TSV signaling. The proposed low swing scheme is achieved by using a single supply voltage, thereby reducing the overall cost and power grid complexity. A novel, single voltage level-down shifter is proposed. The proposed shifter outperforms existing single voltage shifters in terms of power consumption. Up to 42% reduction in dynamic power is demonstrated through low swing TSV signaling in a 45 nm 3D IC technology.

The rest of the paper is organized as follows. Background information on low swing operation is provided in Section II. Previous work on level shifters is summarized in Section III. The proposed level-down shifter and modified level-up shifters are described in Section IV. The simulation results are presented in Section V. Finally, the paper is concluded in Section VI.

II. Background

The proposed technique is depicted in Fig. 1. Full swing input signal is converted into a low swing signal through a novel level-down shifter proposed in this paper. After the TSV, the signal is restored to full rail through a level-up shifter. Both shifters operate with a single supply voltage, thereby reducing the complexity of the power supply and power grid design. Thus, an additional power supply and grid are not required to achieve the proposed low swing TSV signaling scheme. It is important to note that the level shifting circuits consume power which decreases the overall power savings achieved through low swing signaling. The power overhead of these shifters should therefore be sufficiently low. Furthermore, in single supply voltage implementations, as targeted in this work, satisfying leakage current (particularly in the level-up stage), delay, and output slew is challenging. A novel level-down shifter is proposed in this work with enhanced performance. Several variations of existing level-up shifters are also developed that trade leakage power for delay.

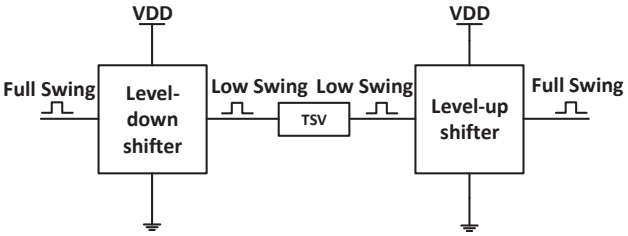

Fig. 1. **Conceptual representation of low swing TSV signaling with level shifters operating with a single supply voltage.**

III. Previous Work

Most of the existing level shifters require multiple supply voltages [5]–[8]. An example of a level shifter with a single supply voltage has been proposed in [9]. This circuit utilizes a chain of buffers to generate a delay time. The output of the delay chain determines the amount of time that the output is charged (or discharged), thereby lowering the swing voltage. The delay chain consumes significant power since each node within the chain switches with the input signal.

Another existing method utilizes an inverter with PMOS transistor in the pull-down network and an NMOS transistor in the pull-up network to reduce the output swing [10]. In this topology, referred to as symmetric source-follower driver, the swing is determined by threshold voltages, preventing the ability to independently adjust the output swing level.

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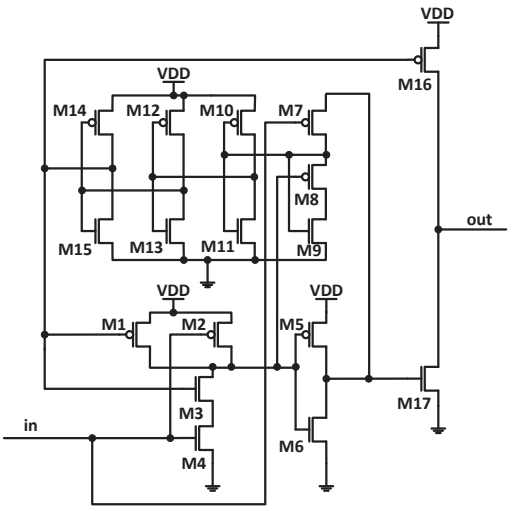


Fig. 2. **Schematic of the proposed level-down shifter.**

IV. Proposed Level Shifters

A. Level-Down Shifter

In this study, a novel level-down shifter is proposed, as illustrated in Fig. 2. This shifter is based on the dynamically enabled drivers discussed in [10], but has a different enabling circuit. The proposed level shifter turns on M16 for a certain amount of time to charge the TSV capacitance to a certain voltage level. The voltage swing can be adjusted by accordingly sizing the transistors within the enabling circuit (adjusts the charging time) and the size of M16 (adjusts the output current). Thus, if the TSV capacitance is known, both charge time and output current are adjusted to obtain the desired voltage swing.

The proposed level-down shifter operates as follows. Transistors M1 to M6 act as a two-input AND gate. One of the inputs is the full swing signal whereas the other input is the output of the enabling circuit. When the input full swing signal transitions from high to low, M7 turns on and pulls the input of M10 and M11 to VDD for a short amount of time determined by the AND gate delay. Next, this signal propagates and turns on M16, charging the output capacitance. Once the input of M17 transitions to ground as determined by the AND gate delay, the input of M10 and M11 transitions to V_{th} of M9, making the input of M16 transition to VDD. The charging process then stops. Thus, the delay of the AND gate and the enabling circuit determines the charge time of the output.

Alternatively, when the full swing input signal transitions from ground to VDD, the output of the AND gate transitions to VDD, turning on M17, which discharges the output to ground. Note that in this case, M7 is off, making the input of M10 and M11 remain at V_{th} of M9. Thus, M16 is off. Also note that transistors M8 and M9 are used to ensure that the input of M10 and M11 remains at V_{th} of M9 when the output of the AND gate is high and full swing input is at VDD. Due to leakage current through M7, the input of M10 and M11 may slightly rise, causing significant leakage power. If there is sufficient increase in voltage at this node, M9 turns on to pull this node to ground, thereby preventing the leakage power.

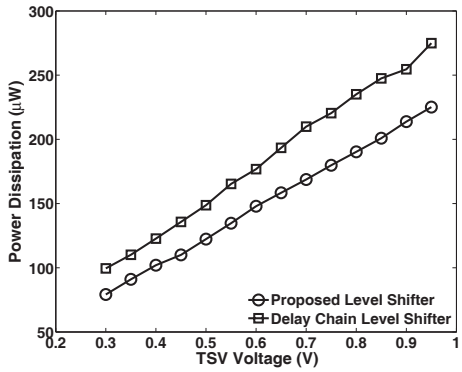


Fig. 3. **Comparison of the proposed and existing [9] level-down shifters.**

The two additional inverters in the enabling circuit (M12 to M15) are used as a cascaded buffer since M16 drives a relatively large TSV capacitance. Thus, slew constraint is maintained. Furthermore, these inverters provide higher delay resolution to fine tune the output voltage swing.

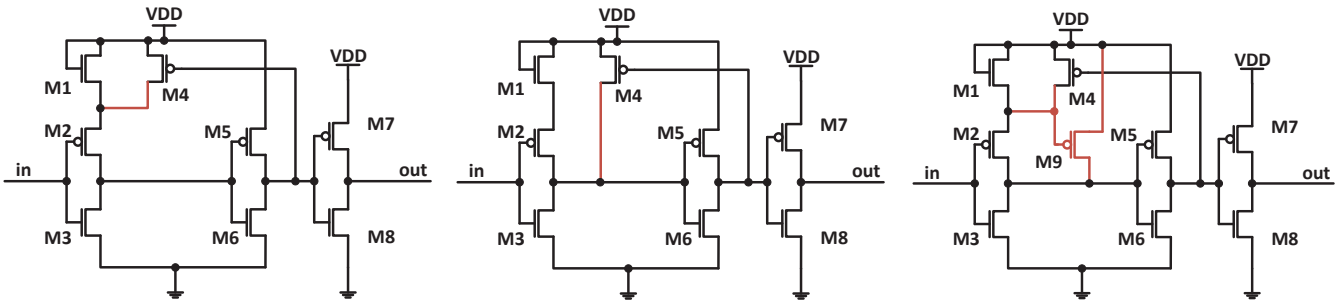
The proposed level shifter consumes less power than the existing single supply topology, proposed in [10]. Both topologies have been designed in a 45 nm technology where the nominal supply voltage is 1 V. The output load is 280 fF. The power dissipation is shown in Fig. 3 as a function of output voltage swing. The proposed topology achieves an average of 18% less power than the existing topology. The number of transistors in both topologies is similar. However, note that in [9], the output stage consists of stacked PMOS and NMOS transistors which require larger size to drive the output load. Alternatively, in the proposed topology, output stage has a single PMOS and NMOS transistor, tolerating smaller sizes.

B. Level-Up Shifter

It is challenging to design a single supply level-up shifter with low leakage current. An example is proposed in [11]. This circuit has a MOS capacitor and a cross-coupled PMOS at the output stage. The MOS capacitor increases the area overhead while also causing high leakage power.

Three level-up shifters are evaluated in this study, as depicted in Fig. 4. The first circuit is proposed in [12] whereas the other two circuits are modified versions of this circuit evaluated in this work. When input signal transitions to ground, M4 eventually turns-on, pulling the source node of M2 to full VDD. Thus, the input of M5/M6 operates at full VDD, significantly reducing the leakage current through M5/M6. When input signal transitions from ground to low swing VDD, M4 turns off and a virtual VDD is generated at the source node of M2, thereby reducing the leakage through M2/M3. The last stage inverter is included to keep the same phase as the input of the level-down shifter. Furthermore, input of M4 is isolated from the output that may have a large capacitive load. Thus, M4 turns on faster.

A disadvantage of this circuit is a relatively high delay when input transitions to ground since it takes certain time for M4 to turn on. This circuit is slightly modified to address this issue, as shown in Figs. 4(b) and 4(c). In Fig. 4(b), the output of M4 is directly connected to the input of M5/M6, thereby



(a) Single voltage level-up shifter proposed in [12] (b) Modified version 2 (c) Modified version 3

Fig. 4. **Level-up shifters evaluated in this work.**

TABLE I
TSV PARASITIC IMPEDANCES [13].

Parameter	Via-middle	Via-last
TSV resistance	858.36 m ohm	20 m ohm
TSV inductance	49.76 pH	34.94 pH
TSV capacitance	117.81 fF	283 fF

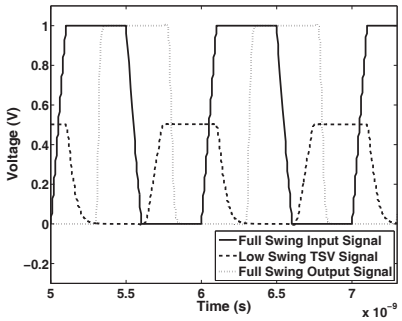


Fig. 5. **Illustration of the correct functionality of the proposed level shifters where the voltage swing for TSV is reduced to 0.5 V.**

Fig. 6. **Conventional, full swing TSV signaling.**

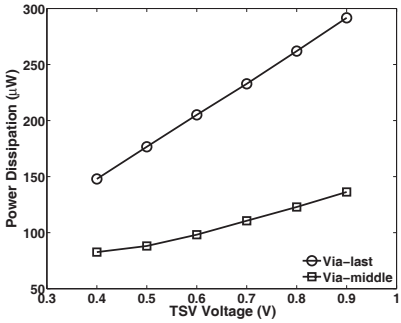


Fig. 7. **Power consumption of low swing TSV signaling as a function of TSV voltage for both via-middle and via-last TSVs.**

charging this node faster at the expense of higher leakage current. In Fig. 4(c), an additional PMOS, M9, is added to store additional charge. Thus, the voltage at the virtual VDD drops slower when the input transitions to ground. If the virtual VDD voltage sufficiently drops, M9 turns on and pulls the input of M5/M6 to full VDD before M4 turns on. Thus, delay is further improved. This method also trades leakage power for reducing delay, as quantified in the following section.

V. Simulation Results

The proposed level-down and level-up shifters are designed in a 45 nm technology with 1 V power supply voltage. The simulation setup is similar to Fig. 1. The incoming signal has full swing with 100 ps transition times and switch at 1 GHz frequency. The voltage swing can be reduced down to 0.4 V by using the proposed level shifters. The level-up shifter drives a load capacitance of 5 fF. The TSV is modeled as a distributed *RLC* circuit with the TSV impedances listed in Table I [13]. The signal waveforms are illustrated in Fig. 5 for a via-last TSV when the voltage swing is 0.5 V, demonstrating the functionality of the proposed level shifters.

A. Comparison with Conventional Full Swing Signaling

To compare the power consumption with conventional full swing signaling, the circuit shown in Fig. 6 is also designed where the incoming signal is the same and output stage drives the same amount of capacitance. This conventional system consumes an overall power of 303.4 μW and 129.8 μW with, respectively, a via-last and via-middle TSV. The power consumed by low swing TSV signaling using the proposed level shifters is illustrated in Fig. 7 as a function of voltage swing for both via-last and via-middle TSVs. According to this figure, when the TSV swing is 0.5 V, low swing TSV signaling achieves 41.8% and 32.1% reduction in, respectively, via-last and via-middle TSVs.

B. Quantification of Critical TSV Capacitance

It is important to determine the amount of TSV capacitance beyond which low swing signaling can reduce power consumption. The power consumed by low swing (0.5 V) TSV signaling as a function of TSV capacitance is depicted in Fig. 8. As shown in this figure, as TSV capacitance increases, low swing signaling can achieve significant power savings. If the TSV capacitance is larger than 240 fF, as for modern via-last processes [13], more than 40% reduction is achieved through low swing signaling. Fig. 9 zooms in the values that correspond to low TSV capacitances. As demonstrated in Fig. 9, a critical capacitance exists beyond which low swing signaling starts saving power. Specifically, for the proposed level shifters, this critical TSV capacitance is approximately 32 fF. Since typical TSVs have much larger capacitances than this value, the proposed level shifters can effectively save

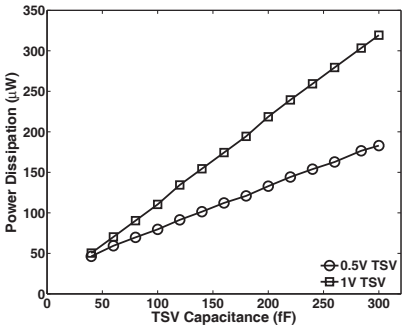


Fig. 8. **Power consumption as a function of TSV capacitance when voltage swing is 0.5 V.**

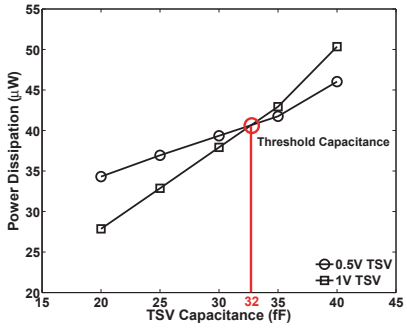


Fig. 9. **Critical TSV capacitance beyond which low swing TSV signaling achieves power savings when low swing voltage level is 0.5 V.**

dynamic power. The critical TSV capacitance also depends upon the voltage swing, as shown in Fig. 10. According to this figure, even when the voltage swing is not sufficiently low, the critical TSV capacitance is still smaller than the TSV capacitance in modern 3D processes. For example, at a swing of 0.6 V, the critical capacitance is approximately 40 fF.

C. Tradeoff between Leakage Power and Delay

The two modified level-up shifters described in Section IV-B are also simulated to evaluate the tradeoff between leakage current and delay. The results are listed in Table II. The original level-up shifter has the lowest leakage current with a relatively high delay. The modified versions have slightly larger (but still within a few hundred nanoamps) leakage current while achieving approximately 20% reduction in delay. Note that higher reduction in delay can be achieved through

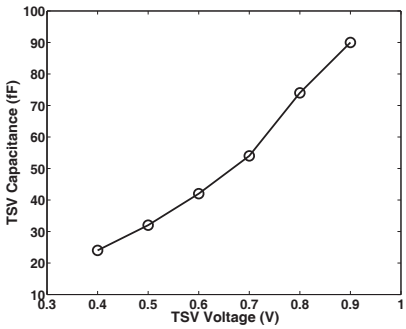


Fig. 10. **Dependence of critical TSV capacitance on voltage swing.**

TABLE II
LEAKAGE POWER AND DELAY FOR DIFFERENT VERSIONS OF THE LEVEL-UP SHIFTER WITH VIA-LAST TSV AT A VOLTAGE SWING OF 0.5 V.

	Input high	Input low	Delay
[12]	50.05 nW	109.7 nW	264.9 pS
Version 2	108.2 nW	137.2 nW	226.1 pS
Version 3	106.3 nW	173.1 nW	216.1 pS

transistor sizing at the expense of higher leakage power (in the range of half microamps).

VI. CONCLUSIONS

Low swing TSV signaling has been proposed to save significant dynamic power since existing 3D technologies typically suffer from large TSV capacitances. Novel level shifters operating with a single supply voltage have been proposed. Single supply voltage significantly reduces the overall system cost. Up to 42% reduction in power has been demonstrated in a 45 nm technology (1 V supply voltage) with a voltage swing of 0.5 V. Critical TSV capacitance beyond which the proposed level shifters can save power has also been characterized. It has been shown that the critical TSV capacitance is smaller than the practical TSV capacitances in modern 3D processes, making the proposed scheme highly applicable to existing 3D technologies.

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