Enhanced Level Shifter for Multi-Voltage Operation

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***Abstract*—A novel level-up shifter with dual supply voltage is proposed. The proposed design significantly reduces the short circuit current in conventional cross-coupled topology, improving the transient power consumption. Compared with the bootstrapping technique, the proposed circuit consumes significantly less area, making it more practical for ICs with a large number of supply voltages. The minimum power-delay product (PDP) for each level shifter is analyzed and compared. Worst-case corner analysis is performed for transient power, delay, and leakage power. The dependence of power and delay on input supply voltage level is also investigated for each topology. Simulation results demonstrate 43% and 36% reduction in, respectively, transient power and leakage power as compared to cross-coupled level shifter, while consuming 9.5% and 79.5% less physical area than, respectively, cross-coupled and bootstrapping techniques.**

I. INTRODUCTION

Reducing power consumption is a major objective for almost any application [1]. Multiple supply voltages and dynamic voltage (and frequency) scaling (DVFS) are common techniques to achieve significant reduction in power with minimal overhead in performance [2], [3]. For both of these techniques, level shifters play an important role due to the signals that cross different voltage islands. When a low voltage signal is interfaced with a higher voltage domain, the voltage level should be increased with minimum overhead in power, area, and delay. The power consumed during level shifting reduces the overall power savings achieved by multiple supply voltages and DVFS. Furthermore, level shifters are also used in clock networks to achieve low swing clocking with significant power savings [4]–[6]. The delay of the level shifters is also important in this application since a larger delay increases the overall clock insertion delay, making the clock network more sensitive to variations.

Existing level shifters can be categorized under two primary classes: 1) shifters based on conventional, cross-coupled topology with differential output [7], [8], 2) shifters based on bootstrapping [9], [10]. Shifters in the first group enhance the delay of the level shifting by exploiting cross-coupled PMOS transistors whereas shifters in the second group enhance the power consumption by reducing the swing at the internal voltage nodes. In some applications where sub-threshold circuits are interfaced with super-threshold operation, wide range level shifters are required, as proposed in [8], [11]. Level shifters with a single supply voltage have also been proposed [12]–[14]. However, shifting voltage swing with a single supply voltage typically produces large leakage current and long signal transition times.

The proposed level shifter reduces the transient power of conventional cross-coupled topology while consuming significantly less area as compared to bootstrapping technique. A relatively fast response is also achieved. The rest of the paper is organized as follows. Conventional cross-coupled level shifter and bootstrapping techniques are summarized in Section II. The proposed level shifter is described in Section III. Simulation results and related discussion are presented in Section IV. Finally, paper is concluded in Section V.

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II. BACKGROUND

A conventional buffer consisting of two inverters powered by the lower supply voltage V_{ddL} can reliably function as a level-down shifter since there is no short circuit or leakage issue [4]. A conventional buffer, however, cannot reliably function as a level-up shifter since the incoming signal with a lower supply voltage drives inverters powered with a higher supply voltage. This situation causes unreasonably high short circuit and leakage current that is not tolerable in most of the applications. For example, in 45 nm technology, if a conventional buffer is used as a level-up shifter, short circuit current is approximately 31% of the overall power consumption while leakage current is in the range of microamps. The traditional cross-coupled topology and bootstrapping technique are summarized in, respectively, Sections II-A and II-B.

A. Cross-coupled Level Shifter

Conventional level shifter using cross-coupled PMOS transistors is depicted in Fig. 1(a). As shown in this figure, the incoming low voltage signal is inverted using an inverter connected to a low voltage domain, V_{ddL}. Cross-coupled PMOS transistors P1 and P2 are used to pull output to the high voltage, V_{ddH}. Leakage issue of the conventional buffer is alleviated since P1 and P2 are not driven by the incoming signal. However, this topology exhibits relatively high short circuit current during transition (either through P1 and N1 or through P2 and N2) even when the input transitions are fast.

B. Bootstrapping Level Shifter

Bootstrapping technique, as depicted in Fig. 1(b), has been proposed to reduce the transient power during level shifting.

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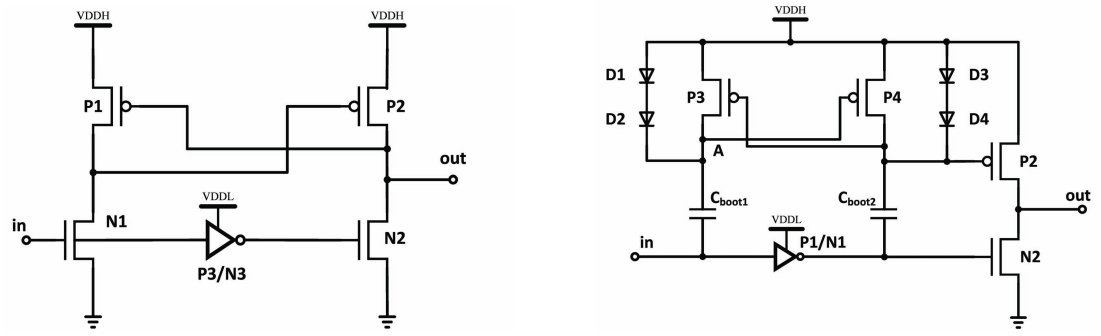
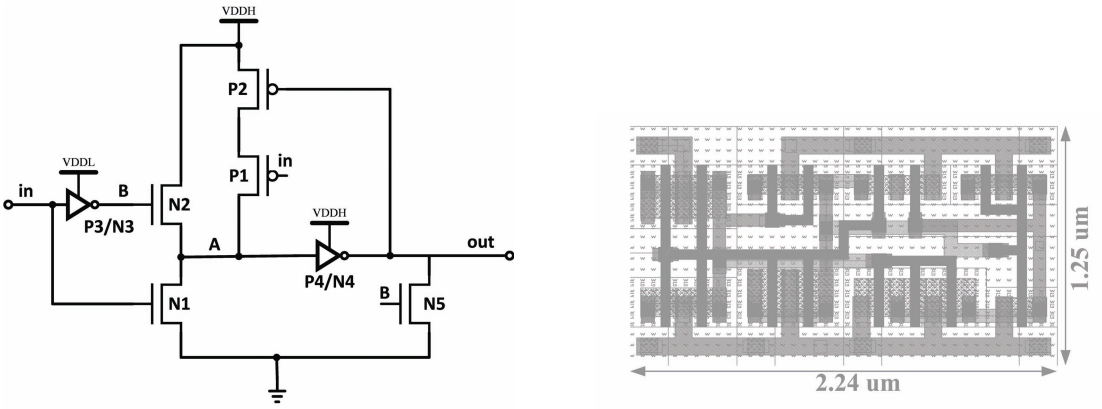


(a) (b)

Fig. 1. **Existing level shifters: (a) conventional cross-coupled topology, (b) bootstrapping technique.**



(a) (b)

Fig. 2. **Proposed level shifter: (a) schematic, (b) physical layout.**

Voltage swing at specific nodes is reduced, thereby saving power [10]. In Fig. 1(b), two boot capacitors C_{boot1} and C_{boot2} replace NMOS transistors to maintain the voltage difference at the gate terminals of P2 and N2. Thus, the pull-down NMOS N2 at the output stage is driven between 0 and V_{ddL} whereas the pull-up PMOS is driven between $V_{ddH} - V_{ddL}$ and V_{ddH}. Bootstrapping technique achieves lower power at the expense of significant increase in physical area due to the relatively large boot capacitors, determined by

$$C_{boot1} = C_A \frac{2V_{diode}}{V_{ddL} - 2V_{diode}}, \quad (1)$$

where C_A is total capacitance at node A, excluding C_{boot1}. V_{diode} is the voltage drop across a single diode, similar to $D0$ in [9]. When V_{ddL} is sufficiently close to $2V_{diode}$, boot capacitor becomes considerably large. In [10], cross-coupled load is divided into half and only one boot capacitor is required, partially reducing the overall area requirement.

III. PROPOSED LEVEL SHIFTER

The proposed level-up, as illustrated in Fig. 2, is based on a traditional buffer with certain modifications to minimize short-circuit current, reduce delay while minimizing the overall number of transistors. Since an input signal at the V_{ddL} level cannot completely turn off PMOS transistors, an inverter is designed with two NMOS transistors (N1 and N2) where N2 is driven by inverted input signal. When input signal is at logic low, N1 is off and N2 is on. Node A is at $V_{ddH} - V_{th}$ since

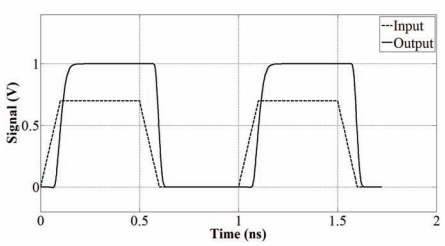


Fig. 3. **Input and output waveforms of the proposed level shifter.**

N2 cannot pass a full VDD. To compensate for the threshold voltage drop, two keeper PMOS transistors, P1 and P2, are added. When output node goes low, P2 is on. Since input signal is also at logic low, node A is pulled to VDDH. Note that P1 is added to prevent short-circuit current when node A is being discharged through N1. A pull down NMOS transistor, N5, is added to reduce the delay when the output is having a high-to-low transition. If the input signal is at logic high, N1 is on, N2 is off. Node A is discharged through N1. Since P1 is off, no short-circuit current exists. As node A is discharged, output rises to VDDH through P4. The input and output waveforms of the proposed level shifter are illustrated in Fig. 3 where the low voltage domain is 0.7 V and high voltage domain is 1 V. The signal switches at 1 GHz frequency with 100 ps transition time and level shifter drives an output capacitance of 5 fF in a 45 nm technology. The proposed level shifter can work with an input voltage domain as low as 0.45 V, as further described in the following section.

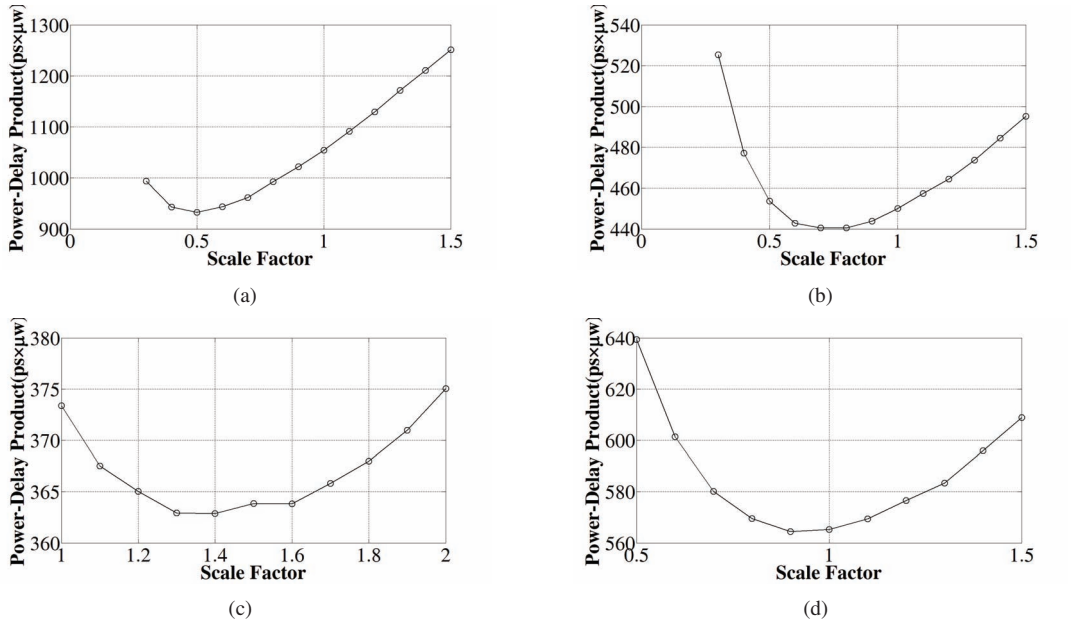


Fig. 4. **Power-delay product as a function of scale factor for each topology: (a) cross-coupled, (b) bootstrapped, (c) buffer, (d) proposed.**

IV. SIMULATION RESULTS

Extracted simulations of four level shifters are performed:

- Traditional buffer consisting of two inverters
- Conventional cross-coupled topology [Fig. 1(a)]
- Bootstrapping level shifter [Fig. 1(b)]
- Proposed level shifter (Fig. 2)

Note that each level shifter is designed at the physical level and extracted using a 45 nm technology. Extracted simulations are achieved at 1 GHz with 100 ps transition times while driving an output load of 5 fF capacitance. Low and high VDD levels are, respectively, 0.7 V and 1 V. Also note that the traditional buffer is included in the comparison only as a reference for delay and transient power. In practice, this topology is not suitable as a level shifter due to unreasonably high leakage and short circuit current, as mentioned before.

The extracted simulation results are presented in four parts: power-delay product for each level shifter is described in Section IV-A, worst-case corner simulation results for delay, dynamic power, and leakage power are provided in Section IV-B, the dependence of each topology on input swing is analyzed in Section IV-C, and finally, the physical area consumed by each circuit is discussed in Section IV-D.

A. Power-Delay Product

The power-delay product for each level shifter is obtained as a function of scale factor, as shown in Fig. 4. The scale factor is the sizing factor for those transistors that affect the delay of the circuit in each level shifter. As shown in this figure, upsizing the critical transistors initially enhances the power-delay product, eventually reaching a minimum value. However, if the transistors are upsized further, power-delay product starts to increase. Thus, by obtaining the power-delay product curves as a function of scale factor, each topology can be compared at the corresponding optimum design point where power-delay product is minimized. Note that when the scale factor is equal to 1, each topology exhibits approximately the same delay of 50 ps. According to Fig. 4, bootstrapping technique achieves the least power-delay product (excluding traditional buffer) that is 22% less than the proposed topology. However, bootstrapping technique has significant area overhead, as quantified in Section IV-D. As compared to the cross-coupled level shifter, the proposed topology exhibits approximately 66% less power-delay product, which is a significant improvement over the most commonly used level shifter topology in the literature.

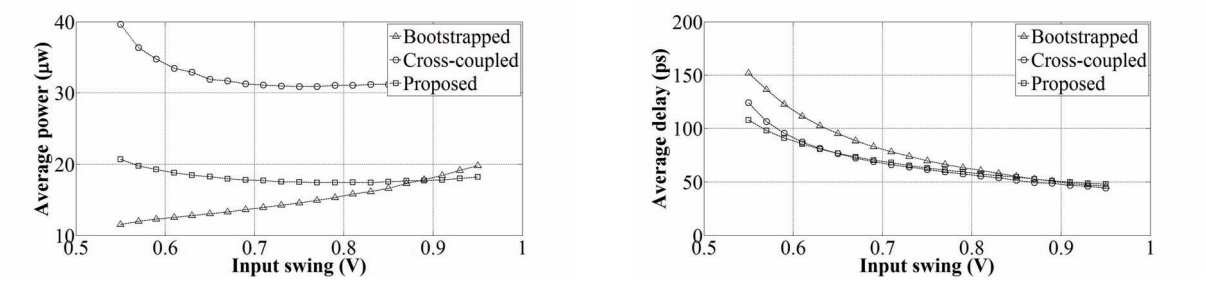
TABLE I
EXTRACTED RESULTS AT NOMINAL CORNER

Topology	Tran. power (μw)	Leakage (nw)	Delay (ps)	Slew (ps)
Cross-coupled	31.09	24.29	67.71	50.40
Bootstrapped	13.75	14.46	80.50	71.96
Buffer	8.43	850.62	56.29	50.13
Proposed	17.73	15.53	69.21	60.82

B. Nominal and Corner Simulation Results

Extracted simulation results at the nominal corner (typical models, 1 V supply and at 27°C) are listed in Table. I. The proposed level shifter achieves 43% reduction in transient power compared to cross-coupled topology while achieving almost the same delay. Leakage power is also reduced by 36%. As compared to bootstrapped topology, the proposed level shifter achieves 14% less delay, but 28% more transient power. Bootstrapped topology, however, has significant area overhead (see Section IV-D). Output slew of each topology is comparable with a noticeable increase for the bootstrapped topology.

All of the topologies are analyzed at the worst-case corner for delay (slow models, 0.9 V, and 165°C), transient power (fast models, 1.1 V, and -40°C), and leakage power (fast models, 1.1 V, and 165°C). The results are listed, respectively, in Tables II and III.



(a) (b)

Fig. 5. **Dependence on input supply voltage: (a) power as a function of input supply voltage, (b) delay as a function of input supply voltage.**

TABLE II
WORST CORNER FOR DELAY (SS MODEL, 0.9V SUPPLY AND 165°C) AND TRANSIENT POWER (FF MODEL, 1.1V SUPPLY AND -40°C)

Topology	Transient power (μw)	Average delay (ps)	Average slew (ps)
Worst corner for delay			
Cross-coupled	23.77	139.18	138.13
Bootstrapped	10.78	199.12	257.74
Buffer	6.10	128.85	126.11
Proposed	14.14	151.26	167.01
Worst corner for transient power			
Cross-coupled	40.88	44.24	31.06
Bootstrapped	17.15	47.24	34.90
Buffer	14.22	37.34	32.12
Proposed	22.73	42.85	35.69

TABLE III
WORST CORNER FOR LEAKAGE (FF MODEL, 1.1V SUPPLY AND 165°C)

Topology	Input @ V_{ddL} (nw)	Input @ gnd (nw)	Average (nw)
Cross-coupled	349.53	338.35	343.94
Bootstrapped	198.50	352.73	275.62
Buffer	4367.20	76.42	2221.81
Proposed	248.37	195.42	221.90

The proposed topology exhibits 24% less delay and 44% lower transient power at the worst corner as compared to bootstrapped and cross-coupled topologies, respectively. Furthermore, the proposed level shifter achieves approximately 20% and 36% less leakage power than, respectively, bootstrapped and cross-coupled topologies in the worst corner.

C. Dependence on Input Swing

The behavior of each topology to different levels of input voltage is investigated in this section. Transient power and delay are shown in Figs. 5(a) and 5(b) as a function of input swing (V_{ddL}). According to Fig. 5(a), bootstrapped topology achieves lower power for input voltage domains less than 0.88 V. Proposed topology achieves significantly less power than the cross-coupled topology, particularly at input voltage domains less than 0.65 V. According to Fig. 5(b), proposed topology outperforms both cross-coupled and bootstrapped topologies in delay as input swing is reduced.

D. Area Comparison

All of the topologies are laid out using a standard cell design methodology where the height is fixed at 1.25 μm. The physical area consumed by the cross-coupled, bootstrapped, and proposed topologies, are, respectively, 3.1 μm^2, 13.65 μm^2, and 2.8 μm^2. Proposed topology consumes 9.5% and 79.5% less area as compared to cross-coupled and bootstrapping topologies, respectively.

V. CONCLUSIONS

A novel dual supply level-up shifter is proposed for multi-voltage operation. The proposed topology achieves 43% less transient power and 36% less leakage power than the most commonly used cross-coupled topology, while also consuming 9.5% less area. As compared to bootstrapping technique, proposed topology achieves 79.5% reduction in physical area. Corner simulations are also performed, demonstrating the superior performance of the proposed level shifter.

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