Figures-of-Merit to Evaluate the Significance of Switching Noise in Analog Circuits

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***Abstract*— An analysis flow is proposed to determine the significance of induced (switching) noise in analog circuits. The proposed flow is exemplified through two commonly used amplifier topologies. Specifically, *input-referred switching noise* is introduced as the first figure-of-merit and compared with the well-known equivalent input device noise through analytic expressions. The comparison is achieved as a function of multiple parameters that characterize switching noise in the time domain (modeled as a decaying sine wave), such as peak amplitude, period, oscillation frequency within each period, and damping coefficient. The analytic expressions used to obtain input-referred switching and device noise are verified with SPICE simulations. These expressions are utilized to develop *dominance regions* for both noise sources. Furthermore, time-domain switching noise amplitude (at the bulk node) at which the input device and switching noise magnitude are equal (in the frequency domain) is determined as the second figure-of-merit, providing guidelines for the signal isolation process. Reverse body biasing is also proposed to alleviate the effect of switching noise by weakening the bulk-to-input transfer function as opposed to reducing the switching noise amplitude at the bulk nodes. It is demonstrated that this method has a negligible effect on primary design objectives of the victim circuit while reducing the input-referred switching noise by up to 10 dB. As a case study, the proposed flow is applied to a potentiostat circuitry where input sensitivity is of primary importance.**

***Index Terms*— Analog-digital integrated circuits, circuit noise, integrated circuit modeling.**

I. Introduction

IN MIXED-SIGNAL integrated circuits, substrate coupling noise has long been a critical issue due to dense and monolithic integration of analog/RF and digital components on the same die. Switching (also referred to as induced) noise caused by a transition of a digital signal propagates through the substrate and reaches an analog/RF circuit, degrading important performance specifications, such as signal-to-noise ratio, gain, and bandwidth, as shown in Fig. 1 [1]–[4].

Heterogeneous integration and faster transition times exacerbate the issue of switching noise in sensitive analog/RF blocks. In addition to induced noise, analog/RF circuits also suffer from intrinsic device noise, such as thermal [5], flicker [6], and shot noise [7]. Traditional analog design flows typically focus on intrinsic noise since extensive analysis and simulation methods exist [8], [9]. Alternatively, the analysis of switching noise and substrate coupling is challenging due to prohibitive computational complexity. Accurate estimation of the substrate noise at the bulk node of an analog/RF transistor requires a simultaneous consideration of the digital switching activity, power/ground networks, and the substrate network [10].

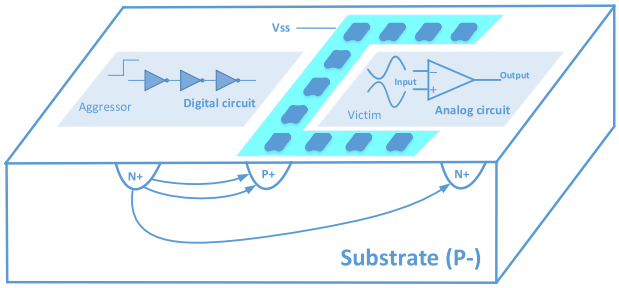

Fig. 1. Switching noise coupling from a digital block to a sensitive analog circuit in the presence of guard rings.

Significant effort has been made to characterize and efficiently analyze the substrate noise coupling. For example, in [11] and [12], the experimental circuits have been used to model substrate noise in a mixed-signal environment and several isolation strategies have been introduced. In [13], a simplified equivalent circuit has been developed to model switching noise and its effects on analog-to-digital converter and voltage-controlled oscillator. Specific logic gates have been used in [14] to model and detect switching noise in digital circuits. In [15], a voltage comparator has been designed as a noise detector to measure the equivalent substrate noise waveforms. The uniformity of the voltages on the ground distribution network is exploited in [16] to efficiently analyze the substrate noise coupling.

These research works primarily focus on the measurement and estimation of switching noise at the victim circuits. For analog design flows, it is also important to evaluate the significance of switching noise and understand the conditions under which switching noise starts to be dominant. This evaluation is important since conventional noise mitigation techniques (such as guard rings [17], deep n-well [18], slew/skew control [19], and power network optimization [20]) typically aim at reducing switching noise amplitude at the expense

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of area and power consumption. It is therefore critical to determine the required reduction in switching noise amplitude to minimize the overhead. The provided analytic expressions are utilized to determine the peak amplitude of switching noise (in the time domain) that makes the input-referred switching and device noise the same in the frequency domain. This criterion is used to evaluate the significance of switching noise.

The primary contributions of this paper are as follows.

1) *Input-referred switching noise* is introduced as a figure-of-merit to determine the significance of induced noise.
2) An analysis flow is proposed to analytically compare the input-referred switching noise with equivalent input device noise.
3) Dominance regions for both switching and device noise are identified as a function of time-domain switching noise characteristics, such as the peak amplitude, period, oscillation frequency within each period, and damping coefficient.
4) Time-domain peak amplitude that leads to equal input-referred switching and device noise in the frequency domain is characterized and used as the second figure-of-merit.
5) A method based on body biasing is introduced to reduce the effect of switching noise by weakening the transfer function from bulk node to input node of an analog circuit.
6) The proposed flow is applied to a sensitive potentiostat circuitry as a case study.

The rest of this paper is organized as follows. Proposed flow is described in Section II. The significance of switching noise is evaluated and dominance noise regions are identified in Section III. A method is proposed in Section IV to alleviate the effect of switching noise while maintaining the primary design objectives of the victim circuit. A case study is described in Section V, where the proposed flow and switching noise reduction technique are applied to a potentiostat circuitry that measures neurotransmitter concentrations. Finally, the conclusion is given in Section VI.

II. Proposed Analysis Flow

The proposed flow is summarized in Fig. 2. Time-domain switching noise profile at the bulk node of the transistors is modeled as a decaying sine wave. Existing techniques can also be utilized to estimate switching noise profile for a specific circuit. Corresponding transfer functions are used to transfer switching noise from the bulk node to the input node of the circuit. This noise is referred to as input-referred switching noise and used as a primary figure-of-merit to determine the significance of switching noise. By comparing the input-referred switching noise with the equivalent input device noise, dominant noise source in the frequency range of interest is determined. Note that the noise analysis at the input eliminates the effect of gain, providing a more fair comparison framework. Once the dominant noise is determined, applicable noise reduction techniques can be applied. Furthermore, time-domain switching noise amplitude (at the bulk node) that leads to equal switching and device noise at the input node (in the frequency domain) is characterized, and used as a guideline while applying switching noise reduction techniques.

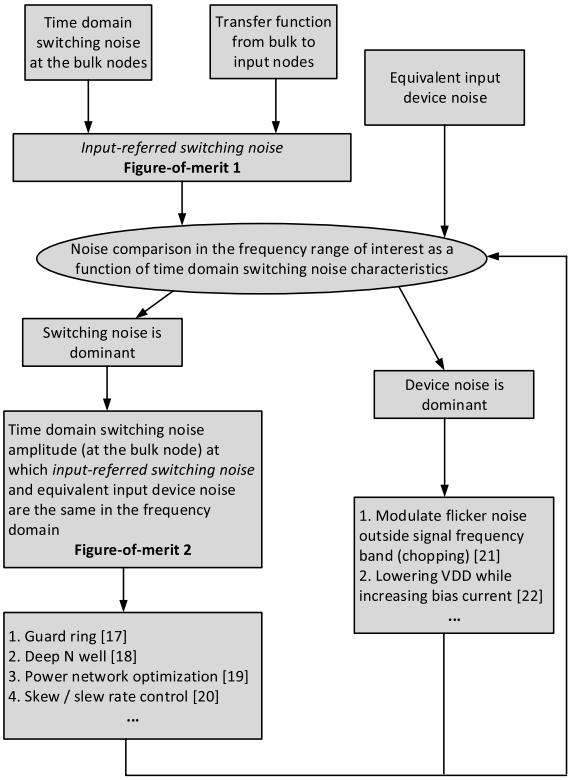

Fig. 2. Proposed flow and the concept of *input-referred switching noise* to determine the significance of induced noise in analog circuits.

Two commonly used amplifier topologies, two-stage common source with a differential input pair and folded cascode, are chosen as analog victim circuits to illustrate the proposed flow. Both amplifiers are designed in a 0.5-μm CMOS technology with a power supply voltage of 3 V. All the simulations are achieved with Spectre using AMI device models [23]. Brief background information on these amplifier topologies is provided in Section II-A. The model used to represent switching noise generated by digital blocks is described in Section II-B. Input-referred switching noise and equivalent input device noise are quantified in, respectively, Sections II-C and II-D.

A. Background on Amplifier Topologies

Two-stage common source with a differential input pair [Fig. 3] and a folded cascode amplifier [Fig. 4], are used as analog victim circuits. Both topologies utilize a current mirror to obtain a single output. Some related specifications of these two amplifiers and the operating points are listed in Table I. Note that the DC gain and phase margin of both amplifiers are comparable.

Each transistor within the amplifiers suffers from both thermal and flicker noise. The resistance R_C between the first and second stage in the two-stage amplifier is used to adjust the location of the pole/zero for frequency compensation.

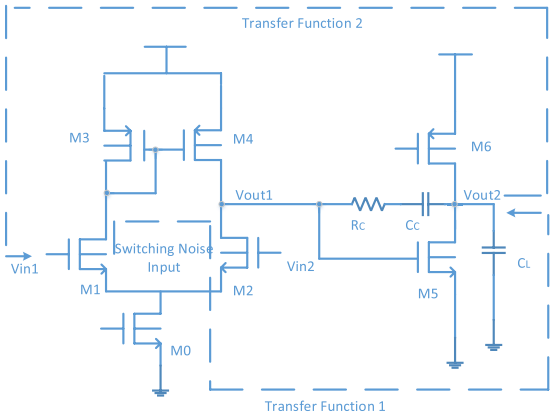

Fig. 3. Schematic of a two-stage amplifier used to evaluate the significance of switching noise.

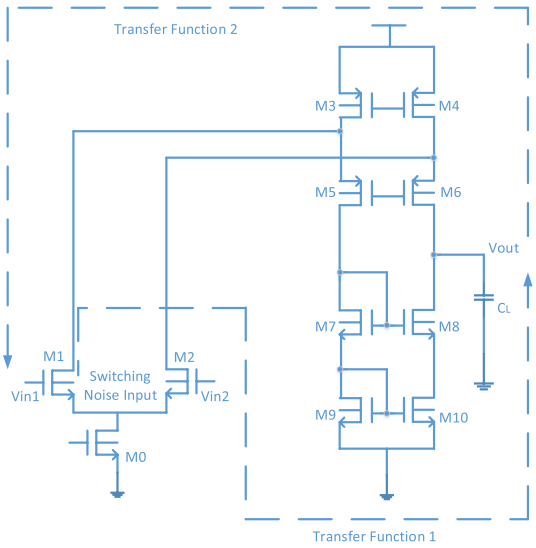

Fig. 4. Schematic of a folded cascode amplifier used to evaluate the significance of switching noise.

TABLE I

AMPLIFIER SPECIFICATIONS AND OPERATING POINTS

	Two-stage	Folded cascode
DC gain	72 dB	75 dB
Phase margin	56°	60°
Location of dominant pole	17.62 kHz	10.83 kHz
Flicker and thermal noise at 1 Hz	-114 dB	-104.5 dB
Input bias voltage	1.6 V	1.5 V
Load capacitance	1 pF	1 pF

In addition to device noise, the transistors suffer from switching noise that is generated by the digital circuitry and propagates to the bulk nodes through the substrate.

B. Switching Noise Modeling at the Bulk Node

A periodic decaying sine wave is used to represent the switching noise generated by the digital circuit. Decaying sine wave is an appropriate function for switching noise, as shown in [11], [24], and [25]. Peak amplitude, oscillation frequency, period of the decaying sine wave, and damping coefficient are the primary parameters of the decaying sine wave and are used

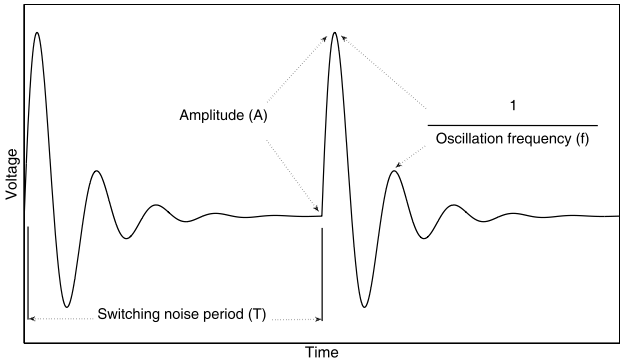

Fig. 5. Characteristics of decaying sine wave used to model time-domain switching noise at the bulk node of a transistor.

to model noise characteristics. These parameters are shown in Fig. 5. Since dominant noise identification is achieved in the frequency domain, Laplace transform is used. The decaying sine wave time- and frequency-domain expressions are

$$\begin{aligned} V_{\text{swi}}(t) = {} & Ae^{-(\alpha t)}\sin(\omega t)u(t)u(T-t) \\ & + Ae^{-(\alpha(t-T))}\sin(\omega(t-T))u(t-T)u(2T-t) \\ & + \cdots + Ae^{-(\alpha(t-(n-1)T))}\sin(\omega(t-(n-1)T)) \\ & \times u(t-(n-1)T)u(nT-t) \end{aligned} \tag{1}$$

$$\begin{aligned} V_{\text{swi}}(s) = {} & \frac{1}{(1-e^{-Ts})} \times A \\ & \times \frac{e^{-(s+\alpha)T} \times (-(s+\alpha)\sin\omega T - \omega\cos\omega T) + \omega}{\omega^2 + (s+\alpha)^2} \end{aligned} \tag{2}$$

where A is the peak amplitude, T is the period of the decaying sine wave, α is the damping coefficient to determine how fast the sine wave decays, ω is the oscillation frequency within a period, which is $2\pi f$, and $u(t)$ is the unit function.

A greater damping coefficient α results in reduced settling time (faster damping), thereby producing smaller noise magnitudes in the frequency domain, particularly at low frequencies. Similarly, noise magnitude in the frequency domain is linearly proportional to the peak amplitude A in the time domain, as indicated by (2). For example, decreasing the peak amplitude from 80 to 30 mV reduces the switching noise by approximately 9 dB over the entire frequency range. Higher oscillation frequency ω in time domain corresponds to a smaller settling time. In the frequency domain, switching noise with a larger ω has a smaller amplitude at low frequencies. For example, if oscillation frequency is increased from 5 to 10 MHz in time domain, the frequency domain magnitude decreases by approximately 7 dB at DC. Finally, an increase in the period T of the switching noise in time domain shifts the fundamental frequency and reduces the noise magnitude in the frequency domain, particularly at low frequencies. For example, if the period increases from 1 to 10 μs, noise magnitude in the frequency domain is reduced by approximately 20 dB at DC. These four parameters are utilized to model different switching noise characteristics.

C. Quantification of Input-Referred Switching Noise

Switching noise generated by a digital circuit couples to the substrate and reaches the bulk node of nMOS transistors in analog blocks. Note that switching noise observed at the pMOS transistors is typically lower due to the capacitive isolation of n-well and is therefore ignored in this analysis [4].

Transfer functions are obtained to transmit each noise source from the bulk node of a transistor to the input node of the amplifiers, as shown by the dashed lines in Figs. 3 and 4. The overall input-referred switching noise is determined by the superposition of these noise sources and used as a primary figure-of-merit to evaluate the significance of switching noise.

Noise sources at the bulk nodes are first transferred to the output of the amplifiers through the transfer function $V_{\text{out}}/V_{\text{bulk}}$. This noise at the output is then transferred to the input of an amplifier through the transfer function $V_{\text{out}}/V_{\text{in}}$, which represents the gain of the amplifier. Thus, switching noise at the bulk node of the nMOS transistors is transferred to the input node of the amplifier by utilizing these two transfer functions

$$V_{\text{in}}^{\text{swi}} = \frac{V_{\text{out}}/V_{\text{bulk}}}{V_{\text{out}}/V_{\text{in}}} \times V_{\text{swi}} = \frac{V_{\text{in}}}{V_{\text{bulk}}} \times V_{\text{swi}} \tag{3}$$

where $V_{\text{in}}^{\text{swi}}$ is the input-referred switching noise, V_{out} is the amplifier output voltage, V_{bulk} is the voltage at the bulk node of an nMOS transistor, V_{in} is the amplifier input voltage, and V_{swi} is the switching noise at the bulk node.

In the two-stage amplifier [Fig. 3], the ratio of these two transfer functions for each nMOS transistor in the second stage is approximately 50 times weaker as compared with the input nMOS transistors due to the gain of the first stage. Thus, for the two-stage amplifier, switching noise is critical primarily for the two input transistors (M_1 and M_2), as also verified by SPICE analysis. Hence, switching noise is applied only to the bulk nodes of M_1 and M_2. The ratio of the transfer functions for the two-stage amplifier is determined by

$$\frac{V_{\text{in}}}{V_{\text{bulk}}} = \frac{V_{\text{out2}}/V_{\text{bulk}}}{V_{\text{out2}}/V_{\text{in}}} = \frac{V_{\text{out1}}/V_{\text{bulk}}}{V_{\text{out1}}/V_{\text{in}}} \tag{4}$$

since the gain of the second stage ($V_{\text{out2}}/V_{\text{out1}}$) is canceled. The DC transfer function $V_{\text{out1}}/V_{\text{bulk}}$ is given by

$$\begin{aligned}\left.\frac{V_{\text{out1}}}{V_{\text{bulk}}}\right|_{\text{2stg}} &= \frac{g_{\text{mb1}}(g_{m2}+g_{\text{mb2}})}{g_{m1}+g_{\text{mb1}}} \times (r_{o2} \parallel r_{o4}) \\ &= g_{\text{mb1}} \times (r_{o2} \parallel r_{o4}) \end{aligned} \tag{5}$$

where g_m and g_{mb} are, respectively, the transconductance of the gate and bulk nodes of a transistor, and r_o is the channel resistance. DC transfer function $V_{\text{out1}}/V_{\text{in}}$ is calculated in a similar fashion

$$\left.\frac{V_{\text{out1}}}{V_{\text{in}}}\right|_{\text{2stg}} = g_{m1} \times (r_{o2} \parallel r_{o4}). \tag{6}$$

By dividing (5) by (6), the DC transfer function $V_{\text{in}}/V_{\text{bulk}}$ for each input transistor of the two-stage amplifier is

$$\text{DCTF}|_{\text{2stg}} = \frac{\left.\frac{V_{\text{out1}}}{V_{\text{bulk}}}\right|_{\text{2stg}}}{\left.\frac{V_{\text{out1}}}{V_{\text{in}}}\right|_{\text{2stg}}} = \frac{g_{\text{mb1}}}{g_{m1}}. \tag{7}$$

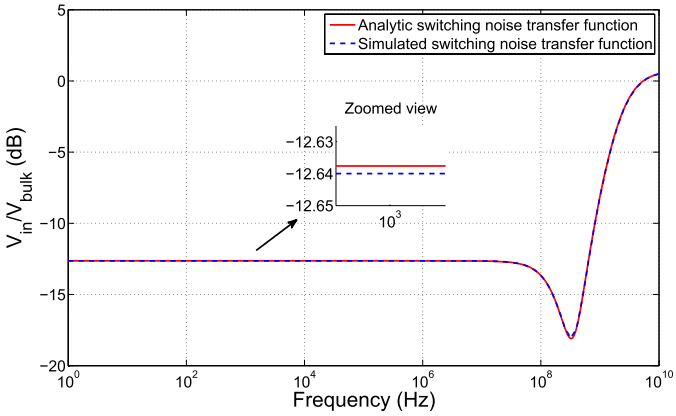

Fig. 6. Comparison of analytic and simulated transfer function $V_{\text{in}}/V_{\text{bulk}}$ used to transmit switching noise from bulk node to the input node in the two-stage amplifier.

Note that since the two input transistors are sized the same, $g_{m1} = g_{m2}$.

A similar procedure is followed for the folded cascode amplifier, yielding the following:

$$\begin{aligned}\left.\frac{V_{\text{out}}}{V_{\text{bulk}}}\right|_{\text{FC}} &= g_{\text{mb1}}\{[(g_{m3}+g_{\text{mb3}})r_{o3}(r_{o1} \parallel r_{o5})] \\ &\quad \parallel [(g_{m7}+g_{\text{mb7}})r_{o7}r_{o9}]\} \end{aligned} \tag{8}$$

$$\begin{aligned}\left.\frac{V_{\text{out}}}{V_{\text{in}}}\right|_{\text{FC}} &= g_{m1}\{[(g_{m3}+g_{\text{mb3}})r_{o3}(r_{o1} \parallel r_{o5})] \\ &\quad \parallel [(g_{m7}+g_{\text{mb7}})r_{o7}r_{o9}]\}. \end{aligned} \tag{9}$$

Thus, the DC transfer function $V_{\text{in}}/V_{\text{bulk}}$ for each input transistor of the folded cascode amplifier is determined by dividing (8) by (9)

$$\text{DCTF}|_{\text{FC}} = \frac{\left.\frac{V_{\text{out}}}{V_{\text{bulk}}}\right|_{\text{FC}}}{\left.\frac{V_{\text{out}}}{V_{\text{in}}}\right|_{\text{FC}}} = \frac{g_{\text{mb1}}}{g_{m1}}. \tag{10}$$

The final transfer function from the bulk node of the input transistor to the input node is

$$\frac{V_{\text{in}}}{V_{\text{bulk}}} = \text{DCTF} \times \frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)\cdots\left(1+\frac{s}{\omega_{zn}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\cdots\left(1+\frac{s}{\omega_{pn}}\right)} \tag{11}$$

where ω_{z1}^m to ω_{zn}^m and ω_{p1}^m to ω_{pn}^m are, respectively, the magnitude of zeros and poles.

Expression (11) is used to transmit the switching noise from the bulk node to the input node for both two-stage and folded cascode amplifiers. These transfer functions are shown in Figs. 6 and 7 for both amplifiers.

According to these figures, the analytic expressions match SPICE simulations. Finally, the overall input-referred switching noise $V_{\text{in}}^{\text{swi}}$ due to two input transistors is determined by

$$V_{\text{in}}^{\text{swi}} = 2 \times \frac{V_{\text{in}}}{V_{\text{bulk}}} \times V_{\text{swi}}. \tag{12}$$

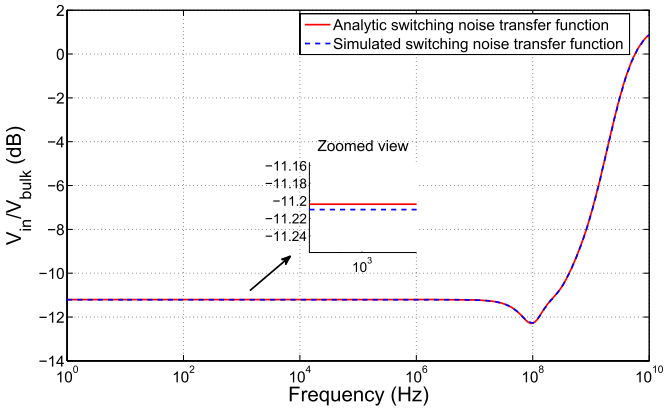

Fig. 7. Comparison of analytic and simulated transfer function $V_{\text{in}}/V_{\text{bulk}}$ used to transmit switching noise from bulk node to the input node in the folded cascode amplifier.

D. Quantification of Equivalent Input Device Noise

As mentioned previously, flicker and thermal noise are considered to determine the inherent noise. The overall device noise at the input node is the superposition of each noise source. For the two-stage amplifier, even though the device noise in the first stage affects the overall noise significantly more than the second stage (since the noise in the second stage is divided by the gain of the first stage to reach amplifier input), transistors M_1–M_6 are included in the analysis.

The DC flicker noise V^2_{flicker} and thermal noise V^2_{thermal} of the two-stage amplifier at the input node are

$$V^2_{\text{flicker}}\Big|_{2\text{stg}} = \frac{2K_N}{C_{\text{ox}}WL_{M1}f} + \frac{2K_P g^2_{m3}}{g^2_{m1}C_{\text{ox}}WL_{M3}f} + \frac{\frac{K_N}{C_{\text{ox}}WL_{M5}f} + \frac{K_P g^2_{m6}}{g^2_{m5}C_{\text{ox}}WL_{M6}f}}{g^2_{m1}(r_{o1} \parallel r_{o3})^2} \tag{13}$$

$$V^2_{\text{thermal}}\Big|_{2\text{stg}} = \frac{8kT\gamma}{g_{m1}} + \frac{8kT\gamma\, g_{m3}}{g^2_{m1}} + \frac{4kT\gamma}{g^2_{m1}g_{m5}(r_{o1} \parallel r_{o3})^2} + \frac{4kT\gamma\, g_{m6}}{g^2_{m1}g^2_{m5}(r_{o1} \parallel r_{o3})^2} \tag{14}$$

where k is Boltzmann's constant, T is the temperature in Kelvin, γ is the thermal noise coefficient, K_N and K_P are the process-dependent constants for, respectively, nMOS and pMOS transistors, C_{ox} is the gate oxide capacitance per unit area, W and L are, respectively, the width and length of a transistor. Thus, the overall DC device noise for the two-stage amplifier is

$$V^{\text{dev}}_{\text{in,DC}}\big|_{2\text{stg}} = \sqrt{V^2_{\text{flicker}}\big|_{2\text{stg}} + V^2_{\text{thermal}}\big|_{2\text{stg}}}. \tag{15}$$

For the folded cascode amplifier, the device noise analysis is achieved as follows. The thermal and flicker noise of each transistor are modeled by an ac current source I_s between the source and drain terminals of each transistor (M_1–M_{10}). This current source is transmitted to the input node by utilizing the transfer function V_{in}/I_s. Thus, the DC device noise at the input node is

$$V^{\text{dev}}_{\text{in,DC}}\Big|_{\text{FC}} = \sqrt{\left(\frac{V_{\text{out}}/I_{s1}}{V_{\text{out}}/V_{\text{in}}}\right)^2 \times I^2_{s1} + \cdots + \left(\frac{V_{\text{out}}/I_{s10}}{V_{\text{out}}/V_{\text{in}}}\right)^2 \times I^2_{s10}} \tag{16}$$

where I_s is

$$I^2_s = 4kT\gamma\, g_m + \frac{K_{N/P}}{C_{\text{ox}}WLf}g^2_m. \tag{17}$$

The DC gain $V_{\text{out}}/V_{\text{in}}$ is equal to (9). V_{out}/I_s, however, varies for each transistor M, as provided in the following:

$$\frac{V_{\text{out}}}{I_s}\Big|_{M3,4} = \frac{ab - r_{o5}b}{a+b} \tag{18}$$

$$\frac{V_{\text{out}}}{I_s}\Big|_{M5,6} = \frac{br_{o5}}{a+b} \tag{19}$$

$$\frac{V_{\text{out}}}{I_s}\Big|_{M7,8} = \frac{ar_{o7}}{-a-b} \tag{20}$$

$$\frac{V_{\text{out}}}{I_s}\Big|_{M9,10} = \frac{-ab + ar_{o7}}{a+b} \tag{21}$$

where

$$a = r_{o5} + (r_{o1} \parallel r_{o3}) + g_{m5}r_{o5}(r_{o1} \parallel r_{o3}) \tag{22}$$

$$b = r_{o7} + r_{o9} + g_{m7}r_{o7}r_{o9}. \tag{23}$$

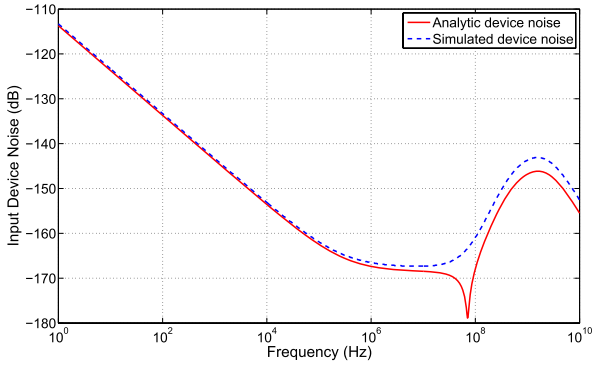

Fig. 8. Comparison of analytic and simulated equivalent input device noise for the two-stage amplifier.

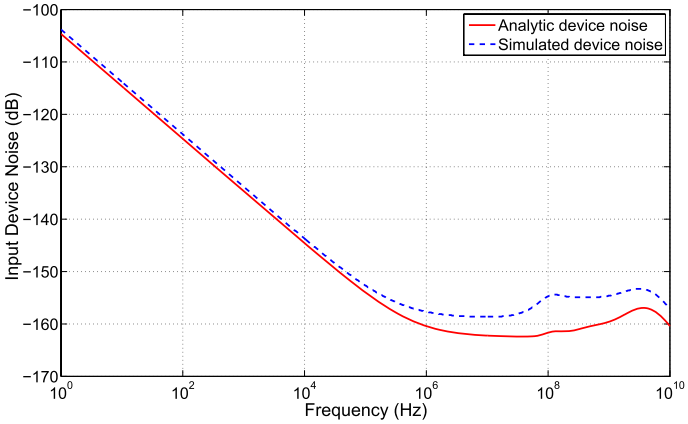

Fig. 9. Comparison of analytic and simulated equivalent input device noise for the folded cascode amplifier.

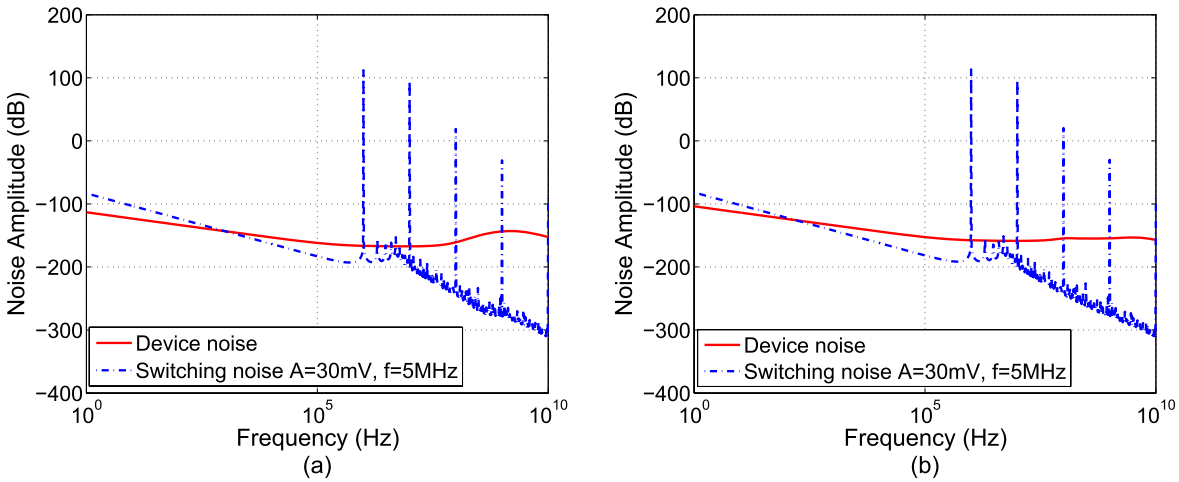

Fig. 10. Comparison of input-referred switching noise and equivalent input device noise. (a) Two-stage amplifier. (b) Folded cascode amplifier.

The overall equivalent input device noise (including both thermal and flicker) for both amplifiers is determined by

$$V_{\text{in}}^{\text{dev}} = V_{\text{in,DC}}^{\text{dev}} \times \frac{\left(1+\frac{s}{\omega_{z1}^{m}}\right)\left(1+\frac{s}{\omega_{z2}^{m}}\right)\cdots\left(1+\frac{s}{\omega_{zn}^{m}}\right)}{\left(1+\frac{s}{\omega_{p1}^{m}}\right)\left(1+\frac{s}{\omega_{p2}^{m}}\right)\cdots\left(1+\frac{s}{\omega_{pn}^{m}}\right)} \quad (24)$$

where ω_{z1}^{m} to ω_{zn}^{m} and ω_{p1}^{m} to ω_{pn}^{m} are, respectively, the magnitude of zeros and poles. Note that the location of poles and zeros are different for each transistor m.

Equivalent input device noise for the two-stage amplifier is shown in Fig. 8. Noise exhibits an approximately linear decrease at low frequencies due to flicker noise. The device noise becomes constant at approximately 1 MHz due to the dominance of thermal noise. Since the DC gain decreases at higher frequencies, equivalent input device noise slightly increases after 10 MHz. Similarly, equivalent input device noise for the folded cascode amplifier is shown in Fig. 9. For both amplifiers, analytic expressions reasonably approximate SPICE simulations.

III. Identification of Dominance Regions

Input-referred device and switching noise are compared to identify dominant noise source as a function of multiple parameters. Equations (12) and (24) are utilized to determine the dominance regions. As an example, these noise sources are plotted as a function of frequency in Fig. 10 for both amplifiers. Solid line represents equivalent input device noise. Dotted-dashed line is the input-referred switching noise when the time domain characteristics are as follows: 1) peak amplitude A is 30 mV (1% of V_{DD}); 2) period T is 1 μs; 3) oscillation frequency f within each period is 5 MHz; and 4) damping coefficient α is 4×10^6. Note that the peak amplitude of 30 mV is comparable with the measured substrate noise in [12] and [26]. Specifically, the time-domain noise amplitude in [26] is approximately 3% of V_{DD}. For a V_{DD} of 3 V, peak-to-peak substrate noise of up to 190 mV has been reported [26].

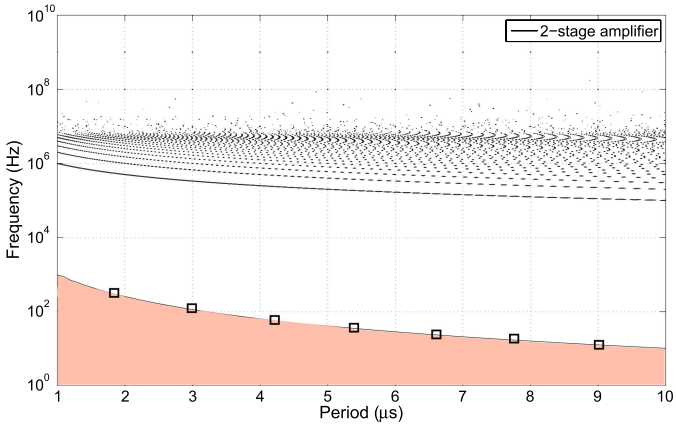

Fig. 11. Noise dominance regions for the two-stage amplifier. The black lines and dots represent the operating points where equivalent input device noise and input-referred switching noise are equal. Switching noise is dominant in the shaded region, whereas the blank region represents the operating points where device noise is dominant.

According to Fig. 10, switching noise is dominant at low frequencies despite high flicker noise. Specifically, in the two-stage amplifier, switching noise is dominant over device noise until approximately 1 kHz. For the folded cascode amplifier, the crossover frequency is 158 Hz. Also note that at DC, input-referred switching noise is 30 and 22 dB higher than the equivalent input device noise in, respectively, two-stage and folded cascode amplifier. Both noise sources decrease with increasing frequency, but switching noise decreases with a faster pace. Thus, device noise starts to be dominant after the crossover point except the fundamental and harmonic frequencies that are determined by the period of the switching noise (modeled as a decaying sine wave) in time domain. Note that the dominant noise analysis shown in Fig. 10 is not affected by temperature variations, since flicker noise dominates thermal noise at low frequencies. Alternatively, at high frequencies, device noise proportionally increases with temperature due to thermal noise. This increase (approximately 5 dB at 10 MHz when temperature rises from 27 °C to 165 °C), however, is negligible since the overall noise is sufficiently low.

TABLE II
TIME-DOMAIN SWITCHING NOISE AMPLITUDE (IN MILLIVOLTS) AT WHICH INPUT-REFERRED SWITCHING AND INPUT-REFERRED DEVICE NOISE ARE EQUAL IN THE FREQUENCY DOMAIN

	Period = 1 μs				Period = 5 μs				Period = 10 μs			
	Two-stg	FC	Two-stg BB	FC BB	Two-stg	FC	Two-stg BB	FC BB	Two-stg	FC	Two-stg BB	FC BB
1Hz	0.9	2.4	1.3	3.4	4.7	11.7	6.5	16.9	9.3	23.4	13	33.7
100Hz	9.5	23.8	13.3	34.3	46.6	117	65.2	168.6	93.1	234	130.4	337.2
1kHz	30	75.5	42.1	108.8	147.5	370.5	206.5	534	294.9	740.9	413	1067.8
10kHz	96.5	242	135.1	348.8	472	1245.7	660.7	1705.4	932.4	2337.5	1305.1	3368.7
100kHz	344.3	846.8	479.3	1221.8	1097.8	2699.8	1528. 2	3895.4	Negligible			

A. Effect of Time-Domain Switching Noise Period

To better investigate the effect of the switching noise period, frequency-domain dominance region is shown in Fig. 11 for the two-stage amplifier. The y-axis represents the frequency, while the switching noise period varies from 1 to 10 μs (x-axis). The remaining parameters of the decaying sine wave are maintained constant at $A = 30$ mV, $\alpha = 4 \times 10^6$, and $f = 5$ MHz. The black line with square markers and dotted black lines represent the operating points where equivalent input device noise and input-referred switching noise are equal. Switching noise is dominant in the shaded region, whereas the blank region represents the operating points where device noise is dominant. As the period of the switching noise increases in the time domain, the dominance region of the switching noise is reduced. Note that at constant period, switching and device noise become equal at multiple frequencies, as indicated by the black line with square markers and the black dots at higher frequencies. These crossover points can also be observed in Fig. 10 at a constant period of 1 μs. In the immediate vicinity of the black dots, switching noise dominates due to fundamental and harmonic frequencies. Thus, if the amplifier bandwidth of interest coincides with these points, switching noise significantly affects circuit operation. Alternatively, in the blank region, emphasis should be placed on reducing device noise. Note that a similar noise dominance region is also obtained for the folded cascode amplifier, exhibiting similar characteristics. The switching noise dominance region is slightly smaller for the folded cascode amplifier due to greater device noise, as can be observed in Fig. 10.

B. Effect of Time-Domain Switching Noise Amplitude

The noise dominance region shown in Fig. 11 is obtained at a constant switching noise amplitude ($A = 30$ mV) in the time domain. Existing switching noise mitigation techniques typically aim at reducing this amplitude. It is, however, difficult to determine an acceptable level of switching noise since no reliable figures-of-merit exist. Thus, (12) and (24) are utilized to numerically solve for the peak amplitude A of switching noise (in the time domain) that makes the input-referred switching noise and equivalent input device noise the same in the frequency domain. This computation is performed as a function of frequency and period of the switching noise. Results for the two-stage amplifier are shown in Fig. 12. The z-axis represents the switching noise amplitude in the time domain at which input-referred switching and device noise

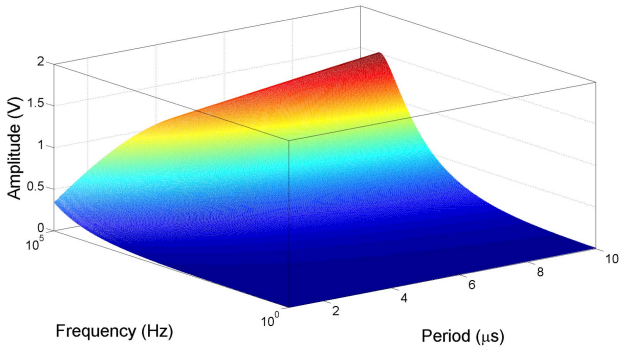

Fig. 12. Time-domain amplitude of switching noise at which input-referred device and input-referred switching noise (in the frequency domain) are equal (for two-stage amplifier).

are equal in the frequency domain. The remaining parameters of the switching noise (decaying sine wave) are constant at $\alpha = 4 \times 10^6$ and $f = 5$ MHz.

At constant period, A increases with frequency since input-referred switching noise is reduced as frequency increases (except the fundamental and harmonic frequencies). Some specific amplitude values are listed in Table II for both amplifiers. For example, when the period of the switching noise is 1 μs, at 100 Hz, the peak switching noise amplitude in the two-stage amplifier should be 9.5 mV to satisfy the equal input-referred switching and device noise. This value increases to 23.8 mV for the folded cascode amplifier. Note that if the period of the switching noise is equal to 10 μs, the fundamental frequency is 100 kHz. At this frequency, the switching noise amplitude that produces equal input-referred switching and device noise is sufficiently small since the effect of switching noise is highly strong at the fundamental frequency. This figure-of-merit provides a guideline on the acceptable level of switching noise, assuming that the time-domain characteristics of the switching noise (at the bulk node) are known. Last two columns for each period in Table II represent the effect of body biasing on dominant noise analysis and this figure-of-merit, as described in the following section.

IV. REVERSE BODY BIASING TO ALLEVIATE SWITCHING NOISE

As mentioned previously, existing noise mitigation techniques (such as guard rings, deep n-well, power network optimization, and skew/slew rate control) typically focus on reducing the peak noise amplitude. In this paper, an alternative approach is described where the magnitude of the transfer

TABLE III
EFFECT OF REVERSE BODY BIASING ON PRIMARY DESIGN OBJECTIVES FOR BOTH AMPLIFIERS

Two-stage common source amplifier								
V_B (V)	I_D (μA)	DC gain (dB)	g_{mb}/g_m	V_{GS} (V)	V_{th} (V)	Output swing (V)	Phase margin	Bandwidth (kHz)
0	89.58	72.3	0.23	941.6 m	807.6 m	1.71	56.1°	17.62
-0.8	87.73	73.4	0.17	1.072	941.1 m	1.70	56.4°	15.48
-1	87.23	73.2	0.15	1.099	969 m	1.70	56.5°	15.80
-2	84.23	68.6	0.11	1.213	1.085	1.68	56.4°	25.39
-3	79.75	59.1	0.08	1.298	1.172	1.66	56.3°	63.16
Folded cascode amplifier								
V_B (V)	I_D (μA)	DC gain (dB)	g_{mb}/g_m	V_{GS} (V)	V_{th} (V)	Output swing (V)	Phase margin	Bandwidth (kHz)
0	54.84	75.2	0.28	1.024	773.9 m	1.56	44.85°	11.87
-0.65	51.66	73.8	0.20	1.139	898.9 m	1.53	48.09°	13.83
-1	49.1	72.5	0.17	1.189	954.3 m	1.51	50.38°	15.80
-2	39.18	68.0	0.12	1.295	1.082	1.44	57.95°	24.51
-3	28.52	62.8	0.09	1.367	1.178	1.39	64.87°	37.78

function from a bulk node (where switching noise is present) to the input node of a victim circuit is reduced, thereby reducing input-referred switching noise even though the switching noise at the bulk node remains the same. Note that in low-voltage operational transconductance amplifiers, bulk node has been properly biased and utilized as the input node since threshold voltage has not scaled proportionally with the power supply voltage [27], [28]. Alternatively, in this paper, bulk node is reverse biased to reduce noise coupling from bulk node to the input node, as described in this section. Also note that the device noise is relatively insensitive to reverse body biasing, as shown in [29].

In (7) and (10), decreasing $g_{\rm mb}$ while maintaining g_m constant reduces the magnitude of the transfer function $V_{\rm in}/V_{\rm bulk}$, thereby alleviating the effect of switching noise at the input of the two-stage and folded cascode amplifiers.

According to the following expression, bulk transconductance $g_{\rm mb}$ of the input nMOS transistors can be decreased by applying reverse body bias to these transistors [30]

$$g_{\rm mb} = g_m \frac{\gamma}{2\sqrt{2\varphi + V_{\rm SB}}} \tag{25}$$

where γ is the body effect coefficient and φ is the surface potential. When body bias decreases, the threshold voltage increases, the current that flows through input nMOS transistors also decreases due to a higher threshold voltage. Less current causes the source voltage of transistors M_1 and M_2 to decrease. However, the change in the source voltage is relatively smaller as compared with the body bias. Thus, $V_{\rm SB}$ increases and $g_{\rm mb}$ decreases. Since both $V_{\rm GS}$ and threshold voltages increase simultaneously, the g_m of the input nMOS transistor remains approximately constant, which is highly important to maintain the primary design objectives of the amplifiers.

The effect of reverse body bias on g_m and $g_{\rm mb}$ is shown in Fig. 13 for the two-stage common source amplifier. As the body bias changes from 0 to -3 V (up to $-V_{\rm DD}$), g_m changes only from 1.73 to 1.601 mA/V (7.5% reduction), whereas $g_{\rm mb}$ decreases from 403.8 to 135.8 μA/V (more than 66% reduction). Thus, as shown in Fig. 13(b), the ratio $g_{\rm mb}/g_m$ significantly decreases as the body bias changes from 0 to -3 V, thereby weakening the bulk-to-input transfer function and reducing input-referred switching noise.

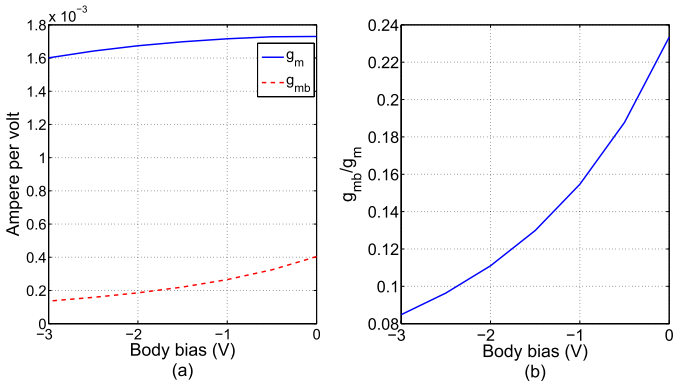

Fig. 13. Effect of reverse body bias on (a) transconductance and bulk transconductance and (b) ratio of bulk transconductance to transconductance for the two-stage common source amplifier.

The effect of reverse body biasing on primary design objectives is listed in Table III for both two-stage common source and folded cascode amplifiers. DC gain, output swing, phase margin, and bandwidth remain approximately the same until a body bias of -1 V. Note that the increase in the threshold voltage is compensated by an increase in the gate-to-source voltage (due to a reduction in the drain current). Also note that when applying reverse body bias, it is important to ensure that the input transistors remain in the saturation region.

As an example, body bias voltages of -0.8 and -0.65 V (both smaller than -1 V) are applied to the bulk nodes of the input transistors in, respectively, two-stage and folded cascode amplifiers. With these body voltages, the peak switching noise amplitude (in time domain) at the bulk node that leads to equal input-referred switching and device noise magnitude (in frequency domain), i.e., the second figure-of-merit, is characterized, as shown in Fig. 14 for the two-stage amplifier. Some specific values are listed in Table II. According to the figure and the table, the peak switching noise amplitude that satisfies equal noise at the input increases with body biasing. For example, when the period of the switching noise is 1 μs, at 1 kHz, the peak amplitude increases from 30 to 42.1 mV for a two-stage amplifier, indicating that approximately 40% more switching noise can be tolerated. For a folded cascode amplifier, the peak amplitude increases from 75.5 to 108.8 mV, thereby tolerating 44% higher switching noise at the bulk node. Note that based on the simulation results, device noise is nearly

TABLE IV
EFFECT OF TEMPERATURE ON THE PROPOSED REVERSE BODY BIASING TECHNIQUE TO REDUCE INPUT-REFERRED SWITCHING NOISE

V_B (V)	Temperature (°C)	Two-stage CS amplifier			Folded cascode amplifier		
		g_{mb}	g_m	g_{mb}/g_m	g_{mb}	g_m	g_{mb}/g_m
0	-40	657.5μ	2.745m	0.24	199.2μ	711.4μ	0.28
	27	403.8μ	1.73m	0.23	140.1μ	508.9μ	0.28
	165	178.1μ	806.1μ	0.22	74.72μ	281.9μ	0.27
-1	-40	437.8μ	2.737m	0.16	121.7μ	694.4μ	0.18
	27	265.3μ	1.716m	0.15	83.38μ	489.1μ	0.17
	165	114.4μ	798.2μ	0.14	42.59μ	265.4μ	0.16
-3	-40	230μ	2.565m	0.09	54.18μ	561.8μ	0.1
	27	135.8μ	1.601m	0.08	35.18μ	382.9μ	0.09
	165	56.08μ	752μ	0.07	16.89μ	204.9μ	0.08

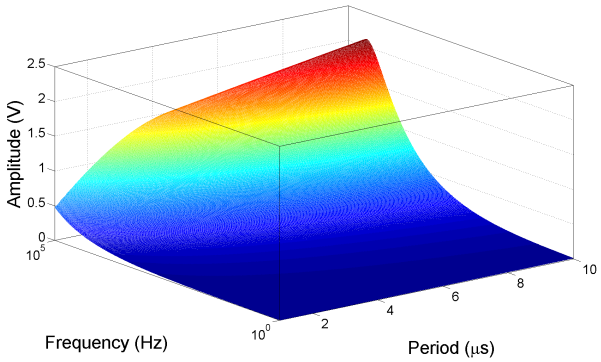

Fig. 14. Effect of body biasing on the time-domain amplitude of switching noise that leads to equal input-referred device and switching noise (for two-stage amplifier).

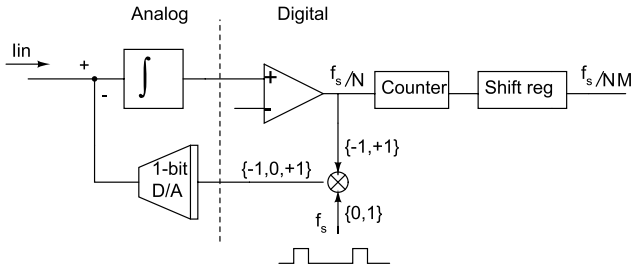

Fig. 15. System level diagram of a single channel of the potentiostat.

independent of the reverse body bias. This characteristic is also described in [29], as mentioned earlier in this section.

Another important characteristic of the proposed reverse body biasing technique is temperature insensitivity. Both g_m and $g_{\rm mb}$ are affected by the temperature, but the ratio $g_{\rm mb}/g_m$ remains approximately constant. To illustrate the effect of temperature, g_m, $g_{\rm mb}$, and the ratio $g_{\rm mb}/g_m$ are listed in Table IV at three reverse body voltages (0, -1, and -3 V) and at three different temperatures (-40 °C, 27 °C, and 165 °C). As shown in this table, at constant body bias, the effect of temperature on $g_{\rm mb}/g_m$ is negligible.

V. CASE STUDY

The proposed flow to evaluate the significance of switching noise and reverse body biasing to reduce input-referred switching noise are applied to a potentiostat circuitry as a case study. The potentiostat array architecture is introduced in Section V-A. Application of the proposed analysis flow is described in Section V-B. Reverse body bias is applied to reduce input-referred switching noise, as discussed in Section V-C.

A. Potentiostat Array Architecture

A 16-channel potentiostat, integrated with microfabricated sensor array, is used for real time and sensitive detection of neurotransmitter concentration [31], [32]. This potentiostat array measures the redox current proportional to the concentration of electroactive neurotransmitters, while keeping the potential of the sensor electrode at specific redox potential [33]. The detection of the neurotransmitters is critical for neural pathways and the etiology of neurological diseases like epilepsy and stroke.

The primary challenges in the design process of a potentiostat are high input sensitivity and wide dynamic range. Input noise should be minimized to enhance these design objectives. It is therefore of primary importance to identify the dominant component of the input noise and evaluate the significance of switching noise.

A single channel of a potentiostat consists of a first-order single-bit delta-sigma modulator as the analog-to-digital converter, a counter for decimation, and a shift register, as shown in Fig. 15. The delta–sigma modulator consists of a current integrator, comparator, and switched-current 1-bit digital-to-analog converter in the feedback loop. Sense amplifier in the current integrator is the primary victim block that is highly sensitive to both induced and intrinsic noise. Alternatively, the counter is the primary aggressor that generates high switching noise. Note that the sense amplifier is a single-stage cascode amplifier with feedback, designed in 0.5-μm CMOS technology, as shown in Fig. 16. The input DC current is 1 pA and the load capacitance of the amplifier is 1 pF.

B. Application of the Proposed Analysis Flow

The switching noise generated by the counter (aggressor) propagates throughout the substrate and reaches the bulk nodes of the nMOS transistors in the sense amplifier. Thus, the first step in quantifying the input-referred switching noise is to determine the switching noise profile at the bulk node of these transistors. This step is achieved by discretizing the physical structure of the substrate into unit cells and modeling each unit cell with lumped parasitic impedances (consisting of resistance and capacitance), as further described in [34]. The overall network is then simulated in SPICE to determine

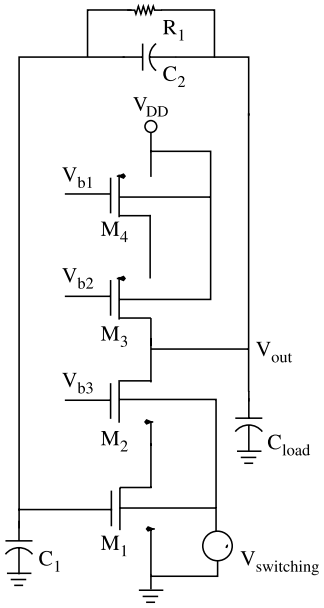

Fig. 16. Schematic of the sense amplifier where switching noise is inserted at the bulk nodes of nMOS transistors.

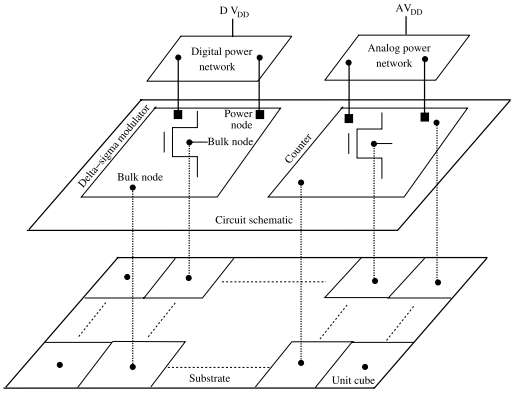

Fig. 17. Conceptual representation of the overall model to analyze noise profile at the bulk nodes of the victim transistors.

noise profiles at the bulk nodes. Also referred to as 3-D-transmission line matrix (3-D-TLM) method [35], the accuracy of this technique has been previously verified by comparing the results with the 3-D field solvers [36] and the experimental data [37]. A conceptual representation of the overall model (based on 3-D-TLM) to determine the switching noise profile at the bulk nodes is shown in Fig. 17. Note that other existing techniques (such as finite-difference method or boundary-element method) can also be used in this step.

The noise profile V_{swi} obtained in the first step is shown in Fig. 18 in time domain. The peak noise is in the range of 5–10 mV, whereas the rms noise is approximately 230 μV.

By utilizing the proposed analysis flow, both equivalent input device noise and input-referred switching noise (first figure-of-merit proposed in this paper) are quantified in the frequency domain. The overall input-referred switching noise due to digital activity and equivalent input device noise due to both active and passive devices are compared in Fig. 19. As illustrated in this figure, at low frequencies, switching noise

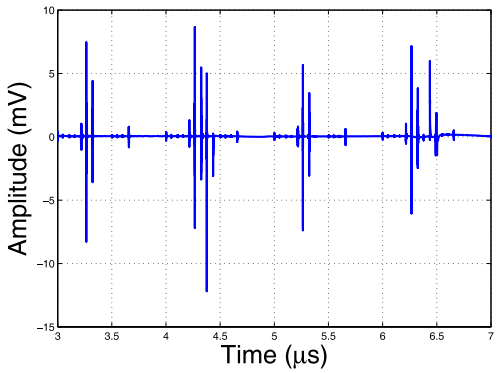

Fig. 18. Switching noise profile at the bulk node of the nMOS transistors in time domain.

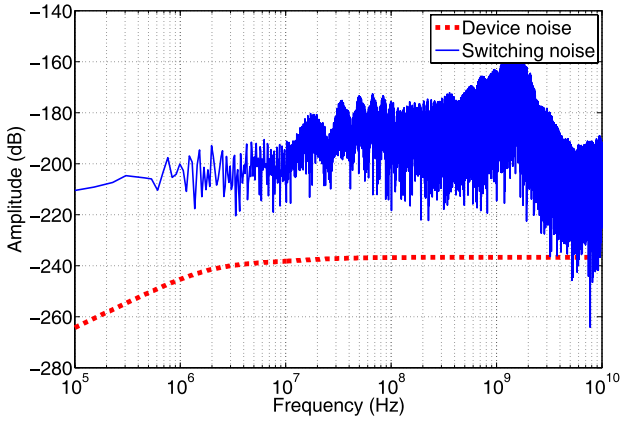

Fig. 19. Comparison of input-referred switching noise and equivalent input device noise in the sense amplifier of the potentiostat.

dominates device noise, where the difference is approximately 40 dB. As the frequency is increased, this difference is initially reduced to approximately 20 dB at 10 MHz. As the frequency increases further, however, switching noise increases whereas device noise remains constant. This result is accurate until approximately 1 GHz, beyond which switching noise starts to decrease. According to this analysis, switching noise dominates device noise within the frequency range of interest. Thus, to increase the input sensitivity of the potentiostat, the counter (primary digital block with high switching activity) should be sufficiently isolated from the sense amplifier (primary victim block). Note that the switching noise analysis is performed when the counter and sense amplifier have separate power/ground networks. Substrate, however, remains as the primary medium for the transmission of switching noise. The noise that couples to the bulk nodes of the transistors significantly contributes to the input-referred current noise.

C. Application of Reverse Body Bias

Reverse body biasing is applied to the input nMOS transistor within the sense amplifier to alleviate input-referred switching noise. The effect of reverse body biasing on g_m, g_{mb}, amplifier gain, output swing, phase margin, and bandwidth are listed in Table V for different bias voltages. It is shown that, up to -3 V, g_m, dc gain, output swing, bandwidth, and phase margin remain approximately the same while g_{mb} is

TABLE V

EFFECT OF REVERSE BODY BIASING ON PRIMARY PERFORMANCE CHARACTERISTICS OF THE SENSE AMPLIFIER WITHIN THE POTENTIOSTAT

V_B (V)	I_D (nA)	DC gain (dB)	g_m	g_{mb}	g_{mb}/g_m	V_{GS} (V)	V_{th} (V)	Output swing (V)	Phase margin	Bandwidth (Hz)
0	956.5	179.9990	24.8 μ	9.752 μ	0.393	660 m	643.2 m	2.4643	86.93°	159.147
-1.2	956.4	179.9992	26.5 μ	5.384 μ	0.203	995.3 m	981.3 m	2.4639	86.92°	159.152
-2.4	956.4	179.9993	26.8 μ	3.480 μ	0.129	1.19	1.176	2.4637	86.94°	159.152
-3	956.4	179.9993	26.9 μ	2.887 μ	0.107	1.26	1.247	2.4637	86.98°	159.153

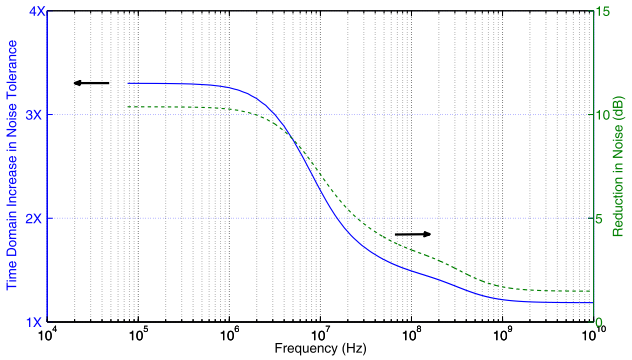

Fig. 20. Noise reduction and time domain increase in noise tolerance when −3 V is applied as the reverse body bias.

significantly reduced, weakening the bulk-to-input transfer function. Note that as opposed to the two-stage and folded cascode amplifiers discussed in the previous section, the sense amplifier in this case study operates in a closed loop with a large feedback resistance. Thus, gain, bandwidth, and output swing are not affected by the reverse body bias.

Reduction in input-referred switching noise is shown in Fig. 20 when −3 V is applied as the reverse body bias. The y-axis on the right-hand side shows the decibel reduction in input-referred switching noise as a function of frequency. More than 10 dB reduction is demonstrated up to 1 MHz. The noise reduction decreases to 4 and 1.5 dB at, respectively, 100 MHz and 1 GHz. The y-axis on the left-hand side shows the increase in the noise tolerance as a function of frequency. Specifically, when −3 V is applied as the reverse body bias, the peak amplitude of the time-domain switching noise at the bulk nodes can be increased by more than three times (from 8 mV when bulk bias is zero to 26 mV when bulk bias is at −3 V) while maintaining the input-referred switching noise constant. Thus, significantly more substrate noise can be tolerated through reverse body biasing.

VI. CONCLUSION

An analysis flow has been proposed to evaluate the significance of switching noise in analog circuits. Switching noise at the bulk node of a transistor (modeled as a decaying sine wave) is first transmitted to the input node by utilizing the corresponding transfer functions to obtain *input-referred switching noise*. Input-referred switching noise is used as a figure-of-merit and compared with equivalent input device noise (thermal and flicker) to identify the dominance regions as a function of time-domain switching noise characteristics, such as amplitude and period. A two-stage and folded cascode amplifier are used to demonstrate the proposed flow. For both amplifiers, the time-domain switching noise amplitude that leads to equal input device and switching noise is determined as the second figure-of-merit. Knowing this amplitude is helpful to gain intuition on the required reduction in switching noise since the existing noise reduction techniques typically increase physical area and power consumption. It is also demonstrated that reverse body biasing weakens the bulk-to-input transfer function, thereby alleviating the effect switching noise without affecting the remaining design specifications, such as gain, bandwidth, output swing, and phase margin. A case study is described to apply the proposed flow and reverse body biasing to a potentiostat circuitry where the input sensitivity is critical. Noise dominance regions are identified and up to 10 dB reduction in input-referred switching noise is demonstrated through reverse body biasing.

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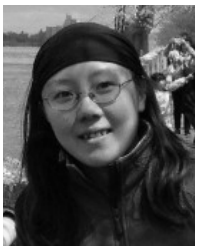

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