Methodology to Determine Dominant Noise Source in a System-On-Chip Based Implantable Device

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***Abstract*—In a mixed-signal environment, a challenging issue during the design process of analog circuits is the evaluation of the dominant noise source. A fair comparison of intrinsic (device) noise with induced (switching) noise is highly important to enhance design constraints such as input sensitivity and signal-to-noise ratio. A methodology and analysis flow are proposed to quantify and compare input-referred device noise with input-referred switching noise in a system-on-chip based implantable device, where input sensitivity is a critical design constraint. It is demonstrated that switching noise due to substrate coupling is approximately 30 dB higher than device noise in the frequency range of interest.**

I. INTRODUCTION

Noise analysis is a primary concern in heterogeneous mixed-signal circuits due to high sensitivity of the analog/RF blocks [1]. Electrical noise in integrated circuits is typically categorized in two domains: (1) induced (also referred to as switching) noise due to high switching activity of the digital blocks and (2) intrinsic (also referred to as device) noise due to active and passive devices [2]. Primary device noise sources include thermal [3], flicker [4], and shot noise [5]. Alternatively, substrate is the primary medium for the switching noise to propagate throughout the die and couple to the sensitive transistors [6].

Accurate identification of the dominant noise source is highly important to enhance design objectives. In the existing work, *ad-hoc* techniques and coarse assumptions are typically utilized to determine the dominant noise source [7], [8]. A methodology is introduced in this paper to quantify different noise sources and compare intrinsic and induced noise in the frequency domain. An implantable potentiostat that monitors neurochemical activity is utilized as the mixed-signal system-on-chip [9]. A potentiostat measures the redox current, which is typically in the range of picoamperes. Due to this extremely small current magnitude, input sensitivity is a critical design objective. Input-referred noise should be reduced to enhance signal-to-noise ratio, thereby increasing input sensitivity. An analysis flow is proposed in this paper to quantify the contribution of both device and switching noise to the overall input-referred current noise.

The rest of the paper is organized as follows. Operation of an implantable potentiostat is summarized in Section II. The proposed analysis flow to determine the dominant input-referred noise is described in Section III. The paper is concluded in Section IV.

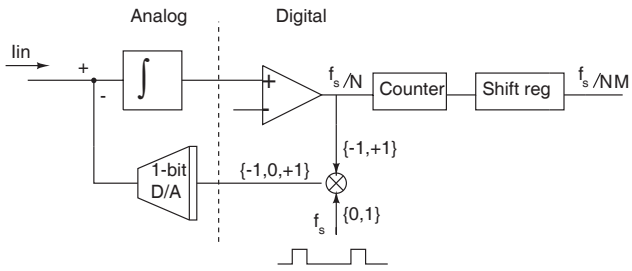

Fig. 1. **System level diagram of a single channel of the potentiostat.**

II. POTENTIOSTAT ARRAY ARCHITECTURE

A 16-channel potentiostat, integrated with microfabricated sensor array, is used for real time and sensitive detection of neurotransmitter concentration [9], [10]. This potentiostat array measures the redox current proportional to the concentration of electroactive neurotransmitters, while keeping the potential of the sensor electrode at specific redox potential [11]. The detection of the neurotransmitters is critical for neural pathways and the etiology of neurological diseases like epilepsy and stroke. The primary challenges in the design process of a potentiostat are high input sensitivity and wide dynamic range. Input-referred noise should be minimized to enhance these design objectives. It is therefore of primary importance to identify the dominant component of the input-referred noise.

A single channel of a potentiostat consists of a first order single-bit delta-sigma modulator as the analog-to-digital converter, a counter for decimation, and a shift register, as depicted in Fig. 1. The delta-sigma modulator consists of a current integrator, comparator, and switched-current 1-bit digital-to-analog converter in the feedback loop. Sense amplifier in the current integrator is the primary victim block that is highly sensitive to both induced and intrinsic noise. Alternatively, the counter is the primary aggressor that generates high switching noise. Note that the sense amplifier is a single stage cascode amplifier with feedback designed in 0.5 μm CMOS technology, as described in the following section.

III. PROPOSED NOISE ANALYSIS FLOW

The analysis methodology for *input-referred switching noise* and *input-referred device noise* are described, respectively, in Sections III-A and III-B.

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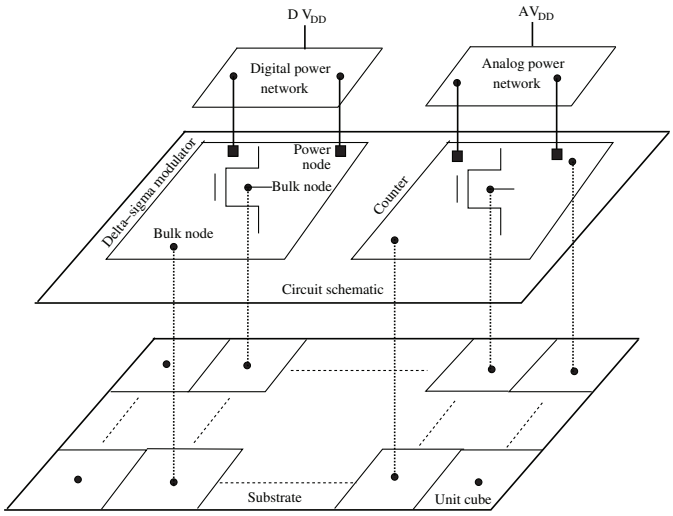

Fig. 2. **Conceptual representation of the overall model to analyze noise profile at the bulk nodes of the victim transistors.**

A. Input-referred Switching Noise Analysis

The switching noise generated by the counter (aggressor) propagates throughout the substrate and reaches the bulk nodes of the N-MOS transistors in the sense amplifier. Thus, the first step in quantifying the input-referred switching noise is to determine the switching noise profile at the bulk node of these transistors. This step is achieved by discretizing the physical structure of the substrate into unit cells and modeling each unit cell with lumped parasitic impedances, as further described in [12]. The overall network is then simulated to determine noise profiles at the bulk nodes. Also referred to as three-dimensional transmission line matrix method (3D-TLM) [13], the accuracy of this technique has been previously verified by comparing the results with 3-D field solvers [14] and experimental data [15]. A conceptual representation of the overall model (based on 3D-TLM) to determine the switching noise profile at the bulk nodes is depicted in Fig. 2. Details of this step are described in [12]. The primary purpose of this paper is to transfer this voltage noise to the input node as current noise, and compare the result with input-referred device noise, thereby identifying the dominant noise source as a function of frequency.

The noise profile V_{swi} obtained in the first step is illustrated in Fig. 3 in both time and frequency domains. The peak noise is in the range of five to ten millivolts whereas the RMS noise is approximately 230 μV. The switching noise spectrum at the bulk node is transferred to the input stage of the sense amplifier by utilizing two transfer functions V_{out}/V_{bulk} and V_{out}/I_{in},

$$\text{Input-referred switching current noise} = \frac{V_{out}/V_{bulk}}{V_{out}/I_{in}} \times V_{swi}(\omega). \tag{1}$$

Referring to the schematic of the sense amplifier shown in Fig. 4, V_{out} is the output voltage, V_{bulk} is the voltage at the bulk nodes of M_1 and M_2, and I_{in} is the input current. C_1=1 pF represents the capacitance of the sensor that the input of the sense amplifier is connected to. The feedback loop consists of C_2=1 pF and R_1=1 GΩ. Note that R_1 is required to ensure a proper DC operating point. Finally, C_L=1 pF is the output load capacitance.

The aforementioned transfer functions are quantitatively obtained. From a small signal analysis, the first transfer function V_{out}/V_{bulk} is

$$(\frac{V_{out}}{V_{bulk}}) = L \times \frac{(1+\frac{s}{\omega_{z1}})+(1+\frac{s}{\omega_{z2}})+\ldots+(1+\frac{s}{\omega_{zn}})}{(1+\frac{s}{\omega_{p1}})+(1+\frac{s}{\omega_{p2}})+\ldots+(1+\frac{s}{\omega_{pn}})}, \tag{2}$$

where ω_{z1} to ω_{zn} are the magnitude of zeros and ω_{p1} to ω_{pn} are the magnitude of poles. L is the low frequency transfer function from the output node to the bulk nodes of the N-MOS transistors,

$$L = \frac{g_{mb1}r_{o2}(Z_1+Z_2)a - g_{mb1}ac(Z_1+Z_2) - g_{mb2}r_{o2}(Z_1+Z_2)a}{(Z_1+Z_2)c + g_{m1}Z_1ac + ac + (Z_1+Z_2)a - g_{m1}Z_1r_{o2}a}, \tag{3}$$

where

$$Z_1 = 1/C_1 s, \tag{4}$$

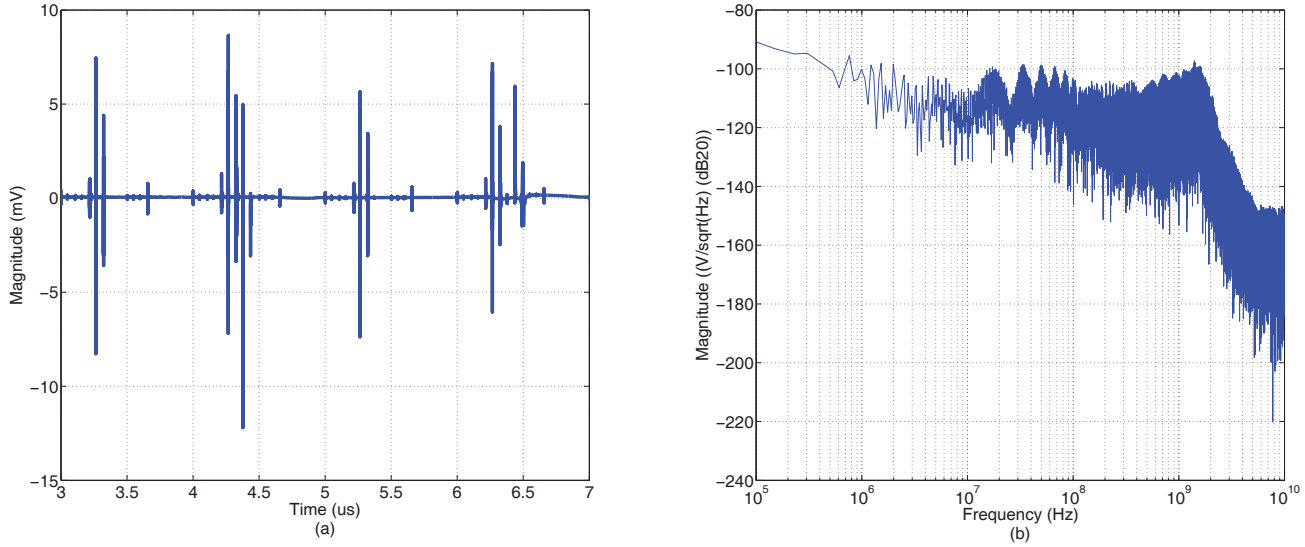

Fig. 3. **Switching noise profile at the bulk of N-MOS transistors: (a) time domain, (b) frequency domain.**

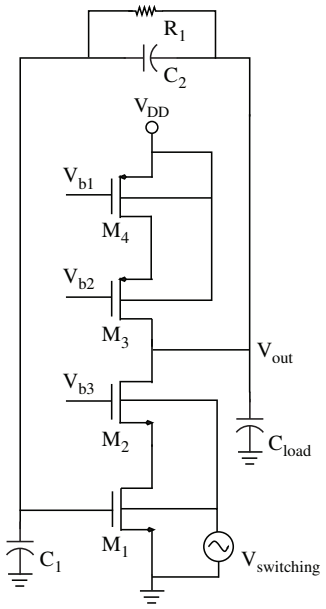

Fig. 4. **Schematic of the sense amplifier where switching noise at the bulk nodes is illustrated.**

$$Z_2 = R_1 \parallel \frac{1}{C_2 s}, \tag{5}$$

$$a = r_{o3} + r_{o4} + g_{m3} r_{o3} r_{o4}, \tag{6}$$

$$b = r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2}, \tag{7}$$

$$c = r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2} + g_{mb2} r_{o1} r_{o2}. \tag{8}$$

g_m and g_{mb} are, respectively, the transconductance of the gate and bulk nodes of the transistor, r_o is the channel resistance.

Similarly, the second transfer function V_{out}/I_{in} is

$$\frac{V_{out}}{I_{in}} = \frac{R_1 \times A(\omega)}{[A(\omega) - 1] + [R_1 C_2 A(\omega) - R_1 C_1 - R_1 C_2] s}, \tag{9}$$

where $A(\omega)$ is the open loop gain of the cascode amplifier. To demonstrate the accuracy of this technique, input-referred switching noise obtained from (1) is compared with simulation results in Fig. 5. Note that the noise source at the bulk nodes is the same in both cases, as depicted in Fig. 3. As illustrated in Fig. 5, the analytic equations closely match the simulation results, demonstrating the accuracy of the transfer functions (2) and (9). The frequency spectrum of the input-referred switching noise due to digital activity is therefore accurately estimated.

B. Input-Referred Device Noise Analysis

The second step in identifying the dominant noise source is to analyze the input-referred device noise. The same circuit shown in Fig. 4 is used for the device noise analysis. The switching noise source $V_{swi}(\omega)$ at the bulk nodes is removed, and a current source $I_{device}(\omega)$ is placed between the drain and source of each transistor as well as across the feedback resistance to model the thermal noise. The power spectral density of the thermal noise of the MOS transistors is [16],

$$I^2_{device} = 4KT\gamma g_m, \tag{10}$$

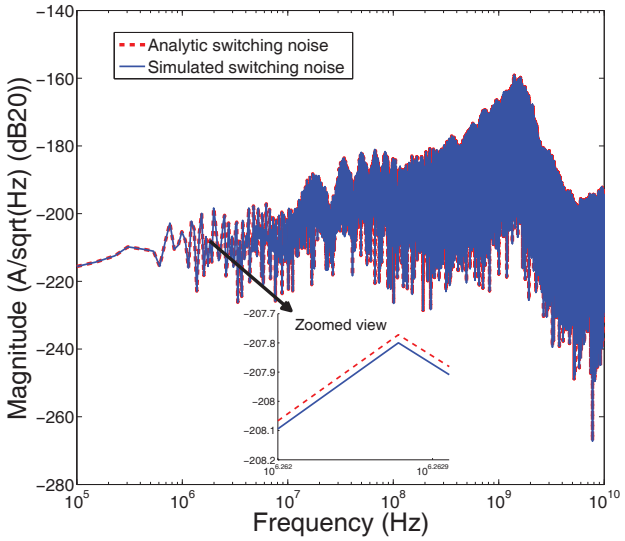

Fig. 5. **Comparison of the input-referred switching noise obtained by (1) with simulation results.**

where K is Boltzmann's constant, T is temperature in Kelvin, γ is thermal noise coefficient, and g_m is the drain-to-source transconductance when $V_{DS} = 0$. Note that only thermal noise is considered in this analysis since the flicker noise is negligible in the frequency range of interest. The input-referred current noise is determined by transferring the noise sources to the input node through the frequency dependent transfer functions,

$$\text{Input-referred device current noise} = \frac{V_{out}/I_s}{V_{out}/I_{in}} \times I_{device}(\omega), \tag{11}$$

where I_s is the AC current source between drain and source of each transistor. Note that the noise due to the feedback resistance is separately analyzed, as described later in this section. The general structure of $(V_{out}/I_s)_m$ for each transistor m is

$$(\frac{V_{out}}{I_s})_m = K_m \times \frac{(1+\frac{s}{\omega^m_{z1}}) + (1+\frac{s}{\omega^m_{z2}}) + \ldots + (1+\frac{s}{\omega^m_{zn}})}{(1+\frac{s}{\omega^m_{p1}}) + (1+\frac{s}{\omega^m_{p2}}) + \ldots + (1+\frac{s}{\omega^m_{pn}})}, \tag{12}$$

where ω^m_{z1} to ω^m_{zn} and ω^m_{p1} to ω^m_{pn} are, respectively, the magnitude of zeros and poles. K_m is the transfer function V_{out}/I_s at low frequency. Note that both the location of poles/zeros and K_m are different for each transistor. The value of K_m for M_1, M_2, M_3, and M_4, are, respectively,

$$K_1 = \frac{V_{out}}{I_{s1}} = \frac{a(Z_1+Z_2)(b-r_{o2})}{(Z_1+Z_2)(-b-a) - ab - g_{m1}Z_1 ab + g_{m1}Z_1 r_{o2} a}, \tag{13}$$

$$K_2 = \frac{V_{out}}{I_{s2}} = \frac{a(Z_1+Z_2)r_{o2}}{(Z_1+Z_2)(-b-a) - ab - g_{m1}Z_1 ab + g_{m1}Z_1 r_{o2} a}, \tag{14}$$

$$K_3 = \frac{V_{out}}{I_{s3}} = \frac{b(Z_1+Z_2)r_{o3}}{(Z_1+Z_2)(a+b) + ab + g_{m1}Z_1 ab - g_{m1}Z_1 r_{o2} a}, \tag{15}$$

$$K_4 = \frac{V_{out}}{I_{s4}} = \frac{b(Z_1+Z_2)(a-r_{o3})}{(Z_1+Z_2)(a+b) + ab + g_{m1}Z_1 ab - g_{m1}Z_1 r_{o2} a}, \tag{16}$$

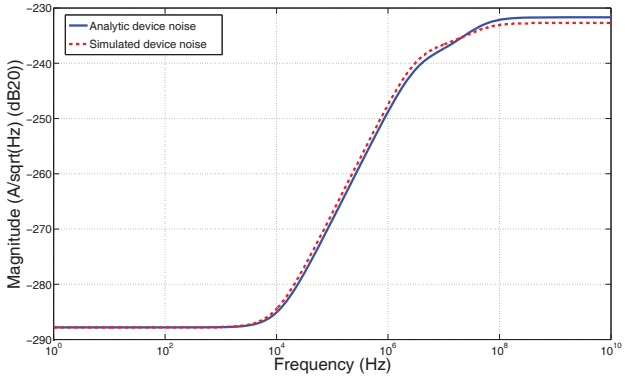

Fig. 6. **Comparison of calculated and simulated input-referred device noise.**

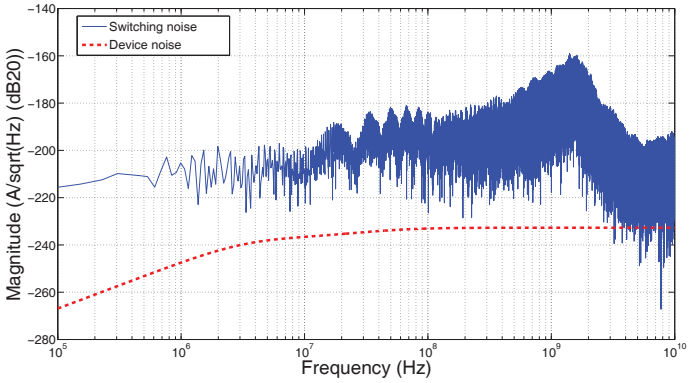

Fig. 7. **Comparison of input-referred switching noise and input-referred device noise in the sense amplifier of the potentiostat.**

where Z_1, Z_2, a, and b are given, respectively, by (4), (5), (6), and (7). Utilizing these expressions, the power spectral density $V^2_{out,noi}$ of the device noise at the output node due to four MOS transistors is

$$V^2_{out,noi} = [I^1_{device} \times (\frac{V_{out}}{I_s})_1]^2 + ... + [I^4_{device} \times (\frac{V_{out}}{I_s})_4]^2. \quad (17)$$

According to (11), once the overall noise at the output is obtained, the RMS result is divided by (9), *i.e.*, V_{out}/I_{in}, to determine input-referred current noise due to transistors.

Finally, the thermal noise of the feedback resistance R_1 is modeled as a current noise source $4KT/R_1$ in parallel with R_1. According to Blakesley's theorem [17], the spectral density of this noise remains the same at the input. Thus, the overall input-referred current noise due to both active and passive devices is

$$I^2_{noi} = I^2_{n,cascode} + \frac{4KT}{R_1}. \quad (18)$$

To demonstrate the accuracy of these expressions, input-referred current noise obtained by (12) or (18) is compared with the noise simulations performed by Spectre. As depicted in Fig. 6, the analytic data closely match the simulation results. Specifically, the device noise at the input is flat at -287 dB until approximately 10 KHz. Beyond this frequency, the noise starts to increase until approximately 100 MHz, and remains constant at -233 dB.

C. Comparison

As mentioned previously, input-referred current noise is a critical parameter for an implantable potentiostat designed to sense neurotransmitter concentration. Since a lower noise at the input increases the sensitivity of the device, it is highly desirable to identify the dominant noise source. The overall input-referred switching noise due to digital activity and input-referred device noise due to both active and passive devices are compared in Fig. 7. As illustrated in this figure, at low frequencies, switching noise dominates device noise, where the difference is approximately 40 dB. As the frequency is increased, this difference is initially reduced to approximately 20 dB at 10 MHz. As the frequency increases further, however, switching noise increases whereas device noise remains constant. This result is accurate until approximately 1 GHz, beyond which switching noise starts to decrease. According to this analysis, switching noise dominates device noise within the frequency range of interest. Thus, to increase the input sensitivity of the implantable device, the counter (primary digital block with high switching activity) should be sufficiently isolated from the sense amplifier (primary victim block). Note that the switching noise analysis is performed when the counter and sense amplifier have separate power/ground networks. Substrate, however, remains as the primary medium for the transmission of switching noise. The noise that couples to the bulk nodes of the transistors significantly contributes to the input-referred current noise.

IV. CONCLUSION

An analysis flow has been proposed to identify the dominant noise source at the input node of an implantable potentiostat where input sensitivity is a primary design objective. Both induced (switching) and inherent (device) noise have been analyzed. The accuracy of the proposed analytic expressions has been evaluated by comparing the results with transistor-level simulations in Spectre. Sufficient accuracy for both input-referred induced and inherent noise has been demonstrated. According to the comparison, within the frequency range of interest, input-referred current noise is dominated by the switching noise that propagates throughout the substrate and reaches the bulk nodes of the transistors rather than the thermal noise. Thus, to increase input sensitivity of the implantable device, efficient substrate noise isolation techniques should be developed.

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