# Power Distribution in TSV-Based 3-D Processor-Memory Stacks

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***Abstract*—Three primary techniques for manufacturing through silicon vias (TSVs), via-first, via-middle, and via-last, have been analyzed and compared to distribute power in a 3-D processor-memory system with nine planes. Due to distinct fabrication techniques, these TSV technologies require significantly different design constraints, as investigated in this paper. A valid design space that satisfies the peak power supply noise while minimizing area overhead is identified for each technology. It is demonstrated that the area overhead of a 3-D power distribution network with via-first TSVs is approximately 9% as compared to less than 2% in via-middle and via-last technologies. Despite this drawback, a via-first based power network is typically overdamped and the issue of resonance is alleviated. A via-last based power network, however, exhibits a relatively low damping factor and the peak noise is highly sensitive to the number of TSVs and decoupling capacitance.**

***Index Terms*—Decoupling capacitance, embedded memory, IR drop, Ldi/dt noise, power delivery, power supply noise, processor-memory stacks, three-dimensional (3-D) integrated circuits, through silicon via (TSV), via-first , via-middle, via-last.**

## I. Introduction

OVER the past decade, various novel integrated circuit (IC) technologies have emerged to alleviate the scaling challenges of planar ICs [1]. Through silicon via (TSV)-based 3-D integration is a promising technology that maintains the benefits of miniaturization by enabling higher integration density and enhancing system performance [2]–[7]. In wafer-level 3-D integration technologies, multiple wafers are thinned, aligned, and vertically bonded. Communication among the dies is achieved by high density TSVs. Global interconnect length is therefore reduced, lowering the overall power dissipation and latency. Three-dimensional integration also provides unique advantages to develop highly heterogeneous systems where diverse functions such as analog/RF-based communication blocks, sensing circuitry, digital data processing blocks, and sensors are merged in a monolithic fashion [4], [8], [9]. Another important application of 3-D integration technology is stacked processor-memory systems, as illustrated in Fig. 1.

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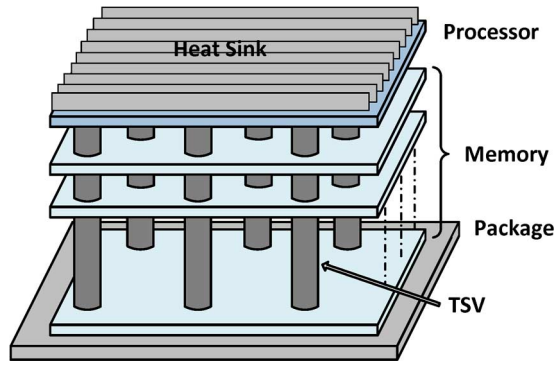


Fig. 1. Three-dimensional integration of dynamic random access memory with the processor.

The difference in the performance of a processor and memory has grown due to significantly different scaling characteristics [10]. This growing disparity between logic and memory remains as a primary bottleneck to further increase the overall throughput. This issue has been partly relieved with the introduction of multi-level cache structures with varying size and speed [11]. However, further increase in the size and number of hierarchical cache levels is highly challenging due to a significant increase in the complexity of cache control logic. Three-dimensional technology alleviates the existing gap between logic blocks and memory units in high performance microprocessors by utilizing vertically embedded dynamic random access memory (DRAM), thereby significantly increasing the memory bandwidth and reducing memory access time. Also note that thermal issues (a significant limitation in login-on-logic 3-D integration [12]) are partially alleviated in memory-on-logic integration since the switching activity and power consumption within the memory planes are significantly lower. Thus, International Technology Roadmap for Semiconductors (ITRS) identifies processor-memory stacks as a near term application of 3-D ICs [13].

A significant circuit- and physical-level challenge in this system is to design a robust power distribution network that achieves reliable power delivery to each die. Maintaining the power network impedance smaller than a target impedance is a difficult task due to reduced operating voltages, increased current magnitudes, and the existence of multiple dies and TSVs. A conservatively large number of power/ground TSVs can significantly increase the area overhead in addition to producing high inductive characteristics due to a smaller damping factor, as demonstrated in this paper.

Previous work on 3-D power delivery has focused on different power distribution topologies, effect of TSV geometry,

and core versus coaxial TSVs [14]–[17]. For example, Wu and Zhang have proposed a strategy to place the TSVs and the decoupling capacitors in a processor-memory system [14]. A method to place decoupling capacitance by exploiting the proximity between the processor die and the DRAM dies has been proposed. Khan *et al.* have performed an architectural analysis of power delivery in 3-D circuits [15]. The impact of TSV size and spacing, C4 (controlled collapse chip connection) bump spacing, and co-axial TSVs has been investigated. Both of these works, however, are based on via-last TSVs. Other TSV fabrication technologies such as via-first and via-middle have not been considered.

Existing work on different TSV technologies primarily focus on fabrication characteristics rather than circuit design requirements. For example, in [18] and [19], via-first TSV technology has been investigated with little attention on circuit design implications. Similarly, via-middle TSVs have been discussed in [20]–[22] focusing primarily on process characteristics. The fabrication constraints of the three TSV technologies are also compared in [23]. Furthermore, yield characteristics of these TSV technologies are analyzed and compared in [24].

Pavlidis and De Micheli have investigated the presence of alternative low impedance current paths in via-first TSVs [17]. These additional current paths have been exploited, resulting in a 22% reduction in the number of intraplane vias or alternatively, a 25% decrease in the required decoupling capacitance [17]. The same filling material, however, has been considered for both via-first and via-last TSVs. Furthermore, a simplified model has been assumed for the power distribution network within each plane.

Via-first, via-middle, and via-last TSV technologies exhibit unique advantages and limitations. A power distribution network in each case exhibits significantly different design requirements, as evaluated in this paper. A nine plane 3-D system with eight planes of embedded DRAM and a single processor plane is considered. The three primary contributions of this paper are as follows: 1) via-first, via-middle, and via-last TSV technologies are explored in a comparative manner to distribute power in a 3-D processor-memory system, 2) design space that satisfies power supply noise while minimizing the overall physical area is determined, and 3) a power loss analysis is performed and design guidelines are provided for each TSV technology.

The rest of the paper is organized as follows. The primary characteristics of the three TSV fabrication technologies are summarized in Section II. Electrical models used to analyze the power distribution network are described in Section III. Approach and simulation results of the power supply noise analysis and power loss are provided in Section IV. The design implications of these results are discussed in Section V. Finally, the paper is concluded in Section VI.

## II. TSV Fabrication Technologies

Each TSV technology exhibits unique challenges during the design process of a 3-D power distribution network. These differences arise due to distinct fabrication techniques. The fabrication characteristics and relative physical dimensions of via-first, via-middle, and via-last TSVs are summarized, respectively, in Sections II-A, II-B, and II-C. These properties are also listed in Table I. Note that process technologies to manufacture TSVs are currently under investigation based on recent research results on wafer thinning, alignment accuracy, mechanical stress, and bonding methods. Thus, TSV geometries for a certain TSV type may vary depending upon the foundry.

TABLE I
Characteristics of Via-First, Via-Middle, and Via-Last TSVs [18], [25], [20]–[22], [25], [25]–[30]

| Parameter | Via-first | Via-middle | Via-last |
|---|---|---|---|
| Filling material | Doped polysilicon | Tungsten | Copper |
| Structure | Cylindrical | Annular and conical | Cylindrical |
| Processing temperature | High | Average | Low |
| Manufacturability | Difficult | Very difficult | Established |
| Formation | Before FEOL | Before BEOL | After BEOL |
| Electrical characteristics | Highly resistive | Resistive and inductive | Inductive |
| Landing metal | $M_1$ | $M_1$ | $M_{Top}$ |
| Take-off metal | $M_{Top}$ | $M_{Top}$ | $M_{Top}$ |

### A. Via-First TSV

In a via-first method, TSVs are fabricated before the transistors are patterned in silicon, i.e., prior to front-end-of-line (FEOL) [18], [25], [26], [28]. Thus, TSVs fabricated with the via-first technique do not pass through the metallization layers, as depicted in Fig. 2(a). The TSV of a plane is connected between the first metal layer of the current plane and the top most metal layer of the previous plane. Polysilicon is typically used as the filling material due to its ability to withstand high temperatures [18], [25], [26], [28]. Via-first TSVs are less sensitive to contamination since both the filling and substrate materials are the same [27]. The physical dimensions of via-first TSVs are smaller than via-last TSVs [30]. Via-first TSVs, however, are highly resistive and have a lower filling throughput due to the use of polysilicon as the filling material [27].

### B. Via-Middle TSV

In a via-middle process, TSVs are fabricated after FEOL, but before the metallization layers are patterned, i.e., prior to back-end-of-line (BEOL) [20]–[22], [27], [29]. Similar to via-first TSVs, via-middle TSVs connect the first metal layer of a plane with the last metal layer of the previous plane, as illustrated in Fig. 2(b). Since the high temperature FEOL process precedes TSV fabrication steps, via-middle process permits the use of tungsten as the filling material, which is significantly less resistive as compared to doped polysilicon. Tungsten can be used as the filling material due to low thermal expansion coefficient (4.6 ppm/K) as compared to copper (17 ppm/K) [21]. A material with low sensitivity to temperature is required since the TSV fabrication step is followed by a moderately high temperature BEOL process. Note however that copper filled via-middle TSVs have also been recently demonstrated [31].

Via-middle TSVs require a relatively large (12:1 or higher) aspect ratio [20]–[22], [29]. Thus, the width of via-middle TSVs is comparable to the width of via-first TSVs whereas the height is comparable to via-last TSVs. This characteristic produces a

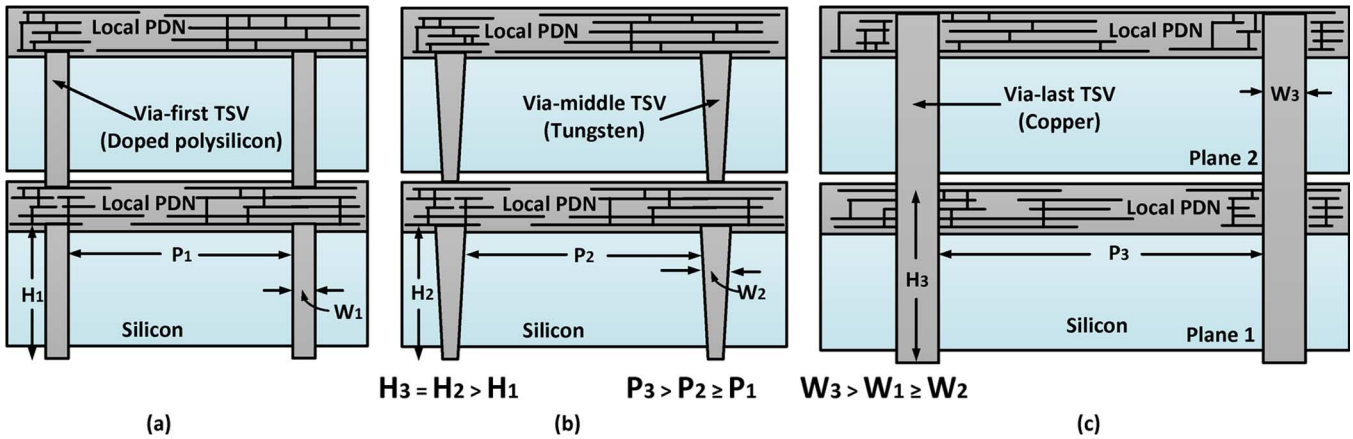


Fig. 2. Illustration of the three primary TSV technologies: (a) via-first, (b) via-middle, and (c) via-last.

relatively high inductive behavior. Also note that the fabrication process of via-middle TSVs is relatively more challenging. For example, a conformal barrier process is required for the tungsten to adhere to the dielectric in the cavity. A 20-nm titanium nitride (TiN) layer is typically deposited using metal organic chemical vapor deposition (MOCVD) [20]. TiN is a hard, dense, refractory material with sufficiently low electrical resistivity ($22\mu\ \Omega$ cm) [32].

Another challenge is the high level of stress during the deposition of the oxide layer which is exacerbated when a conformal layer is required. This challenge is partially negated with the use of a tapered TSV structure that progressively shrinks in size [20], [21]. This structure is illustrated in Fig. 2(b). Other challenges include sensitivity to contamination and the requirement to maintain the temperature within 500 °C [27]. Novel deposition techniques such as atomic layer deposition (ALD) and time-modulated deposition alleviate some of these issues [20], [33].

From the design perspective, via-middle technology is an interesting compromise between a highly resistive via-first and a low resistive, but highly inductive via-last TSVs. Furthermore, similar to via-first TSVs, via-middle TSVs do not cause metal routing blockages. The Semiconductor Manufacturing Technology (SEMATECH) consortium has chosen via-middle TSVs as a primary focus area [34].

### C. Via-Last TSV

In the via-last approach, TSV formation occurs after the metallization layers are fabricated, i.e., after BEOL [18], [27], [30]. Thus, as opposed to via-first and via-middle TSVs, via-last TSVs pass through the metal layers, causing metal routing blockages, as depicted in Fig. 2(c) [17], [30]. A lower resistivity filling material such as copper is used since high temperature FEOL and BEOL processes are performed before the via formation [18], [27]. The use of copper as a filling material makes the process sensitive to both temperature (should be maintained less than 230 °C) and contamination [27]. Despite exhibiting relatively low resistance, the inductive characteristics of via-last TSVs are relatively more significant than via-first TSVs due to greater dimensions [30]. The physical connection between the TSV and metal layers is typically achieved at the top most metal layer.

## III. Electrical Models for TSV-Based 3-D Power Distribution

The models used to analyze power supply noise for each TSV technology are described in this section. System level model, including the orientation of the planes and the dimensions of the dies are discussed in Section III-A. Electrical models used for TSVs, substrate, and the power distribution network within a plane are provided, respectively, in Sections III-B, III-C, and III-D. Finally, the model for the load circuit is described in Section III-E.

### A. System Level Model

In [35], Sun *et al.* have investigated the potential benefits of a nine plane 3-D stack from an architecture perspective. The authors have demonstrated that a 100 mm$^2$ processor die with eight stacked DRAM planes can achieve an overall storage capacity of 1 GB. The improvements in access latency, footprint, and energy consumption have been quantified and compared to a one-, two-, and a four-layer system.

A similar architecture is considered in this work to develop a valid design space for robust power delivery, while considering different TSV technologies. Specifically, a 3-D system in a 32 nm CMOS technology consisting of eight memory planes and one plane for the processor is considered. Each plane contains nine metal layers where the metal thickness and aspect ratio are determined according to 32 nm technology parameters [36]. The power supply voltage is equal to 1 V. Each plane occupies an area of 120 mm$^2$, excluding the TSVs and the intentional decoupling capacitance. The system has 1 GB of DRAM spread uniformly across eight memory planes. Each memory plane has 1 Gb DRAM divided into 32 modules of equal size, where each module has 32 Mb memory. Similarly, the processor plane is also divided into 32 modules. Each of these modules consume an area of $1500 \times 2500\ \mu$m$^2$. This topology is depicted in Fig. 3. For via-first and via-middle technologies, the TSVs are placed beneath the active circuit, as illustrated in Fig. 3(a) whereas in via-last technology, the power and ground TSVs are distributed

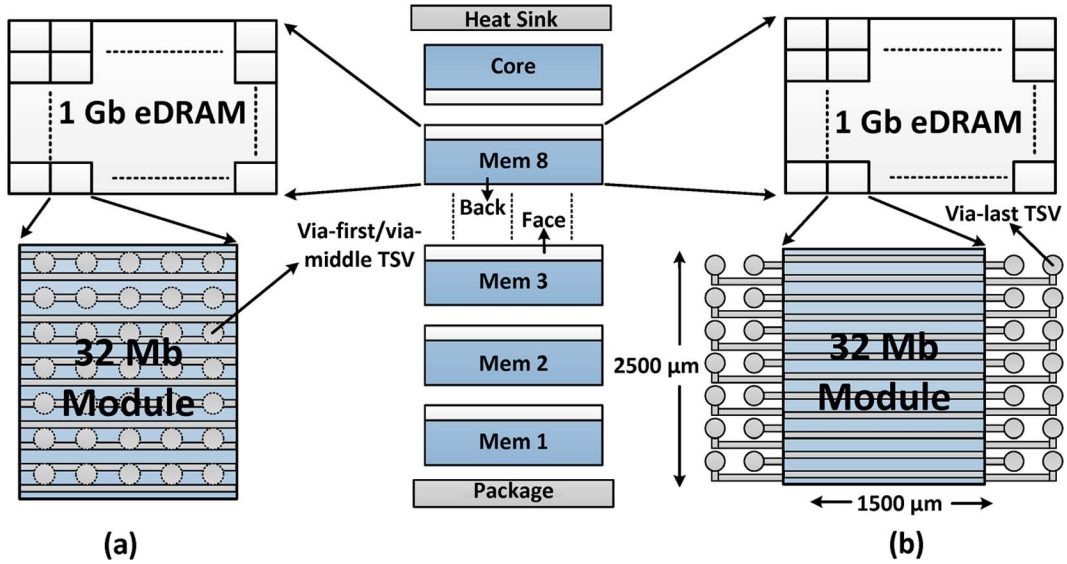


Fig. 3. 3-D processor-memory stack: (a) via-first and via-middle technologies where TSVs are placed beneath the active circuit and (b) via-last technology where TSVs are distributed on both sides of each module.

on both sides of each module, as depicted in Fig. 3(b). Note that although the TSVs are placed beneath the active circuit in via-first and via-middle technologies, these TSVs consume additional device area. Thus, in Fig. 3(a), the area represented by a 32 Mb DRAM module includes both the $1500 \times 2500$ $\mu$m$^2$ DRAM area and the TSV area. Note that the processor plane does not contain any TSVs, as described below.

As depicted in Fig. 3, the processor plane is typically placed closer to the heat sink due to high switching activity. The memory planes are therefore closer to the package (I/O pads) whereas the processor plane is farthest from the I/O pads. The orientation of the memory planes such as face-to-face or face-to-back exhibits a design tradeoff. The first memory plane can face the package where the metal layers are directly connected (without the TSVs) to the package pads. Alternatively, the first memory plane can face the adjacent DRAM plane. In the second option, as considered in this work, TSVs are required to connect the first memory plane with the package pads. First option eliminates these TSVs, but the additional current paths available in via-first and via-middle technologies [17] cannot be exploited in distributing power. These additional current paths exist only when the current flow is from the lowest to the highest metal layer in a plane, as described later. Another consideration is the orientation between the processor plane and the adjacent memory plane. A face-to-back approach maintains the symmetry of the 3-D system, but the communication bandwidth between the two planes is limited by the number of TSVs. Alternatively, in a face-to-face approach, processor and memory can communicate with the metal layers without requiring TSVs, thereby enhancing the communication bandwidth. This scheme, as considered in this work, also reduces the overall number of TSVs, partly compensating the additional TSVs between the first memory plane and package. Thus, TSVs are not required for the processor plane.

In the rest of this paper, the analysis is performed for an area of $1500 \times 2500$ $\mu$m$^2$, which corresponds to 32 Mb DRAM in each memory plane. Part of the processor plane that corresponds to this area is also included. The procedure is similar for the remaining 31 modules. An equivalent electrical model corresponding to the power distribution network of this portion of the system is illustrated in Fig. 4. This model consists of the TSVs, substrate, power distribution network within a plane, switching load circuit, and decoupling capacitance, as described in the following sections. Note that in addition to these on-chip impedances, the parasitic package resistance and inductance are, respectively, 3 m$\Omega$ and 100 pH at both the power and ground supplies, assuming an organic flip-chip package [37].

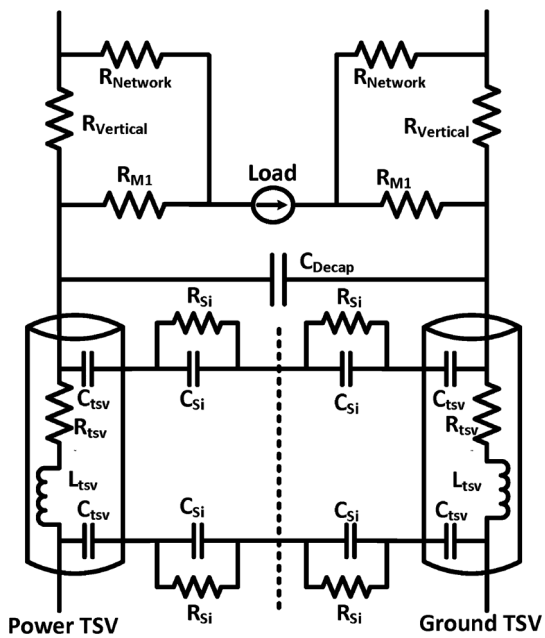


Fig. 4. Equivalent power distribution network of each module within a plane.

### B. TSV Model

A TSV is typically represented as a cylinder with a diameter $W$ and depth $H$. Aspect ratio of a TSV is given by $H/W$. The minimum distance between the two TSVs is determined by the pitch $P$, which is typically twice the TSV diameter [13]. The TSV model consists of a resistance $R_{\rm tsv}$ and inductance $L_{\rm tsv}$ due to the filling material, and a capacitance to the substrate $C_{\rm tsv}$ due to the thin dielectric layer [38]. $R_{\rm tsv}$ is determined by [39]

$$R_{\rm tsv} = \sqrt{\left(R_{\rm ac}^{\rm tsv}\right)^2 + \left(R_{\rm dc}^{\rm tsv}\right)^2} \tag{1}$$

where the dc resistance $R_{\rm dc}^{\rm tsv}$ and ac resistance $R_{\rm ac}^{\rm tsv}$ are, respectively

$$R_{\rm dc}^{\rm tsv} = \frac{\rho_f H}{\pi (W/2)^2} \tag{2}$$

$$R_{\rm ac}^{\rm tsv} = \frac{\rho_f H}{2\pi (W/2)\delta_{\rm tsv}}. \tag{3}$$

$\rho_f$ is the conductivity of the filling material and the skin depth $\delta_{\rm tsv}$ is [39]

$$\delta_{\rm tsv} = \frac{1}{\sqrt{\pi f \mu_f \rho_f}} \tag{4}$$

where $f$ is the frequency and $\mu_f$ is the permeability of the filling material. The TSV self-inductance $L_{\rm tsv}$ is [40]

$$L_{\rm tsv} = \frac{\mu_o}{4\pi}\left[2H \ln\left(\frac{2H + \sqrt{(W/2)^2 + (2H)^2}}{W/2}\right) + (W/2 - \sqrt{(W/2)^2 + (2H)^2})\right] \tag{5}$$

where $\mu_o$ is vacuum permeability. The mutual inductance between the power and ground TSVs is not considered due to high complexity and strong dependence on the physical placement of the TSVs. Note that a high mutual inductance decreases the TSV loop inductance. Thus, ignoring the mutual inductance produces a conservative (rather than an optimistic) analysis. The TSV capacitance $C_{\rm tsv}$ is determined from the cylindrical capacitor formula as [41]

$$C_{\rm tsv} = \frac{2\pi \epsilon_{ox} H}{\ln\left(\frac{W/2 + t_{ox}}{W/2}\right)} \tag{6}$$

where $\epsilon_{\rm ox}$ is the oxide permittivity.

Note that in a via-middle technology, a tapered TSV structure is utilized to mitigate the high level of stress during the TSV formation, as mentioned earlier. Thus, the resistance and inductance of via-middle TSVs are determined, respectively, by the following integrations:

$$R_{\rm tsv}^{\rm via-middle} = \int_{W_{\min}}^{W_{\max}} \frac{R_{\rm tsv}}{W_{\max} - W_{\min}}\, dW \tag{7}$$

$$L_{\rm tsv}^{\rm via-middle} = \int_{W_{\min}}^{W_{\max}} \frac{L_{\rm tsv}}{W_{\max} - W_{\min}}\, dW. \tag{8}$$

TABLE II
MODEL PARAMETERS FOR TSVS [18], [21], [40]

| Parameter | Via-first | Via-middle | Via-last |
|---|---|---|---|
| Diameter $W$ | 4 $\mu$m | 4 $\mu$m to 2.66 $\mu$m | 10 $\mu$m |
| Height $H$ | 10 $\mu$m | 60 $\mu$m | 60 $\mu$m |
| Pitch $P$ | 8 $\mu$m | 8 $\mu$m to 9.34 $\mu$m | 20 $\mu$m |
| Oxide thickness $t_{ox}$ | 0.2 $\mu$m | 0.2 $\mu$m | 0.2 $\mu$m |
| TSV resistance $R_{tsv}$ | 5.7 $\Omega$ | 858.36 m$\Omega$ | 20 m$\Omega$ |
| TSV inductance $L_{tsv}$ | 4.18 pH | 49.76 pH | 34.94 pH |
| TSV capacitance $C_{tsv}$ | 23 fF | 117.81 fF | 283 fF |
| Tapering angle | *NA* | 1° | *NA* |
| Aspect ratio AR | 2.5:1 | 15:1-22:1 | 6:1 |
| Material resistivity $\rho_f$ | 7.2 $\mu\Omega$m | 12 $\mu\Omega$cm | 16.8 n$\Omega$m |
| Substrate resistance $R_{si}$ | 8.81 k$\Omega$ | 1.57 k$\Omega$ | 1.76 k$\Omega$ |
| Substrate capacitance $C_{si}$ | 1.19 fF | 6.72 fF | 6 fF |
| Coefficient of thermal expansion *CTE* | Low | 4.6 ppm/K | 17 ppm/K |

For the via-middle TSV capacitance, (6) is utilized to calculate the arithmetic average since the effect of this capacitance is negligible when large decoupling capacitances are used, as described in Section IV. Also note that the skin effect is neglected for via-first and via-middle based TSVs due to sufficiently small TSV diameters. The maximum and minimum thickness for via-middle TSVs are listed in Table II. The primary characteristics of the three TSV technologies are also listed in this table.

### C. Substrate Model

The substrate is modeled as an $RC$ impedance, where the substrate capacitance $C_{\rm si}$ and the substrate resistance $R_{\rm si}$ are, respectively [41]

$$C_{si} = \frac{\pi \epsilon_{si} H}{\ln\left(\frac{2P}{W/2} + \sqrt{\left(\frac{2P}{W/2}\right)^2 - 1}\right)} \tag{9}$$

$$R_{si} = \frac{\epsilon_{si}\rho_{si}}{C_{si}} \tag{10}$$

where $\epsilon_{si} = 105 \times 10^{-12}$ F/m and $\rho_{si} = 10$ $\Omega$cm are, respectively, silicon permittivity and substrate resistivity.

### D. Power Distribution Network Within a Plane

Power distribution network within a plane plays an important role in analyzing power supply noise in TSV-based 3-D circuits. The characteristics of this network vary depending upon the TSV technology, as described in this section.

In the proposed 3-D processor-memory stack, the two top most metal layers ($\rm M_9$ and $\rm M_8$) in each plane are dedicated to global power distribution. The physical characteristics of the on-chip interconnects are obtained from a 32 nm CMOS technology with nine metal layers [36]. An interdigitated topology is utilized where a stack of vias, located at each intersection of $\rm M_9$ and $\rm M_8$, transmits the power supply voltage to the first metal layer, and ultimately to the switching devices. This topology is illustrated in Fig. 5. In this figure, each horizontal and vertical resistance correspond, respectively, to $\rm M_8$ and $\rm M_9$ resistance. The resistance due to the stack of vias and $\rm M_1$ is represented by the diagonal resistance. A single stack of vias from $\rm M_1$ to $\rm M_9$ is assumed to be 16 $\Omega$ [42]. Note that $\rm M_9$ is less resistive than $\rm M_8$ due to significantly greater thickness [36]. Thus, $\rm M_9$ is routed vertically since the vertical dimension is longer than

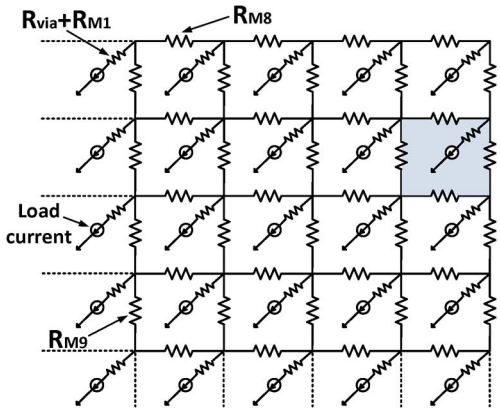


Fig. 5. Interdigitated power distribution network within a plane consisting of two top most metal layers, stack of vias and $\mathrm{M}_1$ at each intersection.

TABLE III
ON-CHIP METAL CHARACTERISTICS FOR THE GLOBAL POWER DISTRIBUTION NETWORK WITHIN EACH PLANE [36]

| Parameter | Metal 8 | Metal 9 |
|---|---|---|
| Pitch | 5.616$\mu$m | 19.4$\mu$m |
| Thickness | 504nm | 8$\mu$m |
| Width | 5.33$\mu$m | 5.33$\mu$m |
| Node to node resistance | $R_{M8}$ = 242.65 m$\Omega$ | $R_{M9}$ = 4.43 m$\Omega$ |
| Number of parallel paths | 445 | 77 |

the horizontal dimension, as depicted in Fig. 3. The number of horizontal $(\mathrm{M}_8)$ and vertical $(\mathrm{M}_9)$ lines is determined from the pitch and width of the interconnects [36]. These characteristics are listed in Table III.

Referring to Fig. 5, the physical area determined by each set of four nodes (see shaded region) is 5.62 $\mu$m $\times$ 19.4 $\mu$m. The power supply voltage is distributed to the periphery of this region by the stack of vias. Within this region, however, power is distributed by the first metal layer $\mathrm{M}_1$ of the standard cells.

Each standard cell has a height of approximately $10 \times \mathrm{M}_1$ metal lines, equal to 1.12 $\mu$m. The width of each standard cell is, on average, equal to $\mathrm{M}_8$ pitch, 5.62 $\mu$m. Since $\mathrm{M}_9$ pitch is 19.4 $\mu$m, 17 standard cells are located within the shaded region, as illustrated in Fig. 6. Note that $\mathrm{M}_8$ pitch in the global power network is greater than the minimum pitch since the $\mathrm{M}_8$ width is increased to match $\mathrm{M}_9$ width of 5.3 $\mu$m. The minimum width and pitch of $\mathrm{M}_1$ in a 32 nm technology are, respectively, 66.2 nm and 112.5 nm [36]. A metal line $(\mathrm{M}_1)$ of width 179 nm is utilized to distribute power and ground within a standard cell of width 5.62 $\mu$m, producing a resistance of approximately 326 m$\Omega$.

The current flow at each switching load circuit is represented in Fig. 7. $\mathrm{M}_8$ and $\mathrm{M}_9$ resistances represent the global power distribution network within a plane and the vertical resistance represents the stack of vias in series with the $\mathrm{M}_1$ resistance. The value of these resistances varies depending upon the TSV technology, as described in the following subsections.

*1) Via-First and Via-Middle TSVs:* In the via-first and via-middle methods, the TSVs connect the $\mathrm{M}_1$ with the $\mathrm{M}_{\mathrm{Top}}$ of the previous plane, as depicted, respectively, in Fig. 2(a) and (b). Referring to Fig. 4, the impedance due to the local metal layers connecting the two TSVs is modeled with $R_{\mathrm{Vertical}}$, which is determined by the stack of via resistance. Note that the direction of

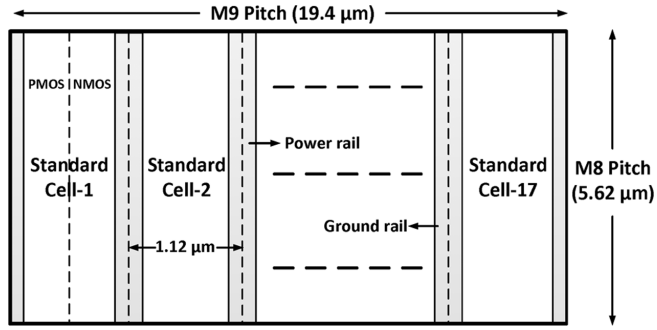


Fig. 6. Physical structure of standard cell logic.

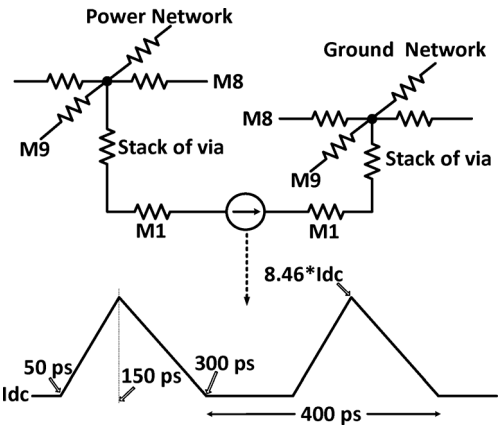


Fig. 7. Illustration of power distribution network and the characteristics of load current.

current flow on the power network within a single plane is from $\mathrm{M}_1$ to $\mathrm{M}_{\mathrm{Top}}$. Thus, alternative current paths exist in via-first and via-middle technologies, as also mentioned in [17]. These alternative current paths are illustrated in Fig. 8. As shown in this figure, the power supply voltage can be distributed only by $\mathrm{M}_1$ provided that the distance between the TSV and device is relatively small. This path is modeled by the resistance $R_{M1}$ in Fig. 4. For farther distances, the current first flows toward the top metal layers through the stack of vias $(R_{\mathrm{Vertical}})$, is then distributed throughout the die by the low resistance global power network. Subsequently, current flows down to the first metal layer through the stack of vias to reach the switching device. This path is modeled by $R_{\mathrm{Network}}$ in Fig. 4. The value of these resistances are listed in Table IV.

*2) Via-Last TSVs:* As opposed to via-first and via-middle TSVs, via-last TSVs are located at the periphery of each module. As shown in Fig. 2(c), via-last TSVs pass through the metalization layers and the connection with the power network within a plane is achieved at the highest metal layer. Thus, the vertical resistance $R_{\mathrm{Vertical}}$ is part of the TSV resistance. Furthermore, alternative current paths mentioned for via-first and via-middle TSVs do not exist in via-last TSVs since the TSV is not directly connected to the first metal layer. Therefore, for via-last TSVs, the resistance $R_{M1}$ in Fig. 4 is infinitely large. Finally, $R_{\mathrm{Network}}$ represents the equivalent resistance between the switching load and the intersection of TSV and top metal layer. The value of these resistances is also listed in Table IV.

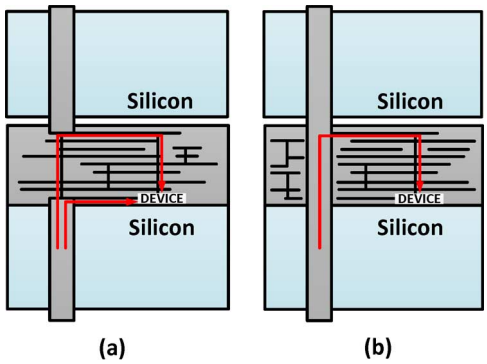


Fig. 8. Current flow from power supply to devices: (a) in via-first and via-middle TSV technologies, alternative current paths exist where the current can reach the devices through the first metal layer, (b) in via-last TSV technology, current flows to the devices only from the top most metal layer.

TABLE IV
POWER DISTRIBUTION NETWORK RESISTANCES WITHIN A PLANE

| Parameter | Via-first | Via-middle | Via-last |
|---|---|---|---|
| Network resistance $R_{Network}$ | 1.97 mΩ | 1.97 mΩ | 8.51 mΩ |
| Vertical resistance $R_{Vertical}$ | 1.97 mΩ | 1.97 mΩ | NA |
| M1 path resistance $R_{M1}$ | 73 $\mu\Omega$ | 73 $\mu\Omega$ | $\infty$ |

TABLE V
POWER PARAMETERS FOR A SINGLE MODULE [14]

| Parameter | DRAM | Processor |
|---|---|---|
| Total power | 3/32 W | 90/32 W |
| Static Power | 0.9/32 W | 27/32 W |
| Dynamic Power | 2.1/32 W | 63/32 W |
| Static Current | 28.125 mA | 843.75 mA |
| Peak Current | 238.125 mA | 7.14 A |
| Operating Frquency | 2.5 GHz | 2.5 GHz |

### E. Switching Circuit

The DRAM consumes 3 W uniformly distributed across the eight stacks [14]. Alternatively, the processor consumes 90 W. 30% of the overall power is due to static power dissipation whereas the remaining portion is due to dynamic power consumption [14]. As illustrated in Fig. 7, a triangular current waveform is assumed with 400 ps period, 100 ps rise time, and 150 ps fall time. The dc current $I_{\rm dc}$ and peak current $I_{\rm peak}$ are determined based on, respectively, the static and dynamic power consumption. The power and switching current characteristics for the DRAM and the processor are listed in Table V. Note that the power and current characteristics in this table represent the 32 Mb DRAM for the memory planes and the corresponding area for the processor plane.

## IV. POWER SUPPLY NOISE ANALYSIS

The simulation results demonstrating distinct power distribution network design requirements for via-first, via-middle, and via-last TSVs are investigated in this section. The approach to determine the design space that satisfies the power supply noise while minimizing the area overhead is described in Section IV-A. Both transient and ac analyses results are discussed, respectively, in Sections IV-B and IV-C. These results have been obtained using HSPICE.

### A. Approach

In 3-D power distribution networks, it is important to determine the appropriate number of TSVs and decoupling capacitance that satisfy the constraint on power supply noise. From this design space, a valid pair that minimizes the physical area overhead is chosen. Note that this specific design point is dependent upon the implementation of the decoupling capacitance. Three methods are considered: 1) metal–oxide-semiconductor (MOS) capacitance in a 32-nm technology node with a capacitance density of 39.35 fF/$\mu$m$^2$ as determined from the equivalent oxide thickness (EOT) of the technology [36], 2) deep trench capacitance with two different densities: 140 fF/$\mu$m$^2$ and 280 fF/$\mu$m$^2$ [43], and metal–insulator–metal (MIM) capacitance with a density of 8 fF/$\mu$m$^2$ [44], [45].

The effect of the number of TSVs and decoupling capacitance on power supply noise is analyzed in both time and frequency domains, as described in the following subsections. Note that in the rest of the paper, number of TSVs refers to the number of power TSVs within a single module. The decoupling capacitance refers to the overall capacitance in each DRAM module. The area overhead is determined as a percentage of the area of a single module ($1500 \times 2500$ $\mu$m$^2$). Similarly, the power loss is determined as a percentage of the power consumption of a single module (93/32 W).

### B. Transient Analysis

The dependence of peak noise on decoupling capacitance and number of TSVs, design space that satisfies the target power supply noise, and the area overhead due to TSVs and decoupling capacitance are provided. Note that the sensitivity of peak noise on number of TSVs and decoupling capacitance varies depending upon the specific design point, as described in this section. Also note that the power supply noise is observed across the current source located at the processor plane which is the farthest node from the power supply pads. In transient analysis, the tolerable power supply noise is assumed to be 100 mV, 10% of the power supply voltage.

*1) Via-Fist TSV:* The peak noise surface as a function of decoupling capacitance and number of TSVs is plotted in Fig. 9(a) for via-first TSVs. Since the TSV resistance is significantly higher in via-first technology, the power distribution network is overdamped, producing a monotonic response. Thus, peak noise decreases as the number of TSVs and decoupling capacitance increase. To determine the valid design space, a contour at 100 mV peak noise is extracted from the noise surface, as depicted in Fig. 9(b). Any point above the curve satisfies the noise constraint whereas the shaded region should be avoided.

According to Fig. 9(b), multiple pairs of number of TSVs and decoupling capacitance exist that satisfy the target supply noise. Thus, a valid pair that minimizes the overall area overhead can be chosen. As mentioned previously, this design point that minimizes the area overhead depends upon the implementation of the decoupling capacitance. For both MOS and MIM decoupling capacitances, the area overhead is depicted in Fig. 10 for each point on the contour of Fig. 9(b). Note that, deep trench capacitance is not considered in via-first technology since the substrate is thinned to approximately 10 $\mu$m.

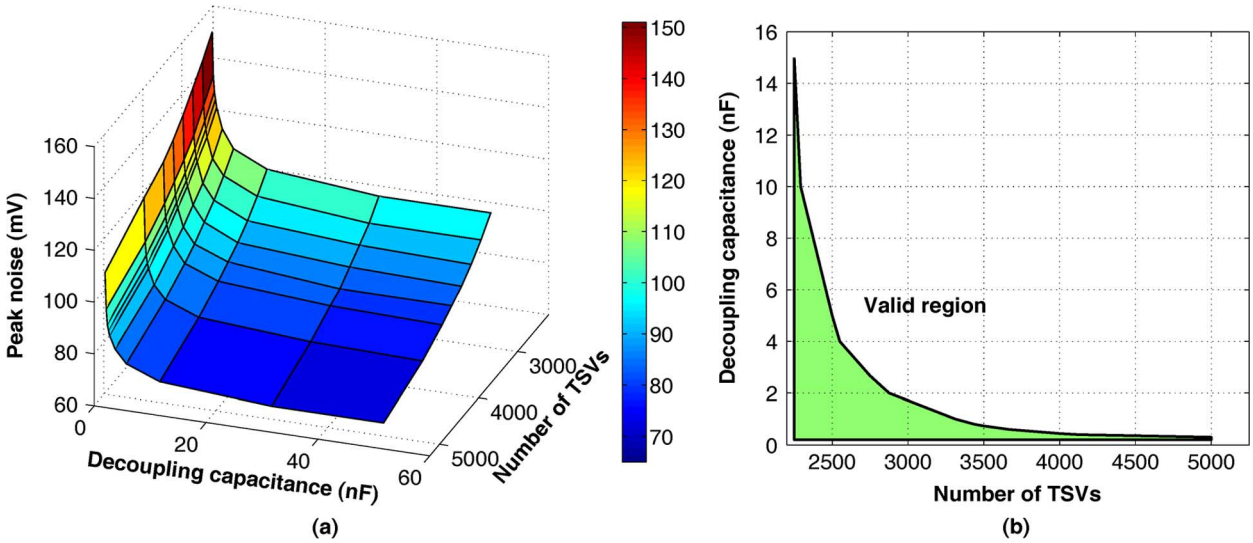


Fig. 9. Peak noise characteristics as a function of number of TSVs and decoupling capacitance in via-first TSV technology: (a) surface plot and (b) contour plot at 100 mV.

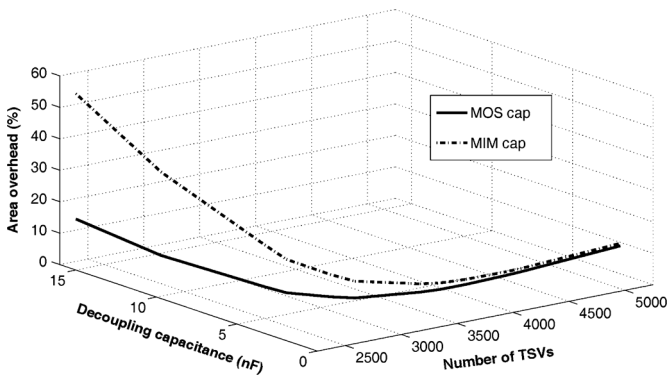


Fig. 10. Area overhead in via-first technology. Note that each point on the curve satisfies the target power supply noise.

As demonstrated in this figure, a specific design point exists that minimizes the area overhead. If an MOS capacitance is used, this design point corresponds to 2750 TSVs and 2.7 nF of decoupling capacitance, producing an area overhead of approximately 9%. Alternatively, with MIM capacitance, this design point is at 3437 TSVs and 0.8 nF of decoupling capacitance, producing an area overhead of 11.83%. Note that if an arbitrary pair is chosen from the contour in Fig. 9(b), the area overhead can be as high as 16% for MOS capacitance and 56% for MIM capacitance.

According to the transient noise results, an important design requirement for via-first technology is to have a significantly large number of TSVs to reduce current per TSV. This requirement increases the physical area overhead. Note however that 6.25 times more via-first TSVs than via-last TSVs can be placed within a constant area due to smaller dimensions of the via-first TSV. Also note that sufficient decoupling capacitance is required to reduce transient $IR$ noise.

An advantage of a via-first based power distribution network is the high damping factor due to high TSV resistance and small TSV inductance. Thus, decoupling capacitance effectively suppresses the transient noise, producing a low peak-to-peak noise, as listed in Table VI. Note however that the power loss is relatively high in via-first based power distribution network due to high TSV resistance, also listed in Table VI.

*2) Via-Middle TSV:* The peak noise surface as a function of decoupling capacitance and number of TSVs is plotted in Fig. 11(a) for via-middle TSVs. The noise contour at 100 mV is illustrated in Fig. 11(b).

Similar to a via-first based power network, the power supply noise monotonically decreases as the number of TSVs and decoupling capacitance increase. Note that the required number of TSVs is lower than via-first TSVs since the TSV resistance is relatively lower due to higher conductivity tungsten as opposed to doped polysilicon. Also note that since via-middle technology exhibits a greater substrate thickness, deep trench capacitance is considered. The area overhead is depicted in Fig. 12 for four different decoupling capacitance densities, as mentioned in Section IV-A.

Similar to a via-first technology, a specific design point exists where the physical area overhead is minimized. If MOS capacitance is used, this design point is at 620 TSVs and 0.6 nF of decoupling capacitance. If however a deep trench capacitance is utilized, this optimum design point shifts to the left. In a specific small portion of the curve, the area overhead is relatively insensitive to decoupling capacitance and number of TSVs. Thus, two design points that minimize area overhead are determined for a low density deep trench capacitance, as listed in Table VI. Finally, if MIM capacitance is utilized, the minimum area overhead corresponds to 631 TSVs and 0.4 nF of decoupling capacitance. Note that the area overhead in via-middle technology is considerably lower than via-first technology due to a fewer number of required TSVs.

An important difference between via-first and via-middle TSVs is the inductive characteristics. Via-middle TSVs exhibit higher inductance due to a greater TSV depth. Since the TSV

TABLE VI
VALID DESIGN POINTS THAT SATISFY THE PEAK POWER SUPPLY NOISE WHILE MINIMIZING THE AREA OVERHEAD FOR EACH TSV TECHNOLOGY

| VIA-FIRST | | | | | | |
|---|---|---|---|---|---|---|
| Capacitance type | Capacitance Density (fF/$\mu m^2$) | Area overhead | Number of TSVs | Decoupling capacitance (nF) | Power loss | Peak-to-peak noise (mV) |
| Metal-oxide-semiconductor | 39.35 | 9.06% | 2750 | 2.7 | 8.3% | 33.42 |
| Metal-insulator-metal | 8 | 11.83% | 3437 | 0.8 | 7.3% | 23.5 |
| VIA-MIDDLE | | | | | | |
| Capacitance type | Capacitance Density (fF/$\mu m^2$) | Area penalty | Number of TSVs | Decoupling capacitance (nF) | Power loss | Peak-to-peak noise (mV) |
| Metal-oxide-semiconductor | 39.35 | 1.96% | 620 | 0.60 | 6.7% | 63.56 |
| Low density deep trench | 140 | 1.68% | 421 | 4 | 8.2% | 31.33 |
| Low density deep trench | 140 | 1.68% | 484 | 2 | 7.6% | 45.13 |
| High density deep trench | 280 | 1.49% | 421 | 4 | 8.2% | 31.33 |
| Metal-insulator-metal | 8 | 3.01% | 631 | 0.4 | 6.6% | 67.5 |
| VIA-LAST | | | | | | |
| Capacitance type | Capacitance Density (fF/$\mu m^2$) | Area penalty | Number of TSVs | Decoupling capacitance (nF) | Power loss | Peak-to-peak noise (mV) |
| Metal-oxide-semiconductor | 39.35 | 1.54% | 76 | 0.385 | 4% | 134.72 |
| Low density deep trench | 140 | 1.21% | 30 | 3.74 | 4.9% | 134.67 |
| High density deep trench | 280 | 0.86% | 30 | 3.74 | 4.9% | 134.67 |
| Metal-insulator-metal | 8 | 2.56% | 76 | 0.385 | 4% | 134.72 |

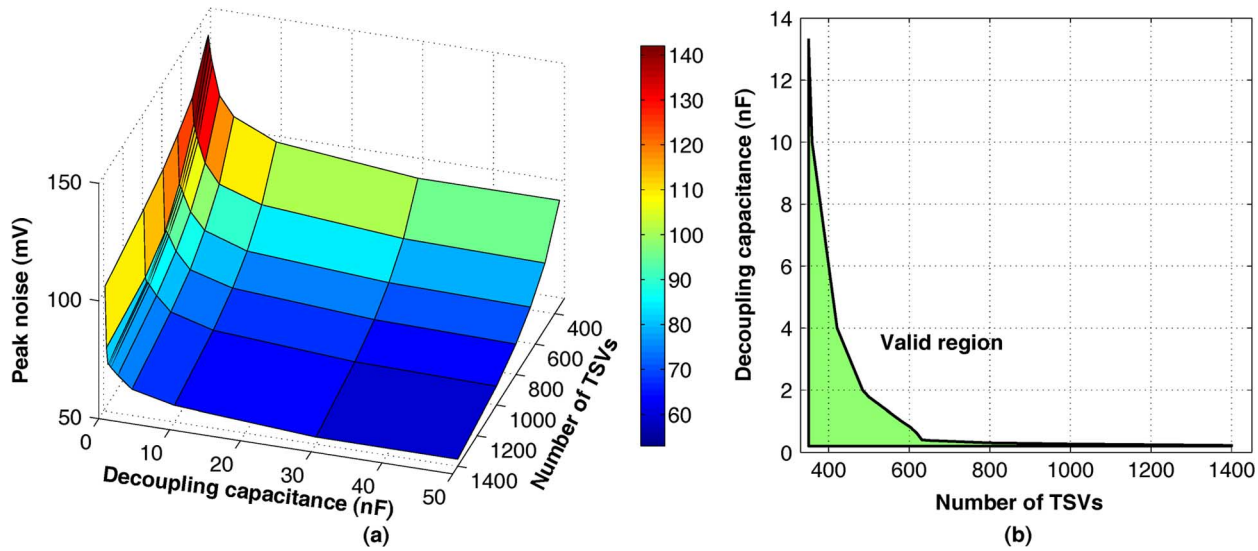


Fig. 11. Peak noise characteristics as a function of number of TSVs and decoupling capacitance in via-middle TSV technology: (a) surface plot and (b) contour plot at 100 mV.

resistance is significantly lower than via-first TSVs, the amount of decoupling capacitance plays an important role in the damping factor and peak-to-peak noise. As listed in Table VI, the peak-to-peak noise in via-middle based power network is approximately twice the peak-to-peak noise in via-first based power network if the decoupling capacitance is low (such as the minimum area design point obtained with MOS-C or MIM-C). Alternatively, for the remaining design points where a deep trench capacitance is used, the peak-to-peak noise is lowered due to a larger decoupling capacitance.

*3) Via-Last TSV:* Via-last technology exhibits significantly different noise characteristics as compared to via-first and via-middle technologies. Since copper is used as the filling material, the resistance of via-last TSVs is significantly lower. Alternatively, the TSV inductance is higher than via-first TSVs and comparable to via-middle TSVs. Due to significantly lower resistance and a relatively large inductance, a power distribution network with via-last TSVs is typically underdamped.

The peak noise surface as a function of decoupling capacitance and number of TSVs is plotted in Fig. 13(a). As opposed to via-first and via-middle TSVs, the noise surface is nonmonotonic with multiple peaks where the noise exceeds the design objective. At specific combinations of the number of TSVs and decoupling capacitance, the power supply noise significantly increases due to the resonant behavior. The noise contour at 100 mV is illustrated in Fig. 13(b) to determine the valid design space where the peak noise constraint is satisfied. The unshaded region represents a valid combination of the number of TSVs and decoupling capacitance. As illustrated in this figure, at a specific decoupling capacitance, an increase in the number

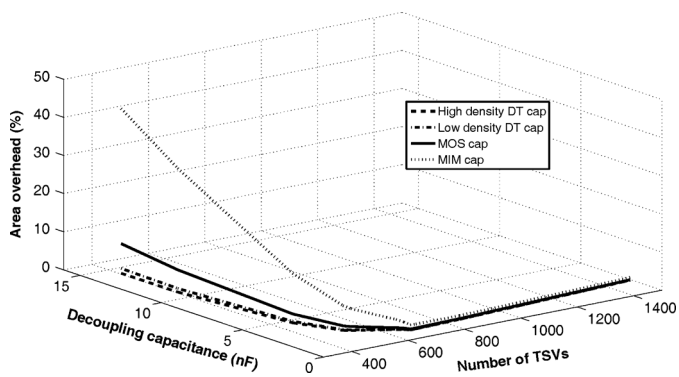


Fig. 12. Area overhead in via-middle technology. Note that each point on the curve satisfies the target power supply noise.

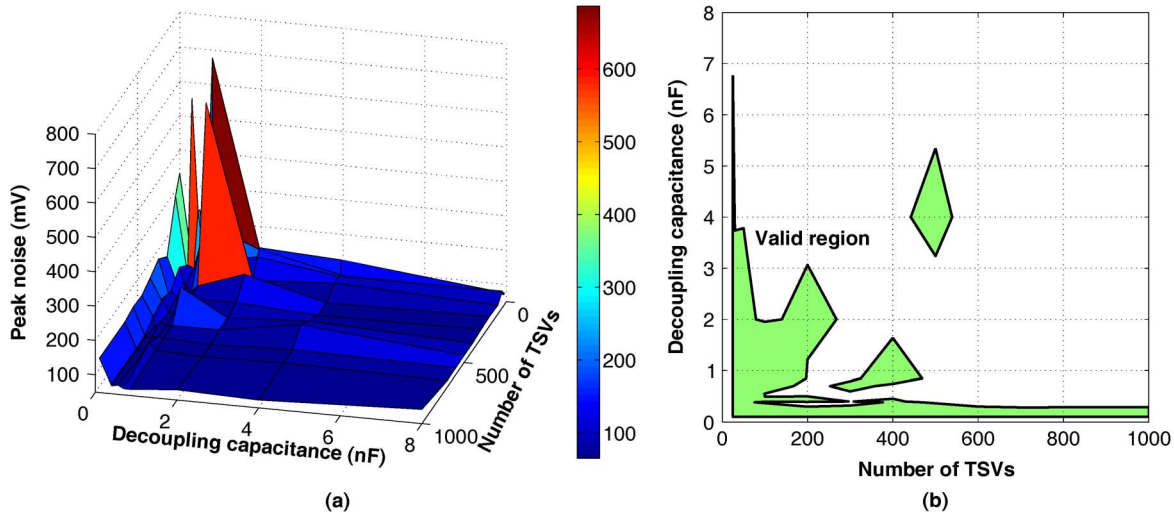


Fig. 13. Peak noise characteristics as a function of number of TSVs and decoupling capacitance in via-last TSV technology: (a) surface plot and (b) contour plot at 100 mV.

of TSVs can violate the noise constraint due to a lower damping factor. In this case, the decoupling capacitance should be increased. Thus, in via-last technology, the power supply noise is highly sensitive to the number of TSVs and decoupling capacitance, particularly at relatively low decoupling capacitances. Furthermore, peak-to-peak noise is also significantly higher, as listed in Table VI. The area overhead, however, is the lowest in via-last TSVs since the number of required TSVs is significantly smaller. The power loss is also low due to small TSV resistance. Note that the dependence of area overhead on number of TSVs and decoupling capacitance is not graphically illustrated for via-last TSVs since this relationship is highly complicated due to the nonmonotonic behavior of the power supply noise. However, the design points that correspond to the minimum area overhead while satisfying the power supply noise are determined and listed in Table VI for MOS, deep trench, and MIM capacitances.

### C. AC Analysis Results

As described in the previous section, the peak noise is reduced by either increasing the number of TSVs or decoupling capacitance for both via-first and via-middle TSVs. Alternatively, for via-last TSVs, the noise exhibits a nonmonotonic relationship with these design parameters. A larger decoupling capacitance increases the damping factor, thereby reducing the peak-to-peak noise. Alternatively, the resonant frequency is shifted to lower frequencies as the decoupling capacitance increases. Thus, input independent ac analysis is useful to better understand the impedance characteristics of 3-D power distribution networks with different TSV technologies. Specifically, the impedance characteristics are investigated at the design points listed in Table VI. Note that at these design points, the power distribution network satisfies the peak noise in time domain and the area overhead is minimized, as described in the previous section. Since a separate set of design points exists depending upon the capacitance density, the impedance characteristics for both MOS capacitance and high density deep trench capacitance are investigated, as illustrated, respectively, in Fig. 14(a) and (b).

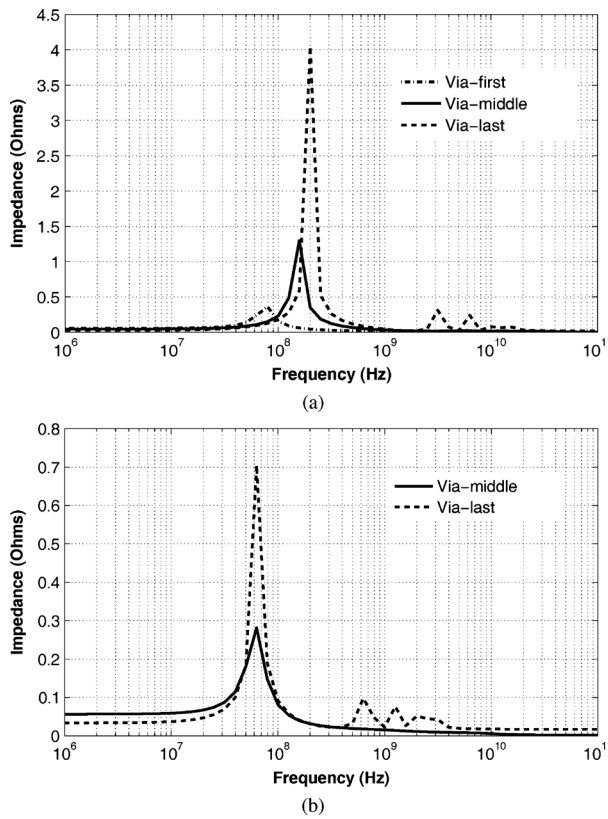


Fig. 14. Impedance characteristics at the design points listed in Table VI. Note that at these design points, the peak noise constraint is satisfied in time domain and area overhead is minimized. Decoupling capacitance is implemented as (a) MOS capacitance and (b) high density deep trench capacitance.

According to these figures, a via-last based power network exhibits lower impedance at relatively low frequencies. Resonance, however, is a critical issue due to a low damping factor. If an MOS capacitance is used as the decoupling capacitance, as depicted in Fig. 14(a), the minimum area is achieved at

a relatively low decoupling capacitance and large number of TSVs (smaller equivalent TSV resistance). In this case, the impedance at the resonant frequency reaches 4 Ω. For a via-middle based power network, the peak impedance is smaller than 1.5 Ω. Alternatively, for a via-first based power network, the peak impedance is smaller than 0.5 Ω since high TSV resistance provides sufficient damping. Note that in a time domain analysis, the frequency is determined primarily by the rise time of the switching load current. In a practical circuit, however, target impedance should be satisfied for a wide range of frequencies since the on-chip rise time varies [46]. In Fig. 14(b), the decoupling capacitance is implemented as a deep trench capacitance. Thus, the minimum area design point is achieved at a relatively high decoupling capacitance and small number of TSVs. The damping factor is therefore higher and the impedance at the resonant frequency is reduced to 0.7 Ω for a via-last based power network and to 0.3 Ω for a via-middle based power network. It is therefore desirable to increase the amount of decoupling capacitance to avoid resonance despite the increase in the area overhead. Also note that despite this reduction in the peak impedance, the resonant frequency is shifted to a lower frequency as the decoupling capacitance is increased. There is therefore a greater possibility for the operating frequency to coincide with the resonant frequency. Thus, in this case, the peak impedance should be sufficiently low. Note that via-first technology is not included in Fig. 14(b) since deep trench capacitance is difficult to implement due to a low substrate thickness.

## V. Design Implications

According to the results described in the previous section, the valid design space (where the power supply noise is satisfied) is significantly different for each TSV technology. The number of TSVs is an important design parameter that affects both the equivalent resistance and the quality factor of the network. Number of TSVs should be sufficiently large to reduce both static and transient $IR$ drop. Alternatively, the number of TSVs should not be excessively large since the quality factor is increased, thereby reducing the damping factor. A low damping factor increases the peak-to-peak noise due to oscillations.

A via-first based 3-D power network requires a large number of TSVs due to high resistivity doped polysilicon. Thus, the area overhead and power loss are relatively higher. Alternatively, a power network with via-last TSVs exhibits smaller area overhead and power loss. A significant issue, however, exists in a via-last based 3-D power network. Due to low resistive and relatively more inductive TSVs, a power network with via-last TSVs is typically underdamped, exacerbating the issue of resonance. As depicted in Fig. 13(b), a slight change in the number of TSVs or decoupling capacitance can cause the power network to fall within the invalid region where the noise constraint is violated. To reduce this sensitivity, a larger decoupling capacitance can be placed. In this case, however, the resonant frequency shifts to a lower frequency, at which the peak impedance should be smaller than the target impedance.

Considering the aforementioned constraints, via-middle TSVs filled with tungsten are relatively more advantageous for power delivery. This characteristic is due to four reasons: 1) higher conductivity than via-first TSVs, 2) higher damping factor (and, therefore, lower sensitivity to decoupling capacitance and number of TSVs) than via-last TSVs, 3) smaller area (per TSV) than via-last TSVs, and 4) less routing congestion.

## VI. Conclusion

Three different TSV technologies, via-first, via-middle, and via-last, have been evaluated to distribute power in a 32-nm 3-D system with eight memory planes and one processor plane. An electrical model has been developed that consists of power/ground TSVs, power distribution network within each plane, substrate, and the switching circuit. Different design requirements have been identified for each TSV technology. A valid design space that satisfies the power supply noise while minimizing the physical area has been determined. It has been demonstrated that highly resistive via-first TSVs can be used to deliver power at the expense of approximately 9% area overhead as compared to less than 2% area overhead in via-middle and via-last technologies. Despite this higher area requirement, a power distribution network with via-first TSVs is typically overdamped and the issue of resonance is alleviated. Alternatively, for via-middle and via-last TSV technologies, the impedance at the resonant frequency should be sufficiently small. This issue is exacerbated for a via-last based power distribution network since the TSV resistance is significantly lower, and therefore the network is typically underdamped. Furthermore, the peak noise exhibits high sensitivity to number of TSVs and decoupling capacitance. Thus, these design parameters should be carefully chosen in a via-last based 3-D power distribution network.

## References


[1] E. Salman and E. G. Friedman, *High Performance Integrated Circuit Design*. New York: McGraw-Hill, 2012.

[2] V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*. Burlington, MA: Morgan Kaufmann, 2009.

[3] T. Zhang *et al.*, "3-D data storage, power delivery, and RF/optical transceiver-case studies of 3-D integration from system design perspectives," *Proc. IEEE*, vol. 97, no. 1, pp. 161–174, Jan. 2009.

[4] J. Q. Lu, "3-D hyperintegration and packaging technologies for micro-nano systems," *Proc. IEEE*, vol. 97, no. 1, pp. 18–30, Jan. 2009.

[5] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.

[6] A. W. Topol *et al.*, "Three-dimensional integrated circuits," *IBM J. Res. Develop.*, vol. 50, no. 4/5, pp. 491–506, Jul./Sep. 2006.

[7] J. A. Burns *et al.*, "A wafer-scale 3-D circuit integration technology," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2507–2516, Oct. 2006.

[8] E. Salman, M. H. Asgari, and M. Stanacevic, "Signal integrity analysis of a 2-D and 3-D integrated potentiostat for neurotransmitter sensing," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, Nov. 2011, pp. 17–20.

[9] M. S. Bakir and J. E. Meindl, *Integrated Interconnect Technologies for 3-D Nanoelectronic Systems*. Boston, MA: Artech, 2008.

[10] W. A. Wulf and S. A. McKee, "Hitting the memory wall: Implications of the obvious," *ACM SIGARCH Comput. Archit. News*, vol. 23, no. 1, pp. 20–24, Mar. 1995.

[11] P. Jacob *et al.*, "Mitigating memory wall effects in high-clock-rate and multicore CMOS 3-D processor memory stacks," *Proc. IEEE*, vol. 97, no. 1, pp. 108–122, Jan. 2009.

[12] S. Borkar, "3-D integration for energy efficient system design," in *Proc. IEEE/ACM Design Automat. Conf.*, Jun. 2011, pp. 214–219.

[13] ITRS Technology Working Groups, "International technology roadmap for semiconductors (ITRS)," 2011.

[14] Q. Wu and T. Zhang, "Design techniques to facilitate processor power delivery in 3-D processor-DRAM integrated systems," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 19, no. 9, pp. 1655–1666, Sep. 2011.
[15] N. H. Khan, S. M. Alam, and S. Hassoun, "Power delivery design for 3-D ICs using different through-silicon via (TSV) technologies," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 19, no. 4, pp. 647–658, Apr. 2011.
[16] G. Huang, M. Bakir, A. Naeemi, H. Chen, and J. D. Meindl, "Power delivery for 3-D chip stacks: Physical modeling and design implication," *Proc. IEEE Electrical Performance Electron. Packag.*, pp. 205–208, Oct. 2007.
[17] V. F. Pavlidis and G. De Micheli, "Power distribution paths in 3-D ICs," in *Proc. ACM/IEEE Great Lakes Symp. VLSI*, May 2009, pp. 263–268.
[18] A. Agarwal, R. B. Murthy, V. Lee, and G. Viswanadam, "Polysilicon interconnections (FEOL): Fabrication and characterization," in *Proc. IEEE Electron. Packag. Technol. Conf.*, Dec. 2009, pp. 317–320.
[19] D. Henry *et al.*, "Via first technology development based on high aspect ratio trenches filled with doped polysilicon," in *Proc. IEEE Electron. Compon. Technol. Conf.*, May/Jun. 2007, pp. 830–835.
[20] G. Pares *et al.*, "Mid-process through silicon vias technology using tungsten metallization: Process optimization and electrical results," in *Proc. IEEE Electron. Packag. Technol. Conf.*, Dec. 2009, pp. 772–777.
[21] G. Pares *et al.*, "Through silicon via technology using tungsten metallization," in *Proc. IEEE Int. Conf. IC Design Technol.*, May 2011, pp. 1–4.
[22] T. Dao *et al.*, "Thermo-mechanical stress characterization of tungsten-fill through-silicon-via," in *Proc. IEEE Int. Symp. VLSI Design Automat. Test*, Apr. 2010, pp. 7–10.
[23] J. U. Knickerbocker *et al.*, "Three-dimensional silicon integration," *IBM J. Res. Develop.*, vol. 52, no. 6, pp. 553–569, Nov. 2008.
[24] A. C. Hsieh and T. T. Hwang, "TSV redundancy: Architecture and design issues in 3-D IC," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 20, no. 4, pp. 711–722, Apr. 2012.
[25] C. Laviron *et al.*, "Via first approach optimisation for through silicon via applications," in *Proc. IEEE Electron. Compon. Technol. Conf.*, May 2009, pp. 14–19.
[26] M. Kawano *et al.*, "A 3-D packaging technology for 4 Gbit stacked DRAM with 3 Gbps data transfer," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2006, pp. 1–4.
[27] M. Kawano *et al.*, "Three-dimensional packaging technology for stacked DRAM with 3-Gb/s data transfer," *IEEE Trans. Eletron Devices*, vol. 55, no. 7, pp. 1614–1620, Jul. 2008.
[28] M. Puech *et al.*, "DRIE achievements for TSV covering via first and via last strategies," in *Proc. Adv. Technol. Workshop 3-D Packag.*, Mar. 2008.
[29] S. Ramaswamy *et al.*, "Process integration considerations for 300 mm TSV manufacturing," *IEEE Trans. Device Mater. Reliabil.*, vol. 9, no. 4, pp. 524–528, Dec. 2009.
[30] D. H. Kim, S. Mukhopadhyay, and S. K. Lim, "Through-silicon-via aware interconnect prediction and optimization for 3-D stacked ICs," in *Proc. Int. Workshop Syst. Level Interconnect Predict.*, Sep. 2009, pp. 85–92.
[31] N. Kumar *et al.*, "Robust TSV via-middle and via-reveal process integration accomplished through characterization and management of sources of variation," in *Proc. IEEE Electronic Compon. Technol. Conf.*, May–Jun. 2012, pp. 787–793.
[32] J. W. Elam *et al.*, "Surface chemistry and film growth during TiN atomic layer deposition using TDMAT and $NH_3$," *Thin Solid Films*, vol. 436, no. 2, pp. 145–156, Jul. 2003.
[33] H. Kikuchi *et al.*, "Tungsten through-silicon via technology for three-dimensional LSIs," *Jpn. J. Appl. Phys.*, vol. 47, no. 4, pp. 2801–2806, Apr. 2008.
[34] S. Arakalgud, "3-D TSV interconnect program—An overview," presented at the SEMATECH Symp., Goyang, Korea, Oct. 2010.
[35] H. Sun *et al.*, "3-D DRAM design and application to 3-D multicore systems," *IEEE Design Test Comput.*, vol. 26, no. 5, pp. 36–47, Sep. –Oct. 2009.
[36] S. Natarajan *et al.*, "A 32 nm logic technology featuring 2nd-Generation high-k+ metal-gate transistors, enhanced channel strain and 0.171 $\mu m^2$ SRAM cell size in a 291 Mb array," in *Proc. IEEE Int. Electron Devices Meet.*, Dec. 2008, pp. 1–3.
[37] R. Tatikola, M. Chowdhury, R. Chen, and J. Zhao, "Simulation study of power delivery performance on flip-chip substrate technologies," in *Proc. IEEE Electron. Compon. Technol. Conf.*, Jun. 2004, pp. 1862–1865.
[38] I. Savidis and E. G. Friedman, "Closed-form expressions of 3-D via resistance, inductance, and capacitance," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1873–1881, Sep. 2009.
[39] J. Kim, J. Cho, and J. Kim, "TSV modeling and noise coupling in 3-D IC," in *Proc. IEEE Electron. System-Integrat. Technol. Conf.*, Sep. 2006, pp. 1–6.
[40] G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, "Electrical modeling and characterization of through silicon via for three-dimensional ICs," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 256–262, Jan. 2010.
[41] J. S. Pak *et al.*, "PDN impedance modeling and analysis of 3-D TSV IC by using proposed P/G TSV array model based on separated P/G TSV and chip-PDN models," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 1, no. 2, pp. 208–219, Feb. 2011.
[42] NCSU 45 nm Process Design Kit [Online]. Available: http://www.eda.ncsu.edu/wiki/FreePDK45:Metal_Layers
[43] B. Dang *et al.*, "3-D chip stack with integrated decoupling capacitors," in *Proc. IEEE Int. Electron. Compon. Technol. Conf.* , Jun. 2009, pp. 1–5.
[44] P. Zhou, K. Sridharan, and S. S. Sapatnekar, "Optimizing decoupling capacitors in 3-D circuits for power grid integrity," *IEEE Design Test Comput.*, vol. 26, no. 5, pp. 15–25, Sep. 2009.
[45] P. Zhou, K. Sridharan, and S. S. Sapatnekar, "Congestion-aware power grid optimization for 3-D circuits using MIM and CMOS decoupling capacitors," in *Proc. ACM/IEEE Asia South Pacific Design Automation Conf.*, 2009, pp. 179–184.
[46] E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Worst case power/ground noise estimation using an equivalent transition time for resonance," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 997–1004, May 2009.

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