Signal Integrity Analysis of a 2-D and 3-D Integrated Potentiostat for Neurotransmitter Sensing

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***Abstract*—3-D integration technology offers significant advantages in implantable devices by reducing the form factor and power dissipation. Signal integrity characteristics of a 2-D and 3-D integrated potentiostat for neurotransmitter sensing are investigated and compared. The potentiostat is implemented as current integrating switched-capacitor first-order single-bit delta-sigma modulator. An electrical model is developed for the substrate, power network, and through silicon vias (TSVs). These models are combined with the neurotransmitter sensing circuit to generate an entire model to analyze signal integrity. Contrary to the conventional assumption, a 3-D integrated hybrid system does not necessarily exhibit enhanced noise isolation despite the advantage of having separate planes, as demonstrated in this paper. Noise coupling into the substrate due to TSVs is shown to be a significant mechanism that degrades signal integrity in 3-D integrated implantable systems.**

I. INTRODUCTION

A multichannel potentiostat, integrated with microfabricated sensor array, is used for distributed simultaneous monitoring of neurochemical activity [1]. A potentiostat measures the redox current proportional to the concentration of the certain species of electroactive neurotransmitters, while keeping the potential of the sensor electrode at specific redox potential [2]. The detection of the neurotransmitters is critical for neural pathways and the etiology of neurological diseases like epilepsy and stroke [3]. The main challenges in the design of a potentiostat are high sensitivity and wide dynamic range of the measured currents. Furthermore, implantation of the device in the human body places stringent constraints on the power consumption and size.

In the past decade, three-dimensional (3-D) integration has emerged as a promising technology to achieve higher integration density and reduce the global interconnect length (therefore power dissipation) in high performance computing applications [4]. As opposed to the conventional practice, the advantages and limitations of 3-D technology in developing an implantable device are investigated with an emphasis on signal integrity. Since the aggressor and victim blocks can be placed on separate planes, the noise performance of a 3-D system is typically assumed to be superior than a 2-D system [4], [5]. The primary purpose of this study is to evaluate the validity of this assumption by developing a comprehensive electrical model for both a 2-D and 3-D integrated potentiostat and better understand noise coupling characteristics in 3-D integrated hybrid systems.

Advantages of 3-D technology in implantable devices are described in Section II. A case study is presented in Section III where the proposed models to analyze noise characteristics are introduced. Switching noise that couples to a victim device is also evaluated and compared for both 2-D and 3-D technologies under different conditions. The results are briefly discussed in Section IV. Finally, the paper is concluded in Section V.

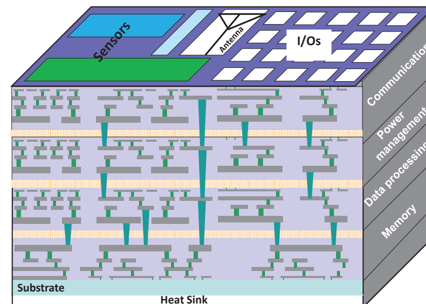

Fig. 1. **Monolithic 3-D integration technology where through silicon vias (TSVs) are utilized to achieve communication among the planes [4].**

II. 3-D INTEGRATED IMPLANTABLE DEVICES

3-D technology offers a unique capability to *merge* diverse devices, technologies, and circuit functionalities within a monolithic system. An illustrative example of such a system is shown in Fig. 1, where disparate planes such as sensors, circuit blocks for communication, power management, and data processing are stacked within a monolithic die [4]. Communication among the planes is achieved by vertical *through silicon vias* (TSVs). This hybrid integration capability is highly advantageous for applications in life sciences since each plane can be individually optimized based on the required function and design objectives. For example, the communication plane is designed with physical parameters that enhance the realization of on-chip passive devices, a primary limitation for implantable devices. Furthermore, the overall area of the system is reduced, achieving a smaller form factor.

A 3-D integrated implantable device suffers from significant noise coupling due to dense integration and TSV characteristics, as demonstrated in this paper. Noise management therefore emerges as a one of the significant limitations in highly heterogeneous 3-D integrated implantable devices. Several noise coupling mechanisms exist in a 3-D system, degrading the performance of frontend circuits [6]. For the neurotransmitter sensing application discussed here, the current magnitude ranges from picoamperes to microamperes, making this signal highly sensitive to switching noise [1].

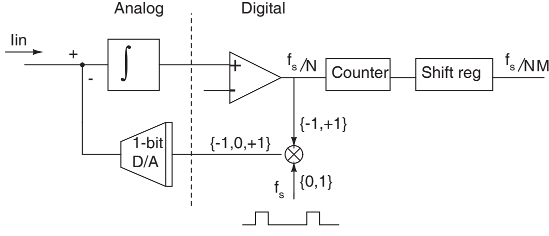

Fig. 2. **System level diagram of a single channel of the potentiostat.**

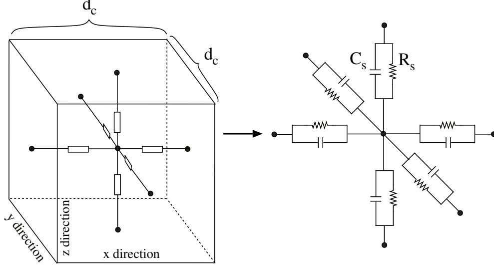

Fig. 3. **Discrete model of a substrate where each cuboid is represented by six resistances and capacitances.**

III. CASE STUDY

The 2-D 16-channel VLSI potentiostat chip, designed and fabricated in 0.5 μm CMOS technology, simultaneously records neurotransmitter levels from multiple neurons [1], [7]. To manage computational complexity, the proposed signal integrity analysis focuses on a single channel that consists of a first order delta-sigma modulator, counter for decimation, and shift register, as depicted in Fig. 2 [1], [7]. Delta-sigma modulator consists of a current integrator, comparator, and switched-current 1-bit D/A converter in the feedback loop.

The counter is the primary aggressor whereas the sense amplifier within the current integrator is identified as one of the primary victim blocks. The switching noise that couples from the counter to the sense amplifier is analyzed for different scenarios. 3-D electrical models used to describe these scenarios are described in Section III-A. Results of the signal integrity analysis are presented in Section III-B.

A. 3-D Electrical Models

The model to analyze switching noise coupling consists of two primary items: (1) monolithic substrate and (2) TSVs.

1) Substrate Model: The substrate corresponding to a single channel of the sensing chip is discretized in three dimensions where each cuboid is modeled using *RC* impedances, as depicted in Fig. 3 [8]. According to this figure, substrate resistance R_s and capacitance C_s are, respectively,

$$R_s = \frac{1}{2}\frac{\rho_s}{d_c} \qquad C_s = \varepsilon_s 2 d_c, \tag{1}$$

where ρ_s is the substrate resistivity and ε_s is the dielectric permittivity of silicon. The sufficient accuracy of this model has been previously demonstrated [8]. In this study, a bulk type substrate with ρ_s=10 Ωcm is assumed. Note that each dimension of the unit cuboid d_c is 9 μm. To model the overall substrate of a single channel, a total of 90, 16, and 3 cuboids are required, respectively, in the *x*, *y*, and *z* directions.

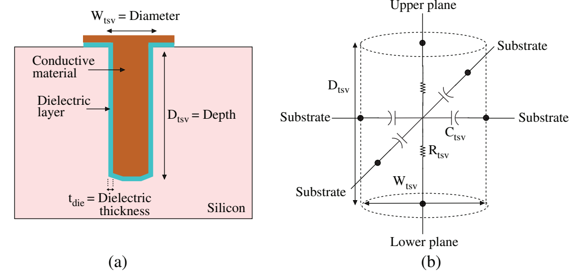

Fig. 4. **TSV representations: (a) Cross section of a TSV consisting of a conductive material and a dielectric layer, (b) electrical model of a TSV.**

2) TSV Model: As depicted in Fig. 4(a), a typical TSV is represented as a cylinder with a diameter W_{tsv} and depth D_{tsv} and consists of two parts: (1) conductive material such as copper or tungsten, (2) a dielectric layer that surrounds the conductive material. The thickness of this dielectric layer t_{die} is in the range of 0.2 μm to 1 μm [9]. In this analysis, t_{die} is assumed to be 0.2 μm.

These parameters vary depending upon the specific fabrication technology [4]. For typical 3-D technologies, the diameter of a TSV is in the range of 5 μm to 10 μm whereas the depth varies from 25 μm to several hundred μm [9]. Note that the TSV depth is primarily determined by the wafer thinning capability of the TSV fabrication process. In this analysis, a TSV depth of 27 μm is assumed.

An electrical model for the TSV is shown in Fig. 4(b) where the TSV is represented by an *L* shaped, 2-stage distributed *RC* circuit [10]. Note that the resistance represents the conductive material whereas the capacitance models the dielectric layer. TSV resistance R_{tsv} and capacitance C_{tsv} are, respectively [11],

$$R_{tsv} = \frac{1}{2}\frac{\rho_c D_{tsv}}{\pi (W_{tsv})^2} \qquad C_{tsv} = \frac{1}{2}\frac{\pi \varepsilon_{sio2} D_{tsv}}{\ln[\frac{(w/2)+t_{die}}{w/2}]}, \tag{2}$$

where ρ_c is the copper resistivity and ε_{sio2} is the dielectric permittivity of silicon dioxide. Note that C_{tsv} is based on a cylindrical capacitor formula. Sufficient accuracy of this model has been previously demonstrated by comparing the results with a 3-D field solver [11].

B. Signal Integrity Analysis

Both the substrate and TSV models described in the previous section are utilized in this section to generate an entire electrical model for a single channel of a neurotransmitter chip in both 2-D and 3-D technologies. These models are used to analyze signal integrity in both cases, as described in the following subsections.

1) 2-D Potentiostat: The bulk nodes of the transistors (in the circuit schematic view) located within an area of 81 μm^2 are lumped together and connected to the corresponding node on the substrate model, as depicted in Fig. 5. The physical layout of the circuit is utilized to determine the approximate location of the blocks with respect to the substrate. Note that those nodes of the substrate that are connected to a substrate contact (tap) including guard rings are biased with the ground

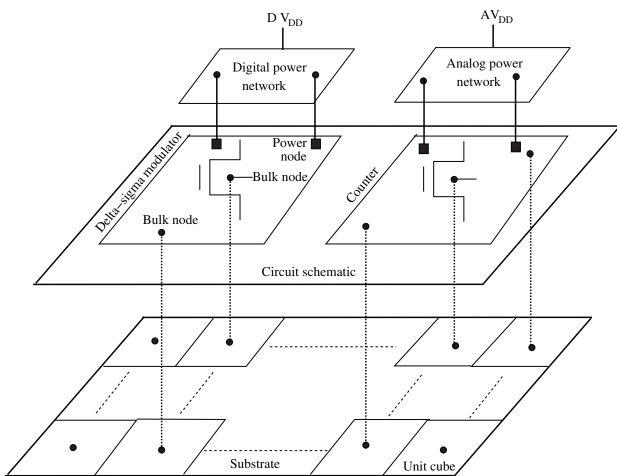

Fig. 5. **Conceptual representation of the overall model to analyze signal integrity in a 2-D potentiostat.**

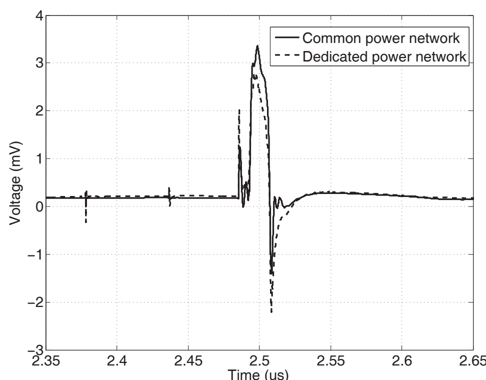

Fig. 6. **Transient analysis results illustrating peak noise at the bulk node of a victim device for two different cases in a 2-D potentiostat.**

voltage in order not to obtain overly pessimistic results. Also note that a lumped resistance of two ohms and a lumped inductance of one henry is used to model the parasitic effects of both on-chip and package power distribution networks. Thus, an entire electrical model considering the substrate and nonideal power network is generated by connecting the bulk nodes in the circuit schematic to the corresponding nodes on the substrate model.

The overall model is analyzed in 0.5 μm CMOS technology using Spectre. The noise at the bulk node of a victim device within the delta-sigma modulator is observed for two different cases: when the digital and analog parts of the circuit (1) share a common power network, (2) have dedicated on-chip power networks. Results of a transient analysis is shown in Fig. 6 where the peak noise is illustrated for the aforementioned two cases. Positive peak noise is in the range of 3 mV. The effect of dedicated on-chip power network for the analog and digital blocks is not significant primarily because off-chip parasitic impedances are dominant. The rms value of the noise over 10 μs is approximately 232 μV for common power network whereas the noise is reduced only to 224 μV for dedicated power network. Noise analysis results for the 3-D integrated potentiostat is described in the following section.

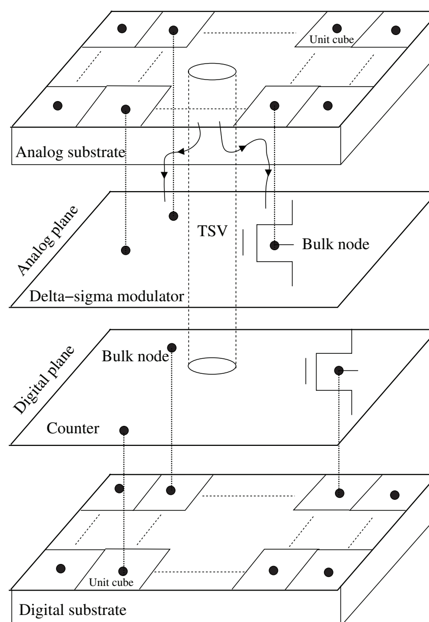

Fig. 7. **Conceptual representation of the overall model to analyze signal integrity in a 3-D potentiostat.**

2) 3-D Potentiostat with Two Stacked Planes: In the 3-D integrated version, the aggressor (counter) and victim (delta-sigma modulator) are placed on separate planes. Specifically, the top plane (closer to the I/O pads) is dedicated to the victim block whereas the bottom plane (closer to the heat sink) is dedicated to the aggressor block. A 3-D electrical model is generated using the aforementioned substrate and TSV models, as depicted in Fig. 7. Similar to the 2-D model, the bulk nodes within the schematic are connected to the corresponding nodes on the substrate. In this case, however, two separate substrates exist: (1) substrate of the bottom plane where the bulks of the counter are connected, and (2) substrate of the upper plane where the bulks of the delta-sigma modulator are connected.

As depicted in Fig. 7, a face-to-face bonding technology is assumed with via-first fabrication technique. In this technique, the TSVs go through the upper (analog) substrate and reaches the metal layers of the analog plane. The top most metal layer of the analog plane is connected to the top most metal layer of the digital plane using bumps. Note that a TSV pitch of 9 μm is assumed. Thus, there is at least a single free cuboid between the TSVs on the analog substrate. Since only a single channel of the device is modeled, eight TSVs are required: five for the clock signals (each at 1 MHz), two for power supply voltage (3 Volts), and one for data signal.

A transient analysis is performed and the noise at the bulk of the same victim device is observed. Peak noise is illustrated in Fig. 8 for two different cases: (1) nonideal TSVs with practical capacitance values, (2) ideal TSVs with zero capacitance value. Note that the result of the 2-D analysis (with dedicated power networks) is also included for comparison. As depicted in this figure, the 3-D system with practical TSVs, despite having separate substrates for aggressor and victim, exhibit significantly higher noise (positive peak noise exceeds

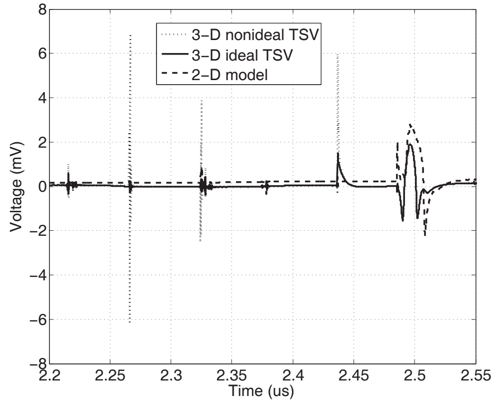

Fig. 8. **Transient analysis results illustrating peak noise at the bulk node of a victim device for two different cases in a 3-D integrated potentiostat.**

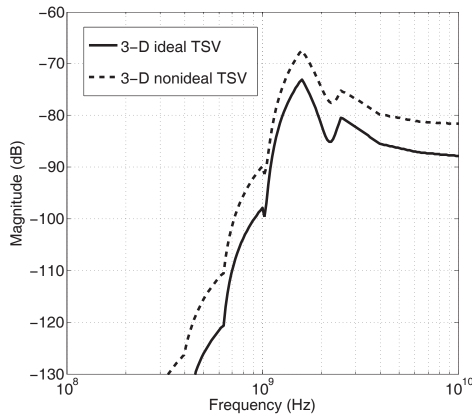

Fig. 9. **AC analysis results showing the amount of transferred noise from the clock signals to the victim bulk in a 3-D integrated potentiostat.**

six millivolts) than the 2-D system.

To determine the primary noise source, the capacitance C_{tsv} in Fig. 4(b) of the clock TSVs is removed, producing an ideal clock TSV with no coupling into the substrate. In this case, the peak noise is significantly reduced (to approximately two millivolts) and is smaller than the 2-D system. Thus, in a 3-D system, significant noise couples into the substrate through clock TSVs, as depicted in Fig. 7. This behavior is also analyzed by investigating the AC response. The magnitude of transferred noise from the clock signals to the victim bulk is shown in Fig. 9 as a function of frequency. The transferred noise is at least 5 dB higher when practical TSVs are used. Note that the ideal TSV is modeled only for the clock TSVs. In the presented 3-D results, noise still couples into the substrate through the remaining three TSVs (power and data). Finally, the rms value of the noise over 10 μs is listed in Table I for all of the cases. The advantage of 3-D technology in reducing noise is obtained only when TSV related noise coupling is alleviated. The implications of this conclusion on the design process are discussed in the following section.

IV. DISCUSSION

For applications such as the neurotransmitter sensing analyzed in this work, the top plane should be dedicated to the highly sensitive frontend circuits due to physical proximity to the pads. In this case, however, clock TSVs with short

TABLE I
RMS VALUE OF THE NOISE AT THE BULK NODE OVER 10 μS FOR DIFFERENT CASES.

Case	RMS noise at the bulk node
2-D common power network	232 μV
2-D dedicated power network	224 μV
3-D nonideal TSV	242 μV
3-D ideal TSV	107 μV

rise times inject significant noise into the substrate of the analog plane since these signals need to reach the bottom plane where the digital circuit is placed. This coupling mechanism is due to the TSV-to-substrate capacitance C_{tsv} of the TSVs. The distance between an aggressor TSV and a victim device should be carefully considered. Furthermore, efficient and 3-D specific noise isolation strategies should be developed.

V. CONCLUSIONS

3-D integration is an emerging technology with significant advantages for implantable devices such as reduction in form factor and power consumption. Signal integrity characteristics of a 2-D and 3-D integrated potentiostat are analyzed. An electrical model is developed to consider the substrate, nonideal power network, and TSVs. Contrary to the common assumption and despite having two separate substrates, 3-D systems do not necessarily exhibit superior noise performance due to TSV related noise coupling. Ignoring this noise coupling mechanism produces 3-D implantable devices with significantly poor signal integrity characteristics.

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